System-in-package solution for a low-power active electrode module

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***Abstract*— This paper presents the design of system in package for a low-power active electrode module. The main aim of this research is to provide a low-cost, high-density, and high-quality module, exploiting the features of a System-in-Package (SiP) solution. To the best knowledge of the authors, this is the first time that SiP technology has been used in the development of a modular active electrode. Two SiPs have been designed and one of them has been fabricated and tested. The dimensions of the latter are 7x7x1 mm and it was designed taking in account the necessity of soldering it by hand. On the contrary, the other package dimensions are 4.5x4.5x1 mm and it was designed for fully exploiting the latest technologies available to authors. The SiPs have been designed to be reused in different electrocardiogram (ECG) systems and are easy to solder using ball grids arrays (BGA) and land grids arrays (LGA) as second level interconnection; both these features allow to reduce the time to market of the supra-system including the module. The active electrode presents a bandwidth which ranges from 7.9m Hz to 300 Hz and it has a mid-band gain which can be set to a maximum value of 40 dB. The fabricated SiP has been tested on a printed circuit board (PCB), with an input signal generated by a Dimetek iBUSS-P biomedical signal simulator showing a satisfying functioning of the SiP.**

I. Introduction

The need for continuously monitoring bio-signals coming from elders and patients affected by chronic diseases, such as brain and heart electrical activity, has stimulated a large interest in the development of new ubiquitous healthcare monitoring systems. Either in electrocardiograms (ECG) and electroencephalograms (EEG), standard procedures consist of the use of wet and passive electrodes, which are attached to the patient's skin for measuring surface voltage fluctuations. Although these electrodes are low price, have a small size and are stable, several aspects make them unsuitable for long term monitoring [1]. In fact, the electrolytic gel utilised in wet electrodes, which is used to reduce the skin-electrode contact impedance as well as noise susceptibility, tends to dehydrate over time worsening signal quality. Moreover, patients need to face uncomfortable skin preparation, which includes cleaning, shaving, mechanical abrasion and moistening, before the electrodes can be applied [2].

As a consequence, over the last two decades two effective dry alternatives have been developed: micro needle array electrodes and active electrodes. Micro needle array electrode consists of the use of a micro patterned surface that penetrate the outer skin layer without touching any nerves and blood vessels, thereby reducing the interface resistance between electrode and skin without causing pain and bleeding [3].

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Active electrodes include an integrated amplifier on the electrode; this not only increases the input resistance of the electrode, but also amplifies the signal, reducing the effect of electrical interferences and motion artefacts picked up by the leads [5]. Although the first active electrode research dates back to 1960, this is still considered an attractive option with much room for improvement [6]. Active electrodes have been employed in several different applications such as contact [7] and non-contact [8] ECG/EEG electrodes. Even if this is a well know component for detecting biopotential signals, previous publications have never focused on developing an active electrode suitable for modular ECG or EEG systems. The main aim of this research is to design, fabricate and test a System in Package (SiP) accommodating the low-power bio-amplifier with DC rejection developed by Huang et al. [5], which for the first time is used in such application. Fig. 1 shows the block diagram of the designed system including the bio-amplifier, which is composed of components inside and outside the SiP. Beside the amplifier die, the SiP includes the passive components that compose a level-shifting circuit placed at the input of the bio-amplifier, and the passive components that compose a low pass filter placed at the output. For the active components, needed for the level-shifting circuit and the low pass filter, two off-the-shelf chips have been chosen and placed out of package.

SiP is a *more-than-Moore* technology which allows to bring together integrated circuits and passive components in order to include an entire system in a single module, improving the performance with respect to standard system-on-board and reducing fabrication cost and dimensions by means of integrated circuit stacking and embedded passive components [9], [10]. Although SiP technology may not guarantee the performance and reduced dimensions of a System on Circuit (SoC), it provides a quicker, lower cost, efficient, and low-

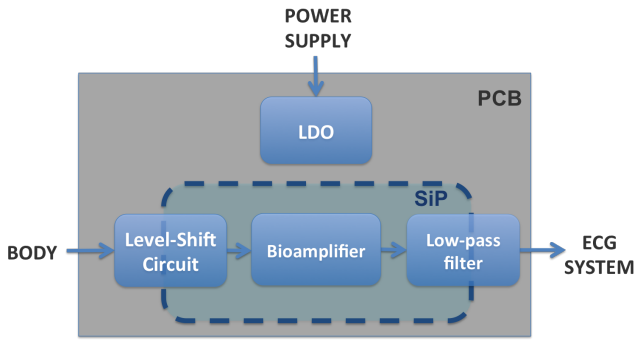

Fig. 1: System block diagram

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risk solution [10]. The SiP amplifier provides all the benefits guaranteed by a modular design, such as the reduction of time to market and the possibility of reusing the module in different products, such as different ECG systems [11]. Additionally, SiP technology provides more compact and more reliable solutions compared with previous modular designs. Previous research, such as [12], has dealt with ECG modular systems, however, to the best knowledge of the authors, no other publication has previously employed SiP technology for active electrode applications. This paper can be considered as a further step towards the development of completely modular ECG/EEG devices; this new market could promote the birth of new companies specialised in the development of single ECG/EEG modules.

The paper is organised as follows. In Section II, the description of two SiP designs is provided. The first one (SiP1), has been developed taking into account the need of hand-soldering the SiP onto a PCB; on the contrary, the second one (SiP2) has been designed without this constraint and for this reason smaller dimensions and higher input/output (I/O) density have been reached. Additionally, Section II includes a brief description of the bio-amplifier developed by Huang et al. [5] and the supra-system which includes the SiP (Fig. 1). In Section III, test procedure is described and, while in Section IV detailed test results are presented and discussed. Last but not the least, in Section V conclusions are drawn and future research is discussed.

II. Design

This section starts with a description of the integrated bio-amplifier. This is followed by a presentation of the two packages (SiP1 and SiP2) designed for the amplifier in question.

A. Integrated circuit

As was mentioned in Section I, for this work, the CMOS bio-amplifier for active electrode with DC rejection developed by Huang et al. [5] has been employed. This amplifier avoids amplifier saturation functioning as a high pass filter and at the same time it provides a high input impedance; these features make it suitable for an active electrode application. This amplifier operates at $\pm$ 0.9 V supply voltage; it has a mid-band gain of 40 dB with $\pm$ 300 mV DC offset rejection and has a power consumption of 6.7 μW. The bandwidth extends from a low-frequency cutoff of 7.9 mHz to a high-frequency cutoff of 2.1 kHz. This amplifier has an input-referred noise of 5.9 μV_{rms} [5]. The schematic of the amplifier is shown in Fig. 2 and the transfer function H(s) is given in (1):

$$H(s) = A_d \frac{sR_0C_0}{(1+sR_0C_0)(1+s\frac{A_d\tau_1}{A_1})(1+s\frac{\tau_2}{A_2})} \quad (1)$$

where $A_d = (1+\frac{R_2}{R_1})(1+\frac{R_4}{R_3}), R_0$ is the equivalent impedance of pseudo resistors M1 and M2; A1, A2 are DC open-loop voltage gains of op-amps AMP1 and AMP2; τ_1 and τ_2 are the time constants of the dominant pole of op-amps AMP1 and AMP2. In this work, the magnification A_d has been set to 20.

The circuit has been fabricated in 0.18μm 1P6M CMOS process, and its final die is approximately 2.64 mm long and 1.14 mm wide.

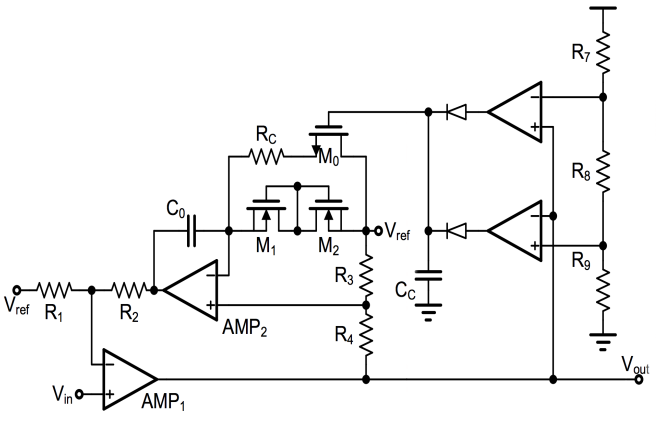

Fig. 2: Schematic of the amplifier

B. SiP1

Both Sip1 and SiP2 have been designed using Cadence SiP RF Layout. In particular, SiP1 has been developed taking in account hand-soldering procedure. Although, as described in the next few paragraphs, one of the main advantages of SiP consists of having a high I/O density by means of Land Grid array (LGA) or Ball Grid array (BGA) [13], [14], SiP1 has been produced with the purpose of testing in mind. Since low-cost and quick hand-soldering was necessary, the optimal I/O density has not been reached. This package is a parallelepiped with a 7x7 mm surface area and a 1 mm height as shown in Fig. 3a. The substrate and mold materials are HL832NX and eme-g760 Type L, respectively. Both of them have been chosen for their sufficient mechanical and thermal performance and relatively low price.

The substrate is composed by the above mentioned laminate separating four embedded copper layers (30 μm thick): two of them (the last and the first on the stack) are pattered, defining the internal circuit; on the other side, the other two are not patterned and are designed to be directly connected to external power and ground through several vertical viae, which connect the layers with the bottom of the package. These choices optimise the power distribution network minimising the power/ground inductance inside the module [15], [16].

The integrated circuit has been placed face up and connected to the substrate via 18 μm golden wires. Passive components (SMD0402 capacitors and resistors) have been placed on the patterned layers. As power and ground planes, the chip and the rest of the internal circuit are connected to the bottom of the SiP through vertical viae.

The SiP interfaces with a PCB via a LGA. This second-level interconnection is composed by an array of solderable surfaces and provides a higher I/O density than the classic quad flat pack (QFP), allowing to interface with the SiP

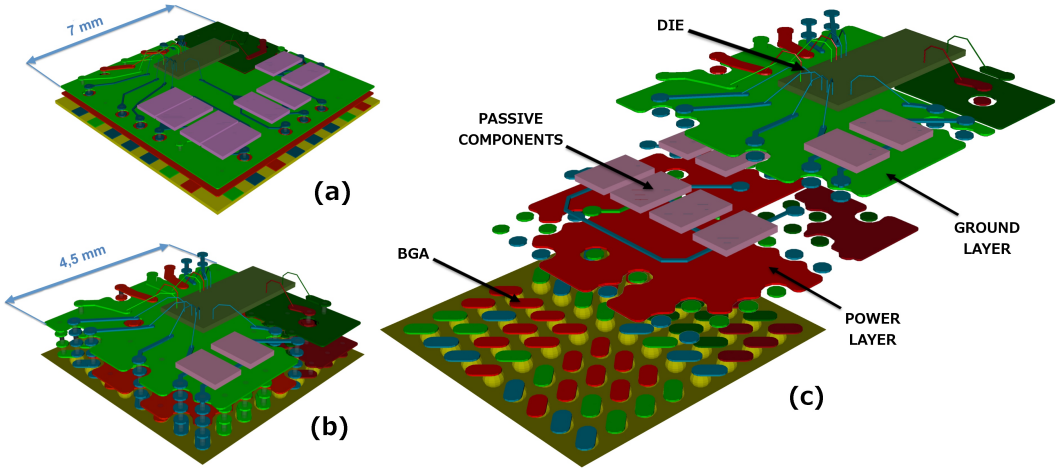

Fig. 3: (a) SiP1 design draw (b) SiP2 design draw (c), SiP2 cross section (laminate is not displayed).

directly from the bottom surface; this is an attractive alternative to using "gull wing" leads, which normally imply waste of PCB area and higher inductance [14]. Moreover, LGA provides soldering self alignment during automatic soldering, drastically reducing soldering time. The 30 LGA contact surfaces used for this design are placed on the border of the bottom surface for facilitating hand soldering; they are 400 μm long and 400 μm wide and are placed at a distance of 400 μm from each other. Bottom and top view of the final product are shown in Fig. 4.

C. SiP2

SiP2 has been designed with the purpose of providing a SiP as small as possible, increasing the number of potential applications of the product. SiP2 has a 4.5x4.5 mm surface area and its internal structure has been obtained scaling down SiP1. SiP2 design is shown in Fig 3b. The main difference between the two designs consists of the use of a BGA second level interconnect in SiP2, designed according to the JEDEC standard. The chosen BGA is composed of a 64 solder balls matrix with a 250 μm diameter and a 500 μm pitch.
Although a BGA could experience balls loss and provide a higher mounted height than LGA, this choice makes the package easier and quicker to solder. As a consequence, the system containing this SiP will experience a further reduction of the time to market. BGA, like LGA, provides high I/O density, high electrical performance, high thermal performance and soldering self alignment [14]. For SiP2, the highest I/O density available to the authors has been utilized. Additional differences between SiP1 and SiP2 are due to the reduced section area; in fact, for placing a sufficient number of power and ground viae in SiP2, a full matrix BGA has been chosen; this choice avoids compromising the power distribution network. Additionally, smaller passive components (SMD0201) have been chosen and most of them have been embedded in a fifth layer as shown in Fig 3c.

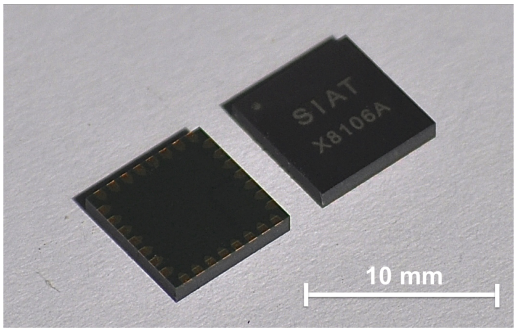

Fig. 4: System in Package: bottom and top view

D. Supra-system

The supra-system, which accommodates SiP1, includes a Low Dropout regulator (LDO) and the active components of a level-shifting circuit and a low pass filter. As shown in Fig. 1, the ECG signal coming from the body passes first through the shifting-level circuit, which adds a 0,9 V DC offset to adapt the signal to the chip input voltage range (0-1.8 V). The shifting-level circuit is composed by some of the passive components placed on the SiP and a MCP6002 opamp, which for the moment has been placed outside the SiP.
The bio-amplifier is followed by a low-pass filter; this is used for decreasing the high-frequency cutoff of the active electrode down to 300 Hz (originally set at 2.1 kHz [5]). This component has been left out from the initial bio-amplifier die so that the bandwidth can be changed according to which kind of bio-signal needs to be measured; the 300 Hz cutoff makes the amplifier suitable for ECG signals. The filter is composed of passive components placed on the SiP and a MCP6002 opamp outside. For this component a second-order Butterworth filter configuration has been used.
As already stated, the PCB also includes a LDO (TPS71701) for converting the supply voltage to a stable 1.8 volts value.

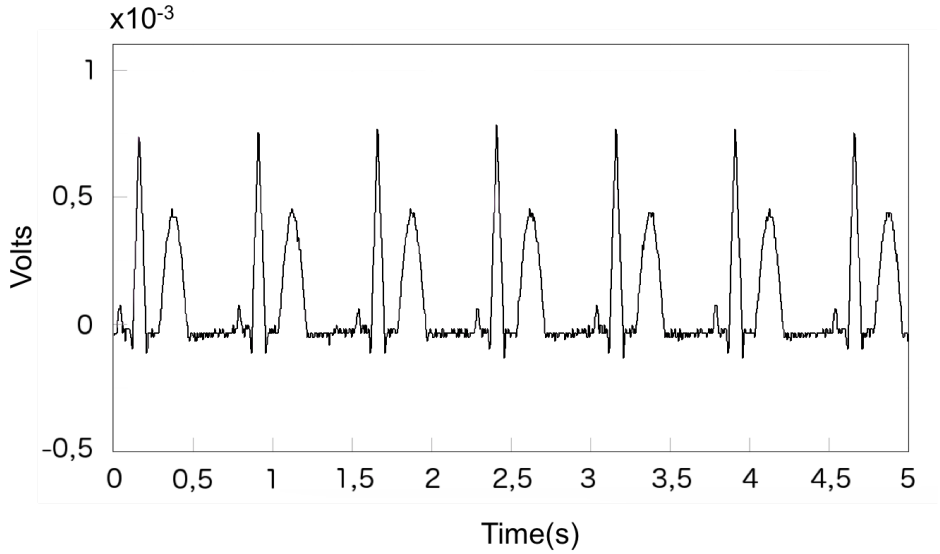

Fig. 5: Lead I ECG signals recorded using the presented active electrode

III. Test set up

For testing purpose the supra-system, including the SiP, has been reproduced on a round PCB with a diameter of 25 mm. The test PCB is shown in Fig. 6. The active electrode has been tested by feeding its input via wires with an ECG simulation signal coming from a Dimetek iBUSS-P biomedical signal simulator. This device reproduces several kinds of small clinical signals, such as EEG, ECG, EMG and ERP signals. More specifically, the active electrodes have been used for measuring the simulation of a lead I signal. The oscilloscope used for output detection is an Agilent DSO5034A and the power supply is an Agilent E3620A.

IV. Result and discussion

Regarding the soldering procedure, the hand soldering of SiP1 has not fully exploited the advantages of the LGA choice; in fact, the time taken for soldering SiP1 by hand was almost the same as soldering a QFP with the same number of input/output ports. However, an automatic soldering process would experience a consistent reduction in time. Fig. 5 shows the output waveforms detected by the Agilent E3620A. A good quality ECG signal was found at the output of the testing PCB. Moreover, the test showed the continuity and the stability of the active electrode when tested for 24hours. Experimental results showed that the entire system (Fig. 1), working with a single 5V power supply, required a power consumption around 20 mW.

When the feasibility of an active electrode in SiP has been proved, this technology could be applied in previous non-intrusive ECG systems such as [17], [18]. In both cases, the active electrodes are placed on a PCB and so, the soldering time could be drastically reduced by a SiP solution. Moreover, the same or smaller dimensions are guaranteed. The presented active electrode, after the necessary bandwidth adjustment, could also be employed in ECG active electrodes such as [19].

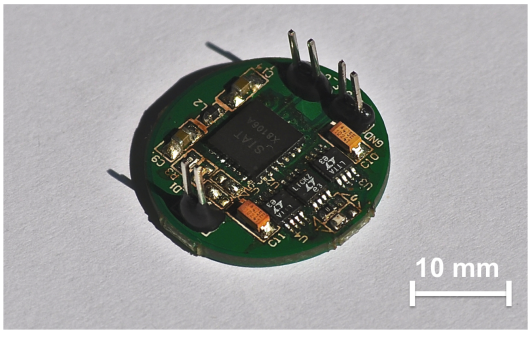

Fig. 6: Complete active electrode on PCB

V. Conclusion

In this paper, the active electrode developed by Huang et al. [5] has been included in a System in Package module. The resulting ECG active electrode can be included in a non-intrusive monitoring system for keeping track of the patients heart condition and predicting impending events. The novelty of this work includes: 1) first use the 6.7 μW CMOS bio-amplifier with DC rejection developed by Huang et al. [5]) for an active electrode and, 2) a new application of the System-in-Package technology for an active electrode module.

The final product has shown good-quality ECG output signal, and has provided the advantages typical for SiP technology. Future work will include the insertion of active components in the package, which so far have been left out. Rather than using off-the-shelf chips, the LDO and the two amplifiers will be designed and integrated in dies that will subsequently be stacked over the active bio-amplifier. Moreover an analog to digital converter will be inserted in the SiP. These will only affect the height of the package.