A Novel Biphasic-Current-Pulse Calibration Technique for Electrical Neural Stimulation

Maohua Ren, Jinyong Zhang, Lei Wang *IEEE Member,* and Zhenyu Wang

Abstract— **One of the major challenge in neural prosthetic device design is to ensure charge-balanced stimulation. This paper presents a new calibration technique to minimize the mismatch between anodic and cathodic current amplitudes. The proposed circuit mainly consists of a digital and an analog calibration, where a successive approximation register (SAR) logic and a comparator are used in digital calibration while a source follower is adopted in analog calibration. With a 0. 18 µm high voltage CMOS process, the simulation shows that the maximum current mismatch is 45 nA (<0.05%).**

I. Introduction

During the past decade, the development of biomedical implantable functional electrical or neural stimulation (FES/FNS) has made great progress in neural rehabilitation, such as cochlear prostheses for the deaf, deep brain stimulators for Parkinson's disease and retinal prostheses for the blind. The principle of neural stimulation is exciting a neural reaction by transferring charge into the neural tissue. In order to avoid irreversible electrochemical reactions leading to dissolving the metal electrode and generating toxic by-product, a zero-net charge transfer into neural tissue during electrical stimulation is a challenging problem.

However, in practical implementation, it is difficult to realize the perfect matching between the current drivers due to the CMOS process variation. The typical mismatch between current source and current sink is around 1% or 2% even if careful layout and design technologies are employed. It has been reported that the residual DC current of more than 100 nA is highly correlated to the neural tissue damage [1]. Therefore, considerable efforts have been made to address the above problem in recent years.

Among these technologies, implementing large blocking capacitor between the output terminal and the electrode is a conventional approach. The main issue of this method is that it is difficult to be integrated into silicon due to the large die area, particularly for multi-channel array neural stimulator. Active charge balancers [2] is an effective scheme to monitor any residual charge in the tissue after each stimulation and keep this residual charge within a safety range of about ±100 mV, but the high complexity of the circuitry limits its application. Analog feedback technique used to sample and hold the matching current has been introduced in [3]-[4]. Reference [5] presented another analog dynamic current matching technique. The cathodic current is generated by a DAC and then sampled by a PMOS transistor to reproduce the matching anodic current. However, the leakage current of the sampling capacitor and injection error of the sample/hold switch limit the accuracy of the output current. Digital calibration technique was implemented to reduce the residual charge in [6]. In this reported work, a comparator is used to detect the mismatch current and the output of the comparator is connected to a logic circuit, which adjusts the DAC to realize current matching. The drawback of this method is that the mismatch between anodic and cathodic current are still exist due to the least significant bit (LSB) quantization error or the resolution of the DAC.

To reduce the LSB quantization error and the mismatch currents caused by the injection error and leakage current, this paper proposed a new neural-stimulator based on mixed mode calibration scheme. The organization of this paper as follows, Section II presents the neural-stimulator and discusses the detailed circuits. Simulation results are given in Section IV and Section V gives the conclusion.

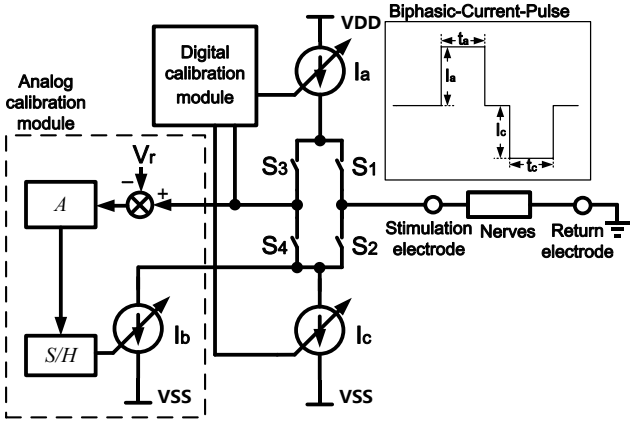

Figure 1. Model of the monopolar curent stimulation with proposed calibration technique (assuming Ia > Ic).

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M. H. Ren is with Institute of Biomedical and Health Engineering, Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, Shenzhen, China. He is also with the School of software and microelectronics, Peking University, Beijing, China (e-mail: mh.ren@siat.ac.cn).

J. Y. Zhang is with Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong, China. He is also with Institute of Biomedical and Health Engineering, Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, Shenzhen, China (e-mail: jyzhang@eee.hku.hk).

L. Wang is with the Institute of Biomedical and Health Engineering, Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, Shenzhen, China (phone: 86-755-26803549; fax: 86-755-26803538; e-mail: wang.lei@siat.ac.cn).

Z. Y. Wang is with the School of Software and Microelectronics, Peking University, Beijing, China (e-mail: zw@ss.pku.edu.cn).

II. PROPOSED NEURAL-STIMULATOR

A. Architecture of the Proposed Neural-stimulator

The architecture of the proposed neural-stimulator is demonstrated in Fig.1. I_a and I_c are programmable current drivers, which are used to produce stimulation current pulse. The calibration circuitry, including digital and analog module, is used to achieve precise matching current between I_a and I_b+I_c. The analog calibration is realized via control block diagram. I_b is an auxiliary current sink, which is designed to compensate the mismatch between Ia and Ic. To keep the output current I_b stable, a sample/hold circuitry is designed in analog calibration module.

The proposed neural-stimulator offers two working modes: stimulation mode and calibration mode. The stimulator works in stimulation mode when switches S_3 and S_4 are off. In this situation, the anodic current flows from the electrode to neural tissue if S_1 is on (S_2 is off), and cathodic current flows in the opposite direction if S_2 is on (S_1 is off). In the calibration mode, S_3 and S_4 turn on (S_1 and S_2 are off), which means that calibration circuitry is only enabled in calibration mode. In addition, analog calibration module is disabled when digital calibration module is working.

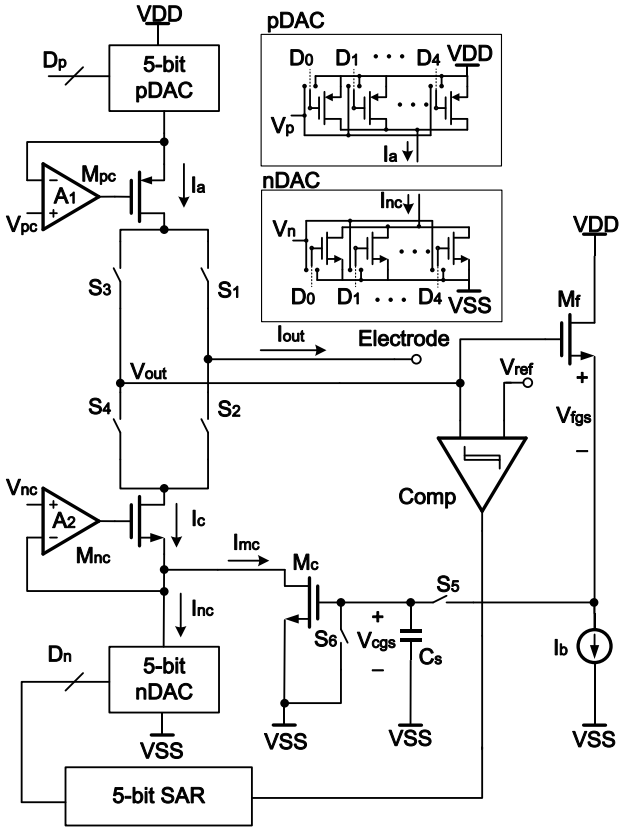

Figure 2. Simplified schematic of the proposed neural-stimulator.

B. Programmable Current Driver

As shown in Fig.2, the current source and current sink are both 5-bit binary-weighted current DACs by using PMOS transistors (pDAC) transistors and NMOS transistor (nDAC), respectively. An active feedback scheme is adopted in current drivers to achieve high output impedance, which can ensure a large output swing. Fig. 3 presents the output voltage versus output current of both current source and sink, I_a and I_c, where the cross point of the two curves is closed to either VSS or VDD. It is apparent that the output current amplitude either current source or current sink is nearly constant when current drivers works in the active region. Therefore, this characteristic can be used in detecting the mismatch between I_a and I_c by implementing a comparator based on the above principle.

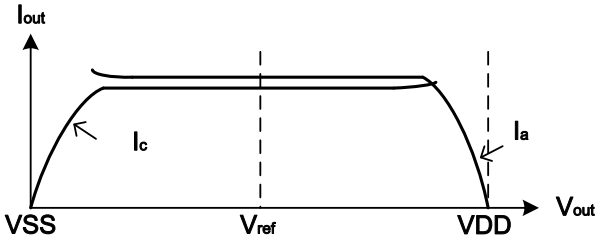

Figure 3. Output of the current source and current sink vs. output of current driver with active feedback scheme.

C. Digital Calibration Module

The purpose of the digital calibration is to adjust nDAC to achieve matching between I_a and I_c. The amplitude of I_a is controlled by a 5-bit digital code D_p and I_c is controlled by the SAR logic circuitry, respectively. The basic principle of digital calibration is that if I_a is larger (smaller) than I_c in stimulation mode, the V_{out} will be kept closed to VDD (VSS) in digital calibration mode.

As demonstrated in Fig. 2, the S_6 turns on and S_5 turns off, therefore analog calibration module is disable in the digital calibration procedure. After setting the input code of D_p, the SAR logic adjusts the output current of nDAC to match I_a. The detailed procedure of the digital calibration can be described as follows; firstly, the SAR logic set the most significant bit (MSB) of the input code of nDAC and then detect the output of the comparator. If the output of comparator is low, then the MSB is reset. The following bits are determined as similar as MSB. As show in Fig.4, T_c is the time interval of detecting and setting each bit of nDAC. D_n is stored in register when digital calibration is finished and the final mismatch between I_a and I_c is less than least significant bit (LSB) quantization error.

D. Analog Calibration Module

In analog calibration procedure, S_5 turns on and S_6 turns off to enable M_c, which is the auxiliary current sink. A sampling capacitor C_s, M_c, M_f as well as I_b forms a negative feedback loop to pull V_{out} to V_{cgs}+V_{fgs}, and the output of the auxiliary current sink, I_{mc}, equals to the difference between Ia and Inc. Therefore, I_a matches I_c adaptively based on the feedback mechanism. Then S_5 turns off and V_{cgs} is stored in C_s. The analog calibration procedure is keeping unless the digital calibration is formed as depicted in Fig.4.

The gate-source voltage V_{cgs}, equals to the voltage across sampling capacitor. The drain current of the MOS transistor operating in the saturation region is given by

$$0.5\mu C_{ox}(W/L)(V_{cgs}-V_{th})^2 = I_{mc}. \quad (1)$$

Based on the above equation, the variation of drain current ΔI_{mc} can be obtained if there is error ΔV_{cgs} of V_{cgs} caused by injection error and leakage current.

$$\Delta I_{mc} = 0.5\mu C_{ox}(W/L)[2(V_{cgs}-V_{th})\,\Delta V_{cgs}+\Delta V_{cgs}^2], \quad (2)$$

and

$$\Delta I_{mc}/I_{mc} \approx (2\Delta V_{cgs})/(V_{cgs}-V_{th}). \quad (3)$$

Assuming that $\Delta V_{cgs}/V_{cgs}$=5%, V_{cgs}=1.0 V, V_{th}= 0.7 V, I_{nc} is constant and $I_{nc} = I_{mc}$, then $\Delta I_{mc}/(I_{nc} + I_{mc})$ is around 16.7%. While if $I_{nc} = 9I_{mc}$, thus $\Delta I_{mc}/(I_{nc} + I_{mc})$ is decreased to 3.3%.

For one thing, to reduce the current error caused by the dynamic voltage stored in the sampling capacitor, a feasible method is decreasing the percentages of the output current depending on the dynamic sampled voltage and the remaining output current should only be determined by the constant voltage (e.g., voltage reference). For another, LSB quantization error still exists after digital calibration. Theoretically, this error can be reduced by implementation of a high-resolution current DAC, which will lead to high complexity of the circuits. Therefore, an optimized analog calibration scheme without using complex DAC is adopted after the digital calibration procedure in this proposed stimulator to reduce the LSB quantization error.

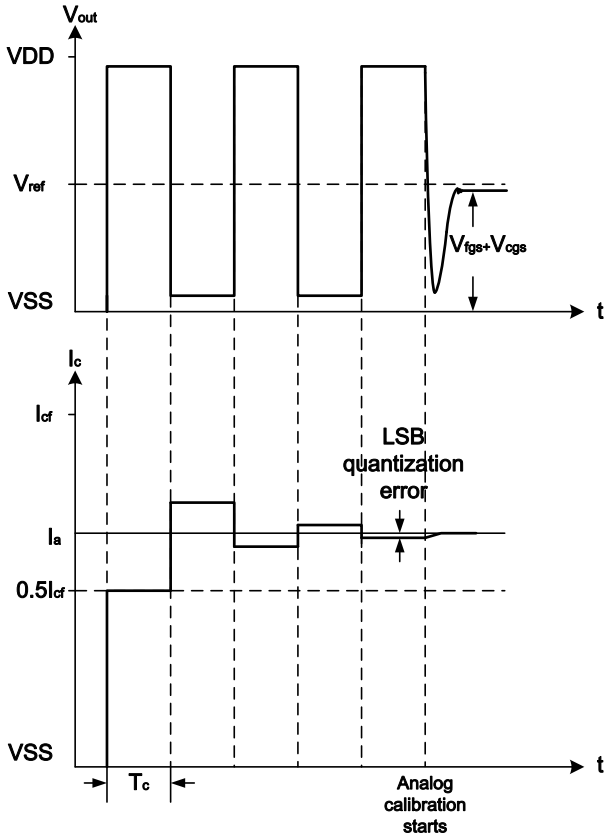

Figure 4. The waveform of calibration procedure.

Although the digital calibration performs before the analog calibration as shown in Fig.4, the digital calibration needs to be executed only once when the input code of pDAC is changed. To ensure the accuracy of the stimulation current, the analog calibration needs to be executed at each inter-phasic period (the interphase interval between anodic and cathodic pulses). Fig .4 suggests that mixed mode combined the digital calibration with analog calibration can effectively eliminate the mismatch error as discussed above.

E. Circuits Implementation Issues

Considering that the load impedance is about 10 KΩ and the power supply is 3.3 V, the output swing range of the stimulator is about from 0.3 V to 3 V. Full-scale output current amplitude of the pDAC is 155 μA, and that of the nDAC is 186 μA. The configuration of nDAC ensures that the I_a can be matched even if the process variation exists. A voltage bias circuit is implemented to generate V_n, V_{nc}, V_p and V_{pc}, as shown in Fig. 5. V_n and V_p are bias voltage for nDAC and pDAC, respectively. A_1 and A_2 are operational amplifier with about 70 dB DC gain and rail-to-rail output swing to enhance the impedance of the current drivers. The comparator is design with hysteresis characteristic to suppress the impact of noise. Switch S_5 is designed with dummy transmission gate [4] to minimize the charge injection error. The sampling capacitor C_s is about 1 pF in this design.

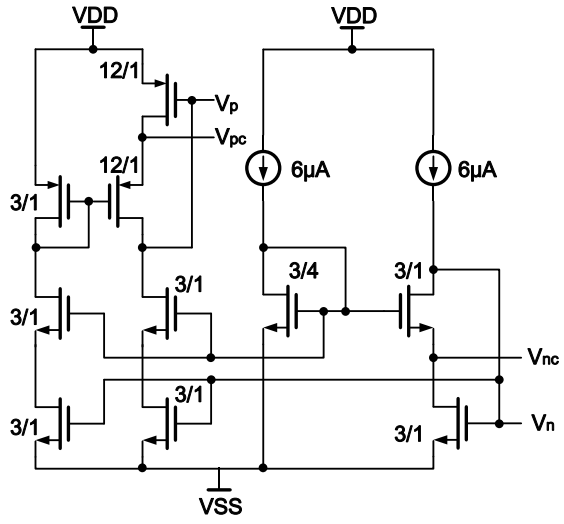

Figure 5. Schematic of voltage bias circuit

III. Simulation Results

The neural-stimulator has been implemented using 0.18-μm high voltage CMOS process. Fig. 6 shows the simulation waveform of calibration procedure. The stimulation current amplitude is set to 155 μA (D_4 D_3 D_2 D_1 D_0 = 11111). The input code of nDAC is adjusted by SAR logic as follow, D_4 (MSB), D_3 and D_1 are set (high) while D_2 and D_0 are reset (low). The digital calibration starts at 10 μs and finishes at 135 μs, and the the final value of the V_{out} is 1.53 V after a 3 μs setting time in analog calibration. Fig. 7 shows the amplitude of biphasic current versus DAC input code. The maximum output current 156 μA is achieved. The LSB current is about 5 μA with the 5-bit resolution DAC.

To further analysis the range of the mismatch of stimulation current, simulation runs at each input code of pDAC, as shown in Fig.8. The total mismatch current is less than 45 nA based on the proposed mixed analog and digital calibration scheme. The largest amplitude of mismatch current (45 nA) occurs in the situation that output current amplitude is 90 μA. The reason for this is that I_a is slightly smaller than I_c but V_{out} is still larger than V_{ref} after the digital calibration when output current achieves 90 μA. Therefore, Mc turns off in analog calibration.

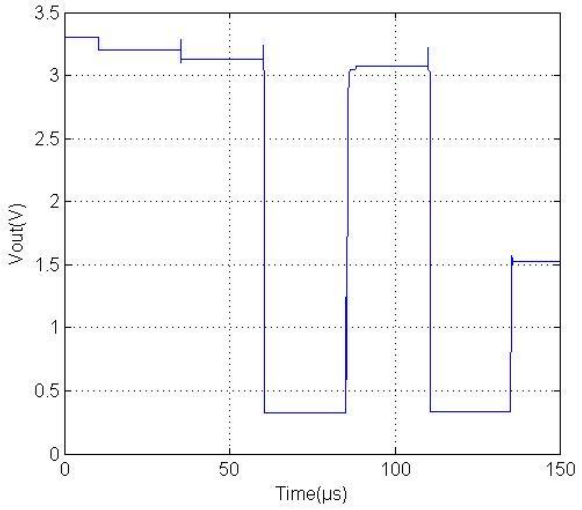

Figure 6. Simulation waveform of calibration procedure at 156μA output current.

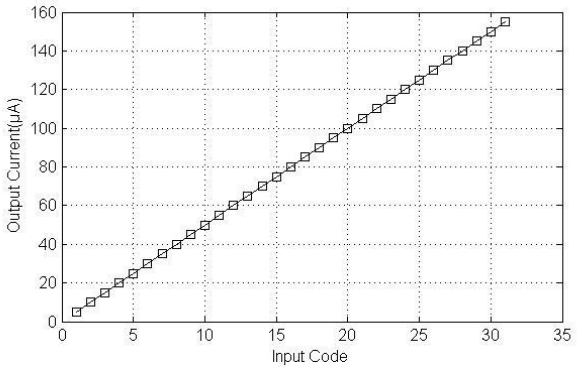

Figure 7. Output current versus input code.

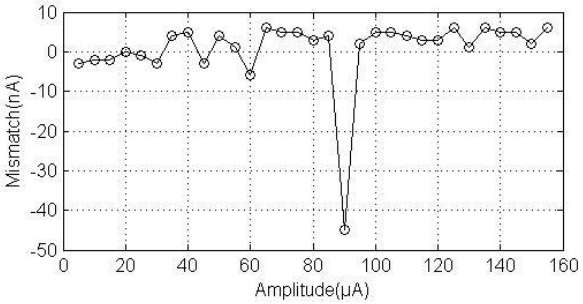

Figure 8. Mismatch current (Ia-Ic).

TABLE I. PERFORMANCE CAMPARISON WITH PREVIOUSLY REPORTED STIMULATORS

	TBCAS 07[7]	JSSC 05[8]	BioCAS 09*[3]	EMBC 12*[5]	**This Work***
Full Scale Current (μA)	1000	600	1000	476	**155**
Current Mismatch (μA)	4	7.2	0.3	0.3	**0.045**
Supply Voltage(V)	+6 -9	+6.5 -6.5	+5 -5	+3.3	**+3.3**
Process (μm)	HV 0.7	1.5	HV 0.35	LV 0.065	**HV 0.18**

* Simulation result

IV. CONCLUSION

This paper presents a new biphasic-current-pulse calibration technique based on mixed analog and digital calibration for neural stimulation devices. To realize matched biphasic-current-pulse, a SAR logic and a comparator are adopted for digital calibration, and a source follower is used for analog calibration, which reduces the LSB quantization error of digital calibration. The mismatch current caused by the injection error and leakage current is effectively suppressed by minimizing the dynamic compensating current (current depending on the dynamic sampled voltage). The simulation results show that the maximum mismatch of a biphasic current pulse is around 45 nA (<0.05%) based the propose calibration scheme.

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