A Dual Slope Charge Sampling Analog Front-End for a Wireless Neural Recording System

Seung Bae Lee, Byunghun Lee, Benoit Gosselin, and Maysam Ghovanloo

***Abstract*—This paper presents a novel dual slope charge sampling (DSCS) analog front-end (AFE) architecture, which amplifies neural signals by taking advantage of the charge sampling concept for analog signal conditioning, such as amplification and filtering. The presented DSCS-AFE achieves amplification, filtering, and sampling in a simultaneous fashion, while consuming very small amount of power. The output of the DSCS-AFE produces a pulse width modulated (PWM) signal that is proportional to the input voltage amplitude. A circular shift register (CSR) utilizes time division multiplexing (TDM) of the PWM pulses to create a pseudo-digital TDM-PWM signal that can feed a wireless transmitter. The 8-channel system-on-a-chip was fabricated in a 0.35-µm CMOS process, occupying 2.4 × 2.1 mm^2 and consuming 255 µW from a 1.8V supply. Measured input-referred noise for the entire system, including the FPGA in order to recover PWM signal is 6.50 µV$_{rms}$ in the 288 Hz~10 kHz range. For each channel, sampling rate is 31.25 kHz, and power consumption is 31.8 µW.**

I. Introduction

Importance of the neural interfacing technology has been on the rise as advanced research in both electrophysiology and behavioral neurosciences are directed towards forming a better understanding of the underlying principles of the human brain and root causes of malfunction in its neuronal circuits. In particular, understanding the mechanisms behind effective therapies, such as deep-brain-stimulation (DBS), which has shown very promising clinical results in Parkinson disease, tremor, movement disorders, and even depression is important. To extend these medical breakthroughs to other neurological diseases, such as epilepsy, dementia, and Alzheimer's disease, multi-site monitoring of the brain activities is essential. Many researchers are engineering multichannel neural recording systems to meet the needs of neuroscience community.

A conventional AFE architecture consists of several voltage gain stages and filters. Then, the signal is buffered, multiplexed before a sample-and-hold (SHA), and digitized using a low power, medium resolution analog to digital converter (ADC). According to the analysis in [1], as the number of channels increases, conventional AFEs consume high power in the buffer and ADC blocks because conversion per channel needs to be completed in a short period of time.

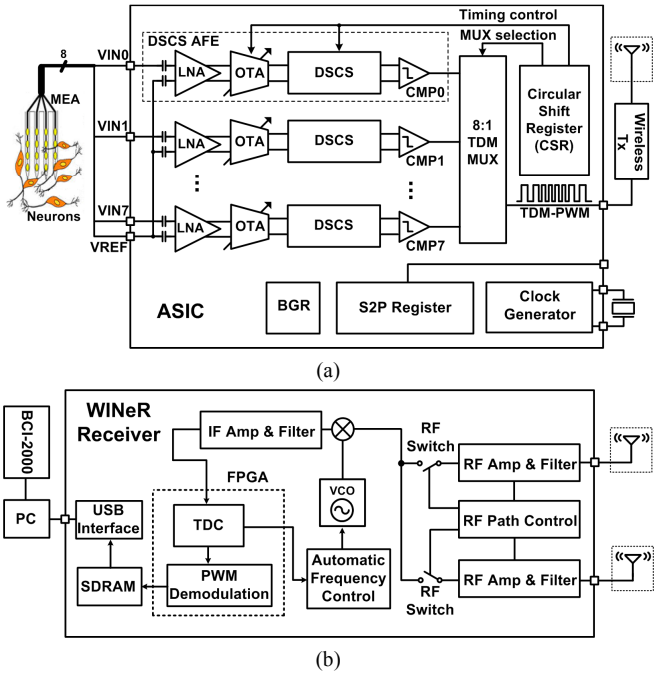

Fig. 1. Block diagram of an 8-ch DSCS-based wireless implantable neural recording (WINeR-6.5) system, (a) Transmitter unit, (b) Receiver unit.

In order to improve the power efficiency of the AFE for multichannel neural recording systems, here we present a dual slope charge sampling (DSCS) architecture. Charge sampling mechanism has been used recently in neural recording interfaces because it is stronger than voltage sampling in terms of wideband operation and provides an inherent pre-filtering function provided by integration [2]-[4]. The proposed DSCS-AFE architecture utilizes the charge sampling benefits while converting input signals to PWM pulses, and eliminating the need for high-speed ADCs on the transmitter unit (Fig. 1). These features render the proposed DSCS-AFE architecture a suitable choice for large channel count systems with limited available power and channel bandwidth.

The prototype presented here is an 8-channels DSCS AFE with additional control circuitry. However, it can be easily extended to higher channel counts. Next section describes the entire wireless integrated neural recording (WINeR) system. section III describes the DSCS-AFE architecture, and section IV includes the measurement results followed by conclusions.

II. System Architecture

A. Transmitter (Tx)Unit

A simplified block diagram of the WINeR-6.5 ASIC is shown in Fig. 1a. Fully differential low noise amplifiers

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(LNA) amplify and filter neural signals with a gain of 100 V/V and adjustable bandwidth. A variable-g_m operational transconductance amplifier (OTA) converts the amplified signal to current with 3-bit binary control over g_m. The DSCS block pulse width modulates (PWM) the neural signal by comparing differentially charged and discharged capacitors via a fast hysteresis comparator. A time division multiplexer (TDM) combines the eight PWM outputs of the DSCS blocks and generates a TDM-PWM signal. A circular shift register (CSR) controls the AFE timing. The pseudo-digital TDM-PWM signal can be directly fed into a wireless Tx to be transmitted using various modulation schemes such as frequency-shift keying (FSK) and on-off keying (OOK). A serial-to-parallel (S2P) 32-bit register was also implemented in order to control various adjustable parameters among the 8 channels.

B. Receiver (Rx) Unit

Block diagram of the WINeR wideband Rx unit has been depicted in Fig. 1b, which has been designed to demodulate and digitize the incoming FSK-TDM-PWM signal (424/442 MHz). The RF signal is picked up by two individual antennas to enhance the wireless coverage over the experimental space, and amplified and filtered by a pair of identical RF front-ends. A control circuit then connects the RF path with stronger signal to a mixer, which down-converts the received RF signal to baseband (41/59 MHz) before demodulating the FSK signal in an FPGA. The resulting TDM-PWM signal is then fed into a time-to-digital converter (TDC) in the same FPGA to generate the digitized samples, which are demultiplexed and buffered in a 1 Mbit SDRAM to handle data transfer delays and transferred to a PC through USB port. A general-purpose open-source platform, called BCI2000, often used with EEG signals for brain-computer interfacing (BCI) applications, runs on the PC to show the received neural signals on the screen and save them in the hard disk in real time [5].

III. DSCS-AFE ARCHITECTURE

The proposed DSCS-AFE schematic diagram is shown in Fig. 2a. The neural signal is amplified in a fully differential LNA. LNA also plays the role of a band-pass filter composed of feedback capacitors and pseudo resistors that are located on the front end and in the feedback loop [6]. The variable-g_m OTA converts the amplified neural signal into a differential pair of currents, which are integrated in two capacitors, C_{C+} and C_{C-}, for a fixed time period, Φ_1, which is labeled as "Charging" period in Fig. 2b. The slope of the capacitor voltages, V_{C+} and V_{C-}, during the charging period depends on the amplitude of the neural signal within that period. Before the charging period, there is a "Precharging" period, Φ_0, during which the capacitor voltages are set to a pair of well-defined preset values, Preset_+ and Preset_-.

Following the charging period, a constant current source and current sink discharge C_{C+} and C_{C-} during another constant period, Φ_2, that is labeled in Fig. 2b as "Discharging" period. V_{C+} and V_{C-} are compared by the fast hysteresis comparator, which is only enabled during Φ_2 to save power. The resulting comparator output is a PWM signal, which duty cycle, T_{PWM}/Φ_2, is proportional to the amplitude of the differential LNA input voltage, V_{IN}-V_{REF}, on the basis of the DSCS mechanism.

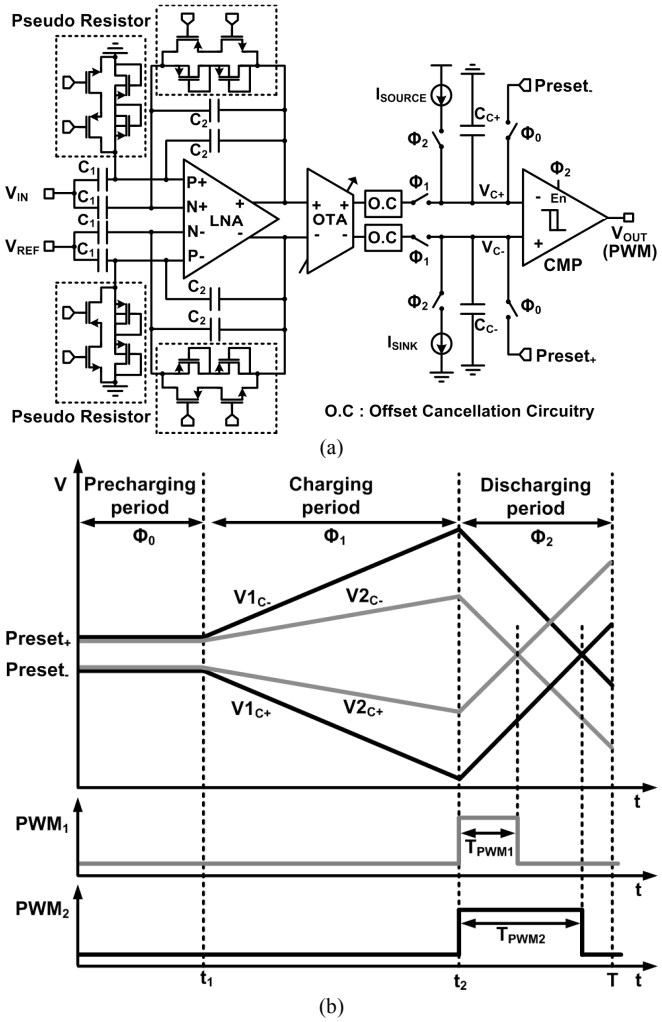

Fig. 2. DSCS-AFE for a single channel: (a) Block diagram, (b) Operating waveforms of the dual-slope integration for two different input voltages.

There are several advantages in using a dual slope integration compared to a single slope that was previously used [5]. First, the amplitude-to-time conversion (ATC) accuracy is independent of both the capacitance values and the clock frequency because they affect both the charging slope and the discharging slope by the same ratio. Second, the fixed input signal integration period results in attenuation of background and LNA noise components on the analog input. Third, there is no need for a separate high precision triangular wave generator, which results in additional power saving.

A. LNA

The proposed LNA uses a complementary input stage in order to double the effective transconductance with a given bias current [6]. Detailed schematic diagram of the LNA and its common-mode feedback (CMFB) is shown in Fig. 3.

B. OTA

The OTA schematic is shown in Fig. 4. It converts the amplified differential voltage at the LNA output to differential current at the input of the DSCS stage. Following a simple differential pair, differential currents are fed into a variable gain fully differential current amplifier stage. The overall g_m of the OTA is adjustable by controlling current mirror ratios

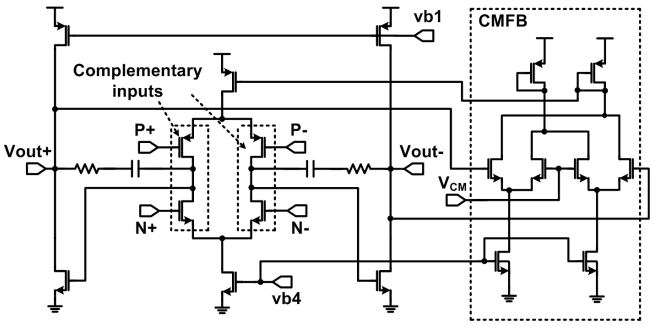

Fig. 3. Schematic diagram of the fully-differential LNA with CMFB.

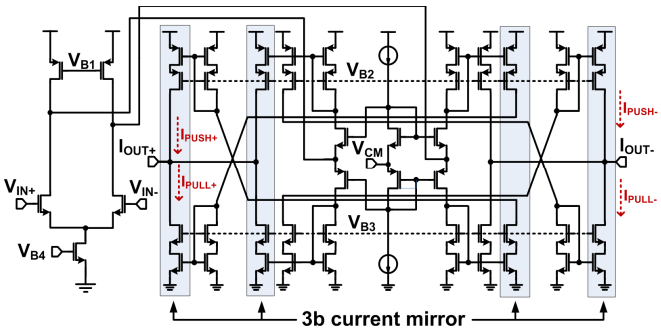

Fig. 4. Schematic diagram of the fully diff. OTA with 3-bit adjustable g_m.

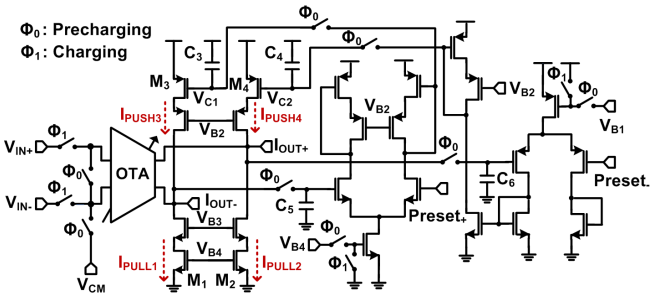

Fig. 5. Schematic diagram of the DSCS block including OTA offset cancellation circuitry.

of the current amplifier stage by 3 bits. The cascode mirror structure in the output stage reduces the non-linearity in charging and discharging output currents due to variations in the output voltages, V_{C+} and V_{C-}.

C. DSCS and OTA Offset Cancellation

At the end of Φ_0, when the OTA outputs are connected to C_{C+} and C_{C-}, the voltage difference between floating OTA outputs and the capacitors, which are precharged at $Preset_-$ and $Preset_+$, creates undesirable instantaneous currents, which can distort the current integration during Φ_1. Moreover, the OTA's offset currents, when its inputs are shorted, can add offset to the charge being sampled during Φ_1. To prevent these effects, the offset cancellation (OC) circuit in Fig. 5 is used.

During Φ_0, the OTA inputs are shorted to the common mode voltage, V_{CM}, and as a result, the OTA current outputs during this phase are its offset current. The OC circuit adds I_{PULL1} and I_{PULL2} to the OTA output pull currents, I_{PULL+} and I_{PULL-} in Fig. 4, and I_{PUSH3} and I_{PUSH4} to the OTA output push currents, I_{PUSH+} and I_{PUSH-}. The resulting currents are connected during Φ_0 to a pair of dummy capacitors, C_5 and C_6, which voltages are compared via a feedback loop to $Preset_+$ and $Preset_-$, respectively, and the resulting error voltages, V_{C1} and V_{C2}, are used to calibrate I_{PUSH3} and I_{PUSH4} until I_{OUT-} and I_{OUT+} node voltages becomes equal to $Preset_+$ and $Preset_-$, respectively, before the end of Φ_0. At the same time the two feedback voltages are sampled in C_3, and C_4 and maintained during Φ_1 such that the OC currents keep cancelling the OTA output currents while charging C_{C+} and C_{C-}. The OC feedback loop is turned on only during Φ_0 to save power.

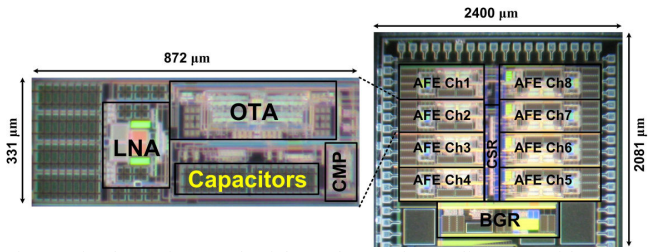

Fig. 6. Die photomicrograph of the 8-ch neural recording SoC with DSCS-AFE, implemented in the TSMC 0.35-µm CMOS (size: 2.4 × 2.1 mm^2).

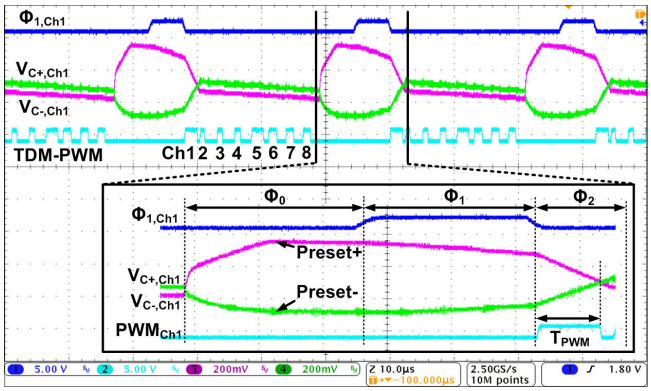

Fig. 7. DSCS-AFE measured waveforms at 250 ksps from 8 channels.

IV. Measurement Results

An 8-ch prototype ASIC was fabricated in the TSMC 0.35-µm 4-metal 2-poly CMOS process. Fig. 6 shows the chip micrograph and floor planning, which occupies 2.4 × 2.1 mm^2, including the padframe. A single DSCS-based AFE channel in this implementation occupies 872 × 331 µm^2.

C_1 was 10 pF, C_2 was 100 fF, $C_{3,4}$ were 200 fF, $C_{5,6}$ were 400 fF, and $Cc+/-$ were 10 pF. The LNA specs were measured when the gain was set at 40 dB. The lower cut-off frequency was tunable from 288 Hz to 1 kHz by voltage-controlled pseudo resistors, and the higher cut-off frequency was ~10 kHz. The fully differential design of the LNA led to 65.5 dB power supply rejection ratio (PSRR) and 56.4 dB common mode rejection ratio (CMRR), with an input referred noise of 2.77 μV_{rms} in 288 Hz ~ 10 kHz. The g_m of the OTA was programmable from 7.43 µS to 52 µS in 8 steps. Discharge current was also programmable from 332 nA to 2.3 µA in 8 steps. Sampling frequency, f_S, for each channel was set to 31.25 kHz. Charging time, Φ_1, was adjustable in 6 steps from 2.7 µs to 15.0 µs by programming the S2P register.

Fig. 7 shows some of the key waveforms in the DSCS-AFE. $\Phi_{1,Ch1}$ is the charging clock signal for the 1st channel, and $V_{C+,Ch1}$ and $V_{C-,Ch1}$ are the differential output voltages of the charge sampling capacitors of that channel. The bottom trace

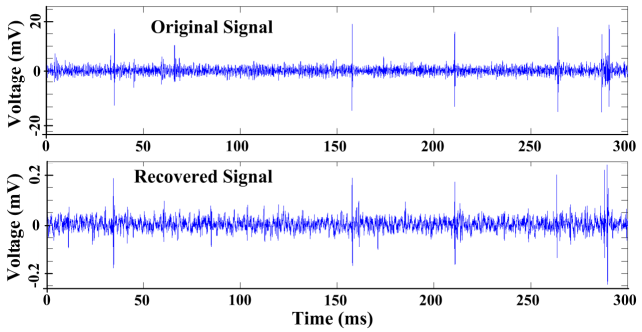

Fig. 8. The original and recovered pre-recorded spike signals, sampled at 31.25 kHz.

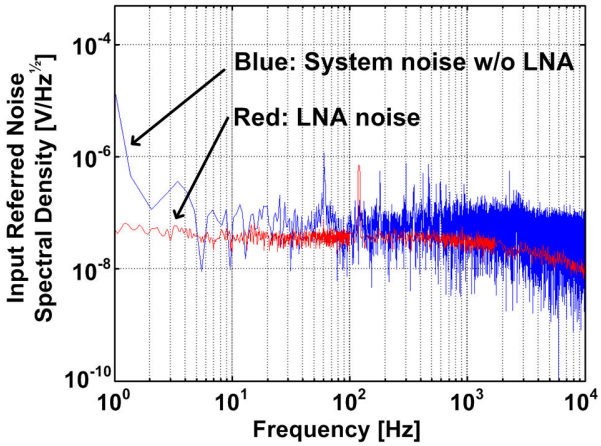

Fig. 9. Input referred noise of the LNA and the entire system without LNA.

is the TDM-PWM output signal, combining PWM signals from all 8 channels. The three phases of the DSCS operation are clearly presented in the enlarged segment. During Φ_0, $V_{C-,Ch1}$ and $V_{C+,Ch1}$ are precharged to $Preset_+$ and $Preset_-$, respectively. They are then differentially charged, during Φ_1, with the offset-calibrated OTA output currents, which are proportional to the differential input signal. During Φ_2, the capacitors are discharged by the programmable current sources, while their voltages are compared. PWM_{Ch1} asserts at the beginning of Φ_2, and goes low when $V_{C+,Ch1} \geq V_{C-,Ch1}$. As such, the pulse width, T_{PWM}, is proportional to the input signal. Table I benchmarks specifications of the new WINeR-6.5 system, with DSCS-based AFE, against other recent work.

Basic functionality of the entire system was verified by playing attenuated artificial spike waveforms. The original signal with ~40 mV_{p-p} amplitude was connected to the LNA through a 100:1 resistive attenuator. The resulting PWM signal from the DSCS-AFE was sent to an FPGA-based TDC for digitization. 16-bit digitized samples were buffered, packetized, and sent to a PC through its USB port as a serial data bit stream, which was then demultiplexed by the BCI2000 open-source software, displayed on the screen, and stored on the hard disk. Fig. 8 compares the original played neural signal with the recovered waveform in the BCI2000.

We measured the input referred noise of the DSCS-AFE by grounding the OTA inputs and conducting fast Fourier transform (FFT) on the recorded signal for 10 s. The resulting input referred noise spectral densities are shown in Fig. 9.

TABLE I
WINER-6.5 SPECIFICATIONS AND BENCHMARKING

Publication	This work	[2] 2012	[7] 2012	[8] 2014
Technology	0.35µm CMOS	0.13µm CMOS	65nm CMOS	0.5µm CMOS
V_{DD} (V)	1.8	1.2	0.5	1.5, 3
Die size (mm^2)	2.4 × 2.1	5 × 5	0.13	2.85 × 3.84
No. of channels	8	96	1	9
Total power (mW)	0.255	6.5	0.005	5
Power/ch. (µW)	31.8	68	5.04	55.68
Area/ch. (mm^2)	0.29	0.26	0.13	-
Sampling rate (kSps/ch)	31.25	31.25	20	200
LNA gain (dB)	40	-	> 32	39.35
LNA input ref. noise (μV_{rms})	2.77	2.2	4.9	4.58
LNA HPF (Hz)	288 to 1000	<1, 280	300	178 - 302
LNA LPF (kHz)	10	10	10	6.92 - 8.13
Resolution (bit)	-	10	8	-
System input ref. noise (μV_{rms})	6.50	-	-	4.58

Integration of these curves from 288 Hz to 10 kHz resulted in an input referred noise of 5.88 μV_{rms}. Including the LNA noise, the noise of the entire system became 6.5 μV_{rms}.

V. CONCLUSION

We have presented a new DSCS-based AFE architecture, which can be used in multi-channel wireless bio-signal recording systems. The DSCS architecture allows for low noise and low power amplification, filtering, and ATC with robust pseudo-digital PWM-TDM output, which does not need the sophisticated synchronization between Tx and Rx in systems with a large number of channels that utilize high speed ADCs in the Tx unit.

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