An Integrated Power, Area and Noise Efficient AFE for Large Scale Multichannel Neural Recording Systems

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Abstract— **A wideband, low-power, low-noise and area-efficient analog front-end (AFE) for acquiring neural signals is described. The AFE builds upon existing architectures but uses block-wise optimization to achieve superior performance when used in a multichannel system with scalable channel count. The AFE is also the first of its kind to enable acquisition from extended neural bandwidths greater than 10 kHz. The AFE is designed in 65 nm CMOS technology and consumes 11.3 μW of power while occupying 0.06 mm^2 per channel and delivering an NEF of 2.92.**

I. INTRODUCTION

Brain researchers use neural recording to obtain insight into brain function. Recent studies have shown that capturing, decoding and analyzing various types of brain signals provides crucial information for diagnosing and treating brain disease. By detecting patterns linked to the onset of seizures, external electronic devices can be activated to mitigate their damaging effects [1]. Furthermore, comparison between neural signals of healthy people vs. those with brain disorders such as Parkinson's or epilepsy provides insight into potential treatments.

However, brain researchers continue to demand less-invasive devices that can remain implanted over longer periods of time, while simultaneously capturing several channels of neural signals at high fidelity. These requirements present several challenges, especially relating to chip area and power consumption, which are directly correlated to invasiveness and the duration over which experiments can be carried out.

For continuous recording, the analog front-end (AFE) of the neural recording system is always active. Since the AFE directly interfaces with brain cells, it is critical to manage power consumption to avoid potential damage to neural tissue. Although there has been a significant amount of prior work that covers standalone area-efficient, low-power, high-fidelity front-end designs (e.g. [2], [3]), this work attempts to deduce AFE parameters based on system-level specifications such as sample rate, channel count, and compression.

Previous work at our research group, described in [4], concluded that the system power directly scales with, and is hence dominated by AFE power in high-channel-count systems.

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To save power, the AFEs used in [2] and [3] use one dedicated low noise amplifier per channel multiplexed into a single analog-to-digital converter (ADC). Unfortunately, multiplexing several channels onto a single ADC requires clocking it N times faster, thereby increasing ADC power proportionally. Clocking the ADC N times faster also reduces the available settling time of the S/H by 1/N. As sampling capacitors are sized to achieve desired signal to noise at the output, the on-resistance of the mux needs to be reduced proportionally to meet this settling time constraint. This leads to large switching transistors that need to be driven by fast clocking signals generated by digital logic, thereby eliminating potential advantages in power efficiency. Large switches also introduce clock feed-through and inter-channel crosstalk that impair signal fidelity.

II. SYSTEM ARCHITECTURE

The proposed architecture, as shown in Fig. 1 uses a dedicated neural amplifier, ADC, and digital filter for each channel. While this general architecture has been implemented in [5], the purpose of this work is to optimize each block toward minimizing AFE area and power impact with increasing channel count while alleviating the disadvantages and overhead associated with conventional approaches.

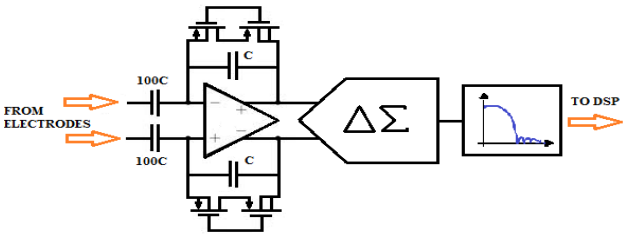

Fig 1. Analog Front End architecture

Each channel consists of a band-pass amplifier, a dedicated self-biased ∑Δ ADC, followed by a digital filter. The amplifier mid-band gain A_m is set to 100 by the ratio of capacitors 100C/C where C =150 fF chosen to minimize gain error. The high-pass cutoff frequency is nominally 0.8 Hz and set by the feedback capacitor and the pseudo-resistor of resistance R, or $f_{HPF} = (2\pi RC)^{-1}$. This design is the first of its kind to encompass extended neural bandwidths to account for neural signals up-modulated during emotional stress [6]. With no additional increase in power, the low-pass 3-dB frequency is extended to 18 kHz by the amplifier unity gain frequency ($f_{LPF} = f_u/A_m$). This extended bandwidth enables neuroscientists to capture a wider range of signals during periods of stress which is common during epileptic attacks.

The amplifier output is buffered, then digitized by a ∑Δ ADC with adjustable dynamic range to enable input signals

voltages ranging from tens of µVs to hundreds of mVs. The choice of the ∑Δ ADC was primarily motivated by its area efficiency coupled with the ease of achieving flexible resolution using a variable clock rate without the need for calibration circuitry.

The oversampling nature of the ∑Δ ADC necessitates a digital filter at its output to remove the out-of-band noise. A 10th order FIR filter was therefore implemented with the coefficients quantized to 5 bits optimizing for power and area efficiency. The output of this filter reads out in parallel and is acquired by a Xilinx FPGA for bench top characterization described later (Section III). We now examine each block in detail.

A. Amplifier

The purpose of the front-end amplifier is to reduce the impedance of incoming neural signals with amplitudes ranging from µVs to mVs at frequencies ranging from fractions of a Hz to kHz. Since each transistor is a noise source, a topology with minimum number of noise-contributing transistors was chosen. The telescopic cascode shown in Fig. 2 has only three effective noise contributing pairs M_i and $M7_{a,b}$ ($M7_{a,b}$ is cumulatively referred to as M7). The input devices were chosen to be PMOS for lower flicker noise.

$$Vn_{in,rms}^2 = \frac{4kT}{gm_i}\left(\frac{2gm7}{gm_i} + 2\right)\frac{V^2}{Hz} \quad (1)$$

From Equation 1, minimizing amplifier noise for a given bias current requires maximizing gm_i and minimizing gm_7. M_i is biased into weak inversion by trickling current (2.2uA) while making them very wide (440 µm/2.5 µm), thereby achieving a high transconductance-to-bias-current ratio. M7a and M7b on the other hand are operated in saturation for a low transconductance to current ratio. As a result, gm_i is a linear function of current while gm_7 is a square root function of current. For a tail current of 4.4 µA the thermal noise floor for the amplifier can be computed as:

$$gm_i = 28*2.2\text{ uA} = 62\text{ uS}. \quad (2)$$

$$gm_7 = K\sqrt{2.2\,uA} = 18.1\text{ uS}. \quad (3)$$

$$Vn_{in,rms}^2 = \frac{8kT}{gm_i}\left(\frac{gm7}{gm_i} + 1\right)\frac{V^2}{Hz} = 8.38 \times 10^{-16}\frac{V^2}{Hz} \quad (4)$$

$$Vn_{in,rms} = 2.9 \times 10^{-8}\frac{V}{\sqrt{Hz}} \quad (5)$$

Transistors M7a and M7b are long-channel to minimizing gm (which contributes to thermal noise) but also a need for large area (to reduce flicker noise). Transistors M3 and M5 are also operated in weak inversion to again maximize their gm in the interest of achieving high open loop gain.

The bias voltages for the amplifier are generated on-chip using a low-voltage cascade bias [7] operating in weak inversion. It draws 600 nA of current, and can be shared amongst many channels, thereby consuming negligible current on a per-channel basis.

A continuous-time common-mode feedback circuit [8] is used to handle large signal swings at its input by using a pair of complimentary source follower buffers. The amplifier output is put through a low-impedance buffer to prevent gain degradation while driving a switched capacitor ∑Δ ADC.

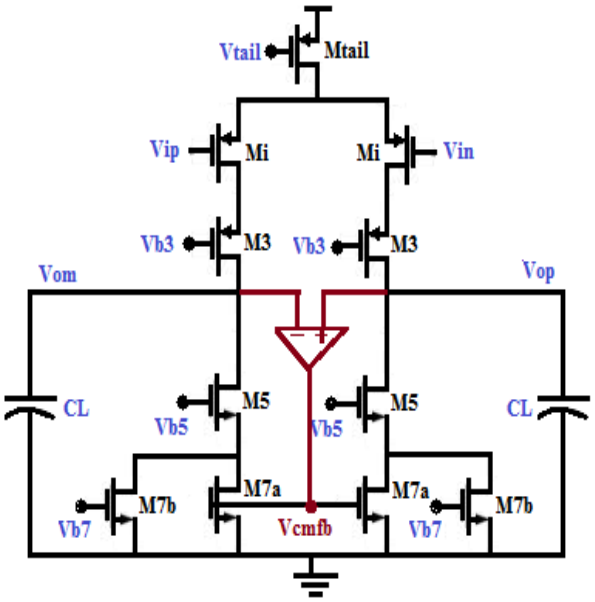

Fig 2. The main amplifier topology

B. Sigma Delta Analog to Digital Converter

The amplified signal is fed into a dedicated ∑Δ ADC for each channel. The 2nd-order ∑Δ ADC is implemented using the Boser-Wooley architecture [9]. To prevent the integrator outputs from saturating, outputs are scaled using a capacitor ratio before integration. Fig. 3 shows the model of the ∑Δ ADC along with its scaling coefficients b, b1, b2 and b3 which are 0.75, 0.125, 0.5 and 0.5, respectively in this design. The integrators are realized using self-biased super inverters as described in [10]. However, for higher clock rates the intrinsic CMFB of the super-inverter in [10] is not fast enough to enable common mode settling within half the required clock cycle. To address this, an auxiliary switched-capacitor CMFB circuit is added to the super inverter as shown in Fig. 4 which holds the output common mode constant over the entire sample and integrate cycle. The ADC operates under a 4-phase clock: 2 for sample, and 2 for integrate, which is generated by logic operating off of a 0.6 V supply for improved power efficiency.

C. Digital Filter

The ∑Δ ADC shapes the quantization noise in a high pass manner and contains out of band noise up to Fclk/2 at its output. Prior to processing in the digital domain, this noise is removed using an FIR low pass filter, whose cutoff frequency is set to 18 kHz in keeping with our band of interest. The maximum ripple tolerable in the pass band was aimed to be 1.5 dB, while attenuation in the stop band to be greater than 50 dB. A 10th-order, or 11 tap FIR filter designed using the Parks McLellan Algorithm meets these requirements with the filter coefficients quantized to 5 bits. The filter's circuit implementation is shown in Fig. 5. Each delay element is implemented with a D Flip-Flop clocked at the same ADC clock rate.

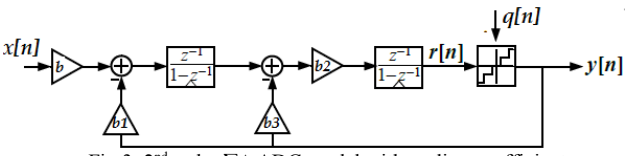

Fig 3. 2nd order ∑Δ ADC model with scaling coefficients

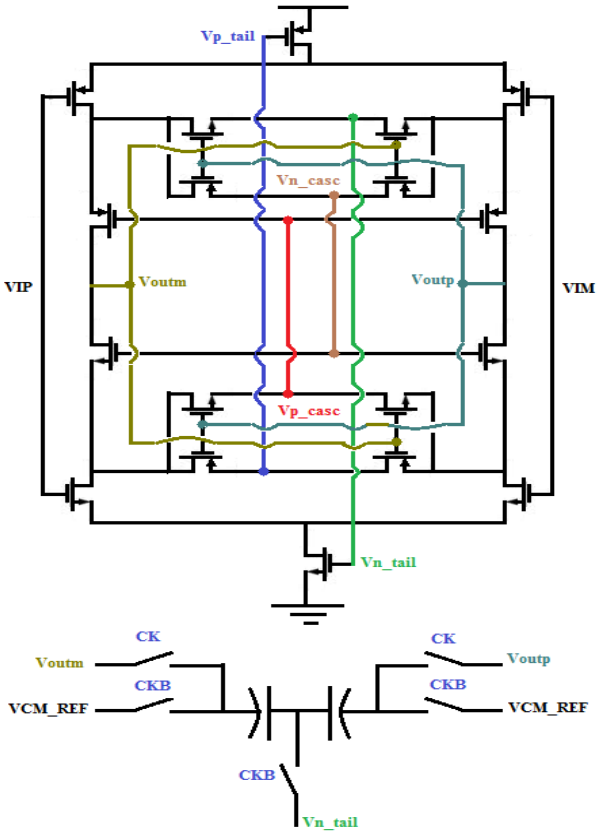

Fig 4. Super inverter with auxiliary switched cap CMFB

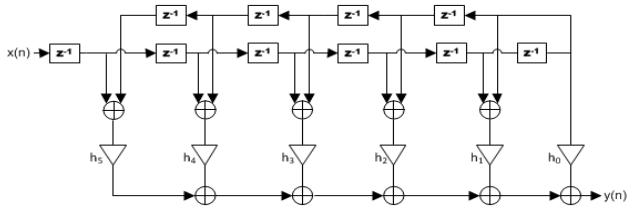

Fig 5. Digital Filter Transfer Circuit Implementation

III. BENCHTOP CHARACTERIZATION

The neural recording system was fabricated in a 65-nm CMOS process from ST Microelectronics. Designed to run from a 1.2-V supply, it occupies an area of 0.06 mm^2 and consumes 11.3 µW. Fig 6 shows a microphotograph of the AFE in the chip. Fig. 7 shows the measured frequency response of the amplifier with a mid-band gain of 39.8 dB, high-pass cutoff of 0.8 Hz and, low-pass cutoff of 18 kHz. Fig 8 shows the input referred noise spectrum of the amplifier which is dominated by flicker noise. The thermal noise floor is 3.1 x 10^{-8} V/√Hz, slightly higher than the value of 2.9 x 10^{-8} V/√Hz predicted by our earlier analysis in equation 5. Integrating this curve in our band of interest 0.8Hz to 18 kHz yields a total noise of 4.8µVrms. The amplifier, along with its CMFB and output buffer, draws 4.62 µA from a 1.2V supply leading to an NEF of 2.92 and thereby NEF^2 x VDD of 10.09. Fig 9 shows the power spectral density of the ADC output for an oversampling ratio of 100 (BW = 18 kHz, Fs = 3.6 MHz). The input to the AFE is a sine wave at 14.2 kHz with 2mV p-p. The ADC output has an SNDR of 55.6 dB corresponding to a 9-bit resolution. The ADC can offer anywhere from 6 bits clocked at 670 kHz to 9 bits clocked at 3.6 MHz. Table I shows the power and area contribution of different the blocks in the AFE. A 3-D plot comparing power, area and noise efficiency-power product for several recently-published neural AFEs is shown in Fig 10. A shorter stem closer to the origin indicates a better system (i.e low power, low area & low NEF^2 * VDD) and as noticeable, our AFE compares favorably in all 3 aspects.

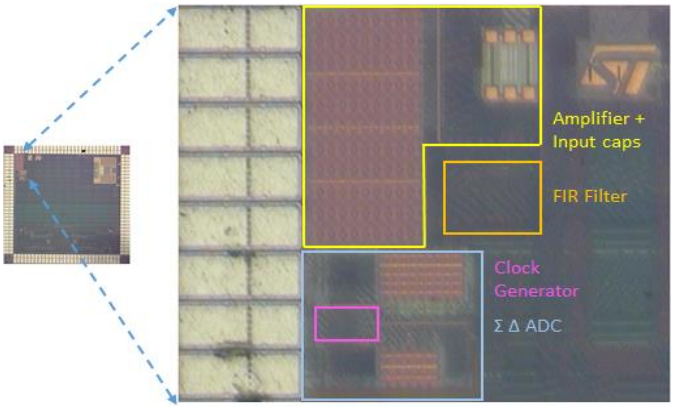

Fig 6. Microphotograph of the chip.

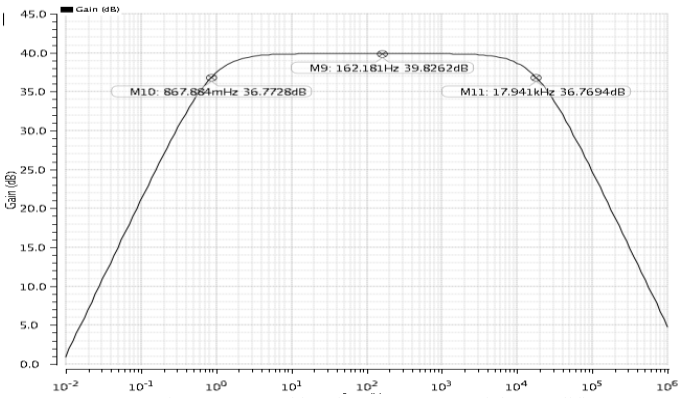

Fig 7. Measured band-pass response of the amplifier

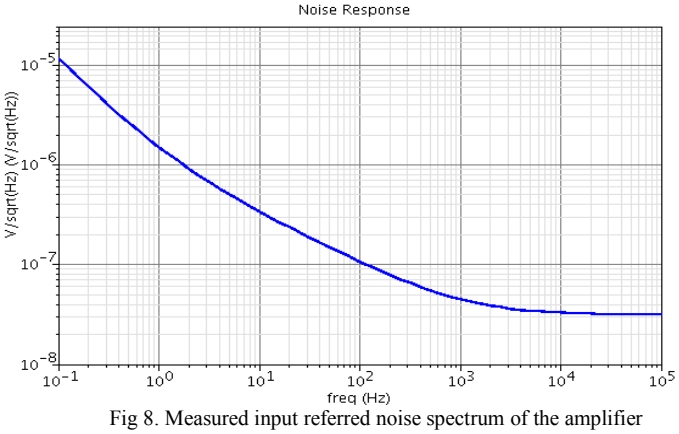

Fig 8. Measured input referred noise spectrum of the amplifier

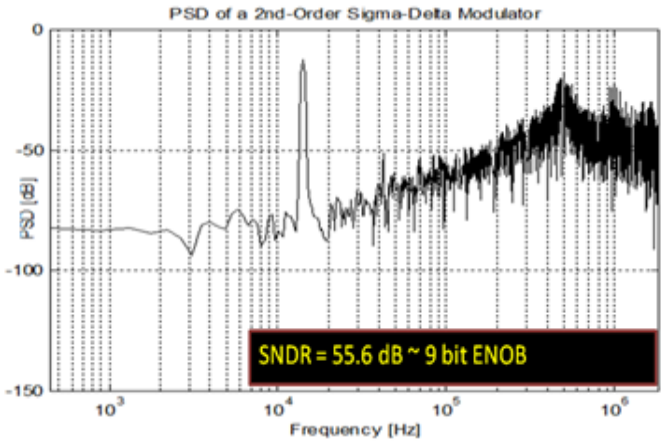

Fig 9. Measured SNDR of the ADC output clocked at 3.6MHz

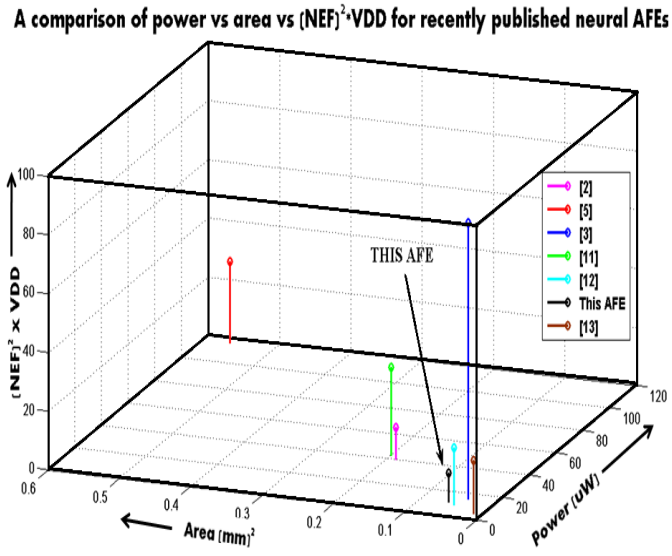

Fig 10. Comparison of this AFE with contemporary designs

IV. CONCLUSION

Managing the per-channel power and area of the AFE leads to truly scalable multichannel neural recording systems. As shown in Fig 11, adopting this AFE in the system proposed in [4] drops power to levels (indicated with "*") that could significantly increase channel count without adding to overall system power consumption.

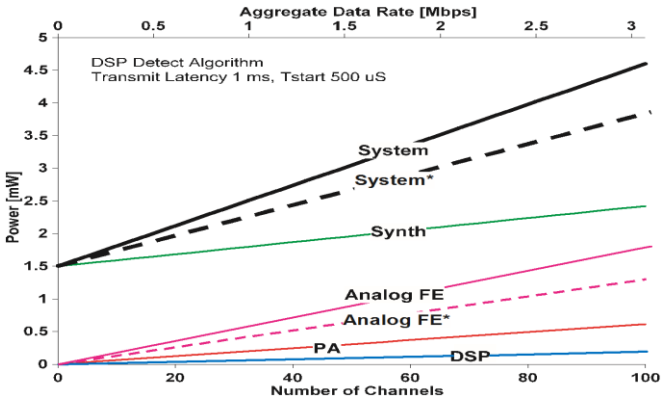

Fig 11. System power consumption vs. channel count – "*" indicates use of the described AFE

TABLE I. BLOCKWISE POWER AND AREA BREAK UP OF THE AFE

BLOCK	Current (uA)	Area (mm^2)
Amplifier		
Main cascode	4.4	
CMFB	0.12	
Output Buffer	0.1	
Total Amplfier	4.62	0.038
Delta Sigma ADC		
Super-inverters	1.55 (x2)	
Pre-amp + Comparator	0.9	
Total ADC	4	0.015
Digital FIR Filter		
Total Filter	0.8	0.004
TOTAL AFE	**9.4**	**0.06**

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