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Design Considerations for a CMOS Lab-on-Chip Microheater Array to Facilitate the *in vitro* Thermal Stimulation of Neurons*

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Abstract—**This paper identifies and addresses key design considerations and trade-offs in the implementation of a high-resolution microheater array for CMOS Lab-on-Chip (LOC) applications. Specifically, this is investigated in the context of facilitating the *in vitro* thermal stimulation of single neurons. The paper analyses the electro-thermal response (by means of COMSOL simulations) and reliability issues (such as melting and electromigration) of different microheater designs. The analysis shows that a small-area heater is more efficient in terms of power, but it has more reliability problems essentially due to electromigration effects. For the proposed heater designs, the expected lifetime is a few days (in continuous operation) in the worst scenario, which is still generally acceptable for LOC applications.**

I. INTRODUCTION

Many recent advances in biomedical research, in addition to emerging applications in point-of-care diagnostics, have been enabled through new capabilities provided by LOC platforms. These allow the monitoring and manipulation of biochemical assays at the micro-scale by integrating microdevices into a single chip [1]. Different types of microactuators (e.g. magnetic [2] and dielectrophoretic [3]) and microsensors (e.g. chemical, optical [4], and capacitive [1, 5]) have been recently integrated into LOCs to stimulate and detect populations of living cells. Furthermore, the trend is now shifting towards using commercially available CMOS technologies to implement on-chip sensors and actuators [6] avoiding costly custom processes. In addition to reducing cost, this enables the monolithic integration with electronics, which is crucial for multi-channel systems/arrays.

Temperature is a dominant factor (at both the macro- and micro-scale) in many biological activities and chemical reactions (e.g. protein characterization [7] and cell culture [8]). Furthermore, a controlled temperature change can be used as a stimulus itself, for example:

(i) Polymerase chain reaction (PCR): temperature changes from 50ºC to 98ºC are applied to amplify fragments of DNA molecules by enzymatic reactions.
(ii) Thermal stimulation of neurons: it has been shown that a local increase of temperature (of about 15ºC) over a short duration can be used to block the generation and/or propagation of action potentials between neurons [9].
(iii) Killing cancer cells: a local increase of temperature (of about 4.5ºC) over an extended duration can be used to kill cancer cells localized in the heated area [10].

In all the previous examples, a key requirement is that the temperature must be controlled to guarantee a proper operation of the bioassay. Moreover, in some cases (e.g. (ii) or (iii)), temperature must be controlled locally, i.e. at neuron or cell level.

A LOC intended for a temperature-controlled bioassay requires thermal sensors and actuators (i.e. heaters) to be embedded within. If temperature is to be controlled at neuron or cell level, then a high (spatial) resolution array of such sensors and actuators is required. To date, however, there has been no detailed analysis to implementing such an array in a standard CMOS technology. In [7, 8], the on-chip heater is implemented using polysilicon in a standard CMOS technology, generating heat by the Joule effect. However, there is just a single heater in [8], and a 3×3 array in [7]. In [11], the concept of a high-resolution heating array is proposed, but without reporting any details about how the local heating elements are implemented.

This paper aims to address the design considerations and trade-offs in implementing a high-resolution, thermally regulated array for a CMOS LOC. The analysis presented herein is towards the development of a CMOS LOC platform to facilitate the *in vitro* thermal stimulation of neurons, as introduced in [9]. Within the context of this application, this paper explores the feasibility of: (1) implementing an array of microheaters at the scale of single neurons; (2) maintaining a nominal temperature of 37ºC across the array; and (3) increasing instantaneously the temperature of a single neuron by up to 15ºC with a rapid decay back to the nominal level.

II. DESIGN OVERVIEW

The organization of an $M\times N$ array of thermally controllable pixels is shown in Fig. 1a. Within this design, each pixel contains: (1) a microheater and (2) a temperature sensor to control the temperature locally, and (3) an electrode to monitor the electrical activity of neurons in direct contact. Each pixel (and, therefore, each microheater) occupies an area $A_p=X_p\times Y_p$, where X_p and Y_p are the horizontal and vertical lengths of the pixel, respectively. Assuming that the dimensions of neurons range from tens to a few hundreds of microns [12] and that the temperature must be controlled at a single-neuron resolution, X_p and Y_p should be selected such that they are comparable to the neuron size.

The microheater topology to be integrated within each pixel is shown in Fig. 1b. This is based on a serpentine-shaped resistor implemented by one of the top metal (interconnect) layers in a standard CMOS technology. Such a resistive heater is biased using a current source I_h and dissipates heat by exploiting Joule effect. One of the key

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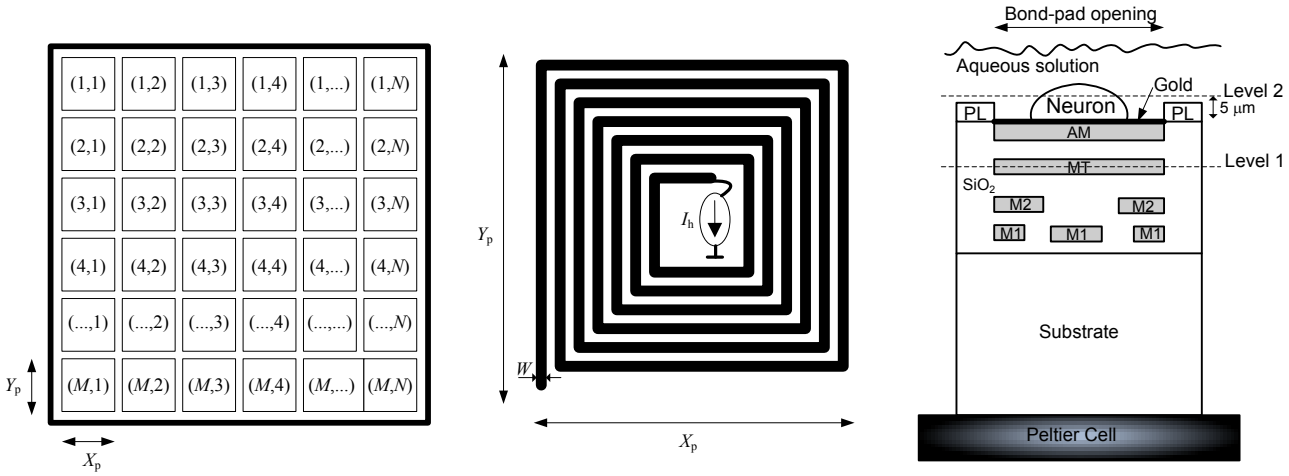

(a) (b) (c)

Fig. 1. (a) $M\times N$ array of pixels for the thermal stimulation of neurons. (b) Serpentine-shaped resistive heater to be integrated in each pixel. (c) Cross section (not to scale) of the pixel using CMOS technology (M1=Metal 1, M2=Metal 2, MT=Metal 3, AM=Analog Metal (4), PL=passivation layer).

design parameters of such a heater is the width (W) of the conductive track. For the same value of heater resistance, the thinner the W is, the smaller the A_p will be. However, a reduced W will result in an increased current density and, therefore, may impact reliability (i.e. heater lifetime due to melting and electromigration). This is discussed in Section IV.

The cross section of the proposed pixel is shown in Fig. 1c assuming the use of a commercially available 0.18μm 1P4M CMOS technology provided by IBM (7HV), which includes a thick "analog metal" (AM) top layer. The electrode to monitor the electrical neural activity is post processed by depositing gold on the top metal layer (AM in Fig. 1c); note that the passivation layers (PL in Fig. 1c) are removed in each pixel by means of a bond-pad opening [13]. The resistive heater in Fig. 1b is implemented using the aluminium metal 3 layer (shown as MT in Fig. 1c), with a thickness of 0.48μm. Part of the heat generated by the heater is conducted through the inter-metal dielectric layers (silicon dioxide, SiO_2) to the neuron located on the chip surface such as to facilitate the thermal stimulation. A thermal sensor (not shown in Fig. 1b) is additionally realized by exploiting the thermal coefficient of a metallic conductor. This is also implemented in the MT layer by interleaving with the heater resistance. Finally, the chip substrate is mounted on a Peltier cell to provide active cooling to the system and, therefore, to improve the dynamic (i.e. temporal) thermal response of the system.

III. Simulation Results

The electro-thermal response of the microheater topology shown in Figs. 1b and 1c has been simulated in 3D using the heat-transfer module in COMSOL Multiphysics 4.2. Three heater designs have been considered: heater #1 with W=1μm, heater #2 with W=1.5μm, and heater #3 with W=2μm. The three heaters have been designed such as to ensure they have the same electrical resistance (of about 100Ω). To achieve this, the wider the W, the longer the heater track and, therefore, the larger the overall pixel area (A_p). The corresponding A_p is $50\times50\mu m^2$, $70\times70\mu m^2$ and $90\times90\mu m^2$ for heaters #1, #2, and #3, respectively. In all three cases, the size of the heaters (and, hence, of the pixels) are comparable to the size of the neurons, thus ensuring that the temperature of a single neuron can be controlled.

The COMSOL simulations also take into account two features (not represented in Fig. 1c) that increase the thermal coupling between the heater and the substrate and, therefore, dampens the heater response. Specifically, these features are: (i) the connection between the sensing electrode (in AM layer) and the readout transistor (in substrate), and (ii) the connection between the heater (in MT layer) and the current-source transistor (in substrate). Additionally, a boundary condition is set such that the bottom of the die is at a constant temperature of 27 ºC (which in reality will be set by the Peltier cell).

The simulation results illustrating the (steady-state) thermal profiles of the three heater designs are shown in Fig. 2 for I_h=30mA. Fig. 2a shows the thermal profile at the heater depth (annotated by "Level 1" in Fig. 1c), whereas Fig. 2b shows that at the target depth ("Level 2" in Fig. 1c). As can be observed in Fig. 2a, the temperature at the heater is about 80ºC, 60ºC, and 45ºC for heaters #1, #2, and #3, respectively. Although the same power (in this case, 90mW) is applied to all the three heater designs, the resulting temperature varies significantly. This is due to the fact that the self-heating caused by Joule effect is inversely proportional to the power-dissipating area. Consequently, the temperature at the target depth is higher in heater #1 (about 60ºC) than in heater #3 (about 40ºC), as shown in Fig. 2b. In all three cases, however, the spatial thermal distribution is quite uniform.

The relationship between the power applied and the resulting temperature at the target location (i.e. centre of the pixel at level 2) is shown in Fig. 3 for the three heater designs. As expected, the temperature increases with the power applied, but this increase is more significant when the power is dissipated over a small area (i.e. in heater #1). For the application of interest, an estimated power (current) of {22,34,48}mW ({15,18,22}mA) is required to maintain the target (i.e. neurons at the chip surface) at a nominal temperature of 37ºC for heaters #1, #2, and #3, respectively. On the other hand, an estimated power (current) of

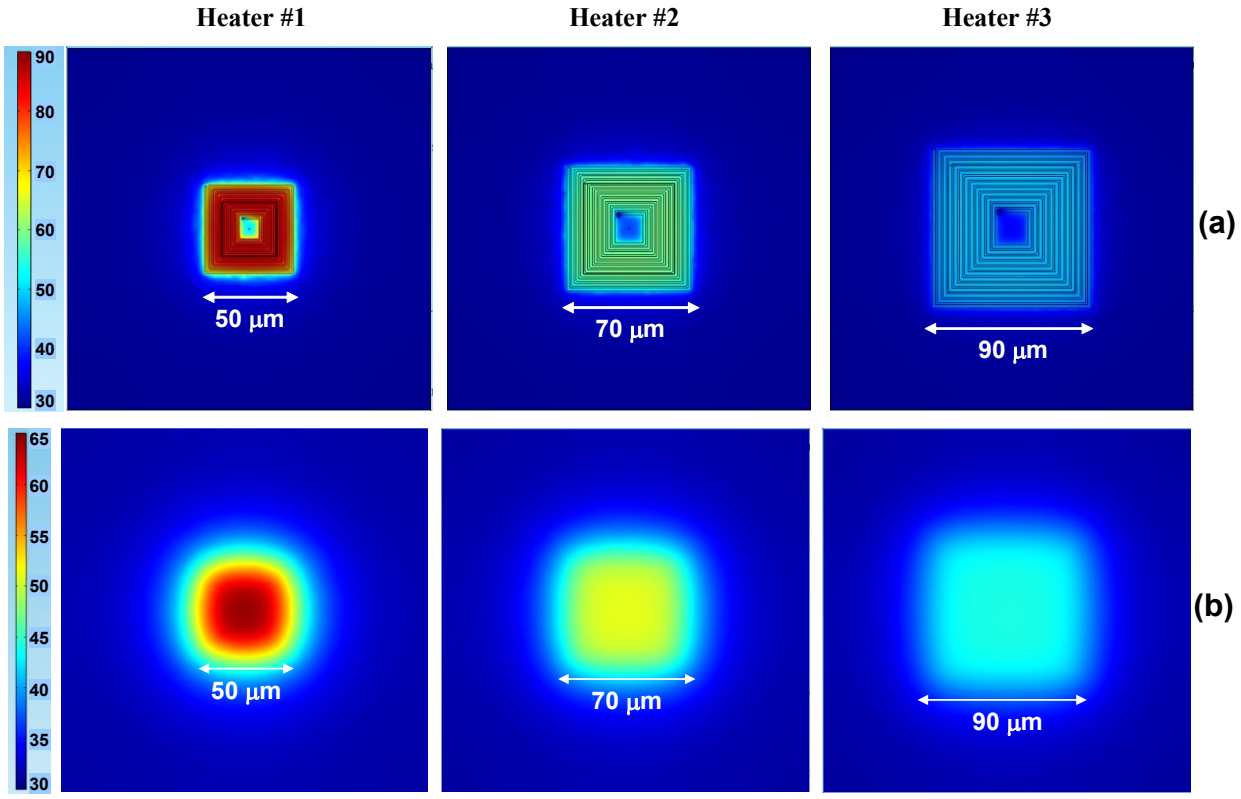

Fig. 2. (a) Thermal profile at the heater depth (level 1 in Fig. 1c) for the three heater designs. (b) Thermal profile at the target depth (level 2 in Fig. 1c) for the three heater designs. In all cases, $I_h = 30$ mA and, hence, the power dissipated by the heater is 90 mW.

{60,93,132}mW ({24,30,36}mA) is required to increase the target temperature by 15ºC (i.e. for thermal stimulation) for heaters #1, #2, and #3, respectively. Accordingly, heater #1 not only provides the opportunity to design a heater array with higher spatial resolution, but it is also a more power efficient solution.

IV. Reliability Analysis

Although the electro-thermal simulations in Section III show that a small-area heater (e.g. heater #1) is more power efficient, its reliability is uncertain since the current density along the metal track can be quite significant. Note that a current of tens of mA in a metal track of a few microns width and a thickness of 0.48μm can generate a current density of the order of MA/cm^2, which can cause both short- and mid-term reliability problems.

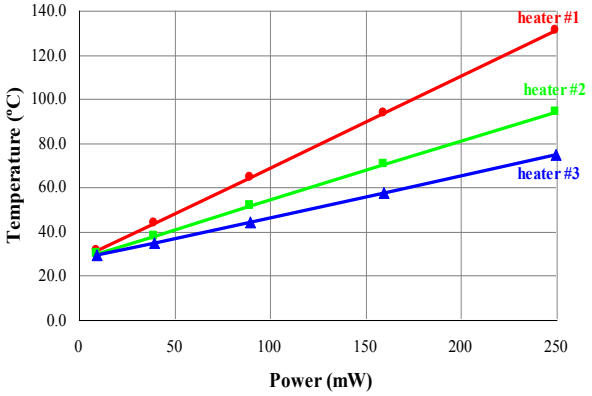

Fig. 3. Temperature at the target depth (level 2 in Fig. 1c) versus power applied for the three heater designs.

A. Short-term reliability

When the microheater proposed in Fig. 1b is driven by a high current to achieve a local temperature increase, the self-heating can be high enough to result in a sudden melting of the metal (i.e. aluminum). Assuming that most of the heat dissipates towards the substrate, the temperature of the metal due to the self-heating can be estimated by [14]:

$$T = T_{\text{ref}} + \Delta T_{\text{self}} = T_{\text{ref}} + J^2 \frac{t_{\text{m}} \cdot \rho_{\text{m}} \cdot t_{\text{ox}}}{k_{\text{ox}} \cdot s}, \qquad (1)$$

where T_{ref} is the reference substrate temperature, J is the current density, t_{m} and ρ_{m} are the thickness and resistivity of the metal track, respectively, t_{ox} and k_{ox} are the thickness and thermal conductivity of the underlying dielectric, respectively, and s is a heat spreading factor to take into account a quasi-2D heat conduction model [15]. From (1), the maximum current density to avoid the melting of aluminum is:

$$J_{\max} = \sqrt{\frac{(660 - T_{\text{ref}}) \cdot k_{\text{ox}} \cdot s}{t_{\text{m}} \cdot \rho_{\text{m}} \cdot t_{\text{ox}}}}. \qquad (2)$$

Table I summarizes, for each of the proposed heater designs, the value of $J_{\max}$ estimated by (2) and the resulting $I_{\max}$, assuming a bad scenario with T_{ref}=100ºC. Fortunately, $I_{\max}$ is about 3-4 times higher than the current I_h required to generate the local increase of temperature, as indicated in Section III. Therefore, although using a relatively low value

of W, the proposed heater designs are not expected to fail due to self-heating (i.e. melting).

B. Mid-term reliability

The mid-term reliability of the proposed microheaters is determined by the electromigration effect, i.e. the migration of metal atoms due to the stress generated by the high current density [16]. A continuous migration of atoms can cause, after a certain period of time, open or short circuits in the metal tracks and, therefore, a failure of the chip. The median time to failure (MTF) of a metal track due to electromigration effects can be estimated in hours using Black's Law [16]:

$$\mathrm{MTF} = \frac{1}{A \cdot J^2} e^{\frac{E_a}{k \cdot T}}, \qquad (3)$$

where A is an empirically-determined constant, J is the current density in A/cm^2, E_a is the activation energy in eV, k is the Boltzmann's constant, and T is the temperature of the metal track in Kelvin degrees. According to (3), MTF clearly decreases with J and T.

Table II summarizes, for each of the proposed heater designs, the value of MTF estimated by (3) considering A=5·10^{-6} [16] and E_a=0.7eV [17]; I_h (and, hence, J) is assumed to be the current required in normal operating conditions to maintain the target at 37ºC. Assuming T=313K (=40ºC) (which is the expected temperature of the heater in normal operating conditions according to simulations), the MTF is about a few hundreds of days; heater #3 shows a better MTF since it has a lower current density. Assuming a much worse scenario with T=373K (=100ºC), the MTF significantly decreases to a few days (in continuous operation). Although the values of MTF shown in Table II are relatively low (in particular, those for 100ºC), these can still be considered acceptable for LOC applications since the chip is typically disposable. Note that a microheater with a very long MTF (say, 10 years) would require a much wider W (say, tens of microns) and, therefore, a very long track and a large A_p that would make it unfeasible for achieving micro-scale spatial resolutions.

TABLE I. MELTING EFFECTS ON THE HEATER DESIGNS

	Heater #1	**Heater #2**	**Heater #3**
J_{max} (MA/cm^2)	17.7	16.3	15.6
I_{max} (mA)	85	117	150
I_h (mA) to stimulate	24	30	36

TABLE II. ELETROMIGRATION EFFECTS ON THE HEATER DESIGNS

	Heater #1	**Heater #2**	**Heater #3**
I_h (mA) to maintain	15	18	22
J (MA/cm^2)	3.1	2.6	2.3
MTF (days) at 40ºC	168	248	312
MTF (days) at 100ºC	2.5	3.8	4.7

V. CONCLUSION

This paper has presented the key design considerations in the implementation of a high-resolution microheater array, which is of interest for emerging applications in the biosciences that need micro-scale control of thermal profiles. To this end, we have conceptualized, designed and simulated arrays with microheater densities of 123, 204 and 400 elements per mm^2. We have compared the spatio-thermal response of these designs, shown the relationship between microheater size, power dissipation and thermal uniformity, and identified the trade-offs. We have also analyzed the issue of reliability and heater lifetime with respect to self-heating and electromigration. Finally, it has been shown that implementing such fine-pitch heating arrays in standard CMOS technologies is viable for future LOC applications.

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