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Clock Recovery PLL with Gated PFD for NRZ ON-OFF Modulated Signals in a Retinal Implant System

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***Abstract*— A Clock Recovery Phase Locked Loop with Gated Phase Frequency Detector (GPLL) for NRZ ON-OFF Modulated Signals with low data transmission rates for an inductively powered subretinal implant system is presented. Low data transmission rate leads to a long absence of inductive powering in the system when zeros are transmitted. Consequently there is no possibility to extract any clock in these pauses, thus the digital circuitry can not work any more. Compared to a commonly used PLL for clock extraction, no certain amount of data transitions is needed. This is achieved by having two operating modes. In one mode the GPLL tracks the HF input signal. In the other, the GPLL is an adjustable oscillator oscillating at the last used frequency. The proposed GPLL is fabricated and measured using a 350 nm High Voltage CMOS technology.**

I. Introduction

Many biomedical implants like cochlear or retinal implants [1] are powered inductively. It is not reasonable to have a long surgery on the patient only to change an empty battery. Because the retina implant system is in a very critical area of the body it should be very small and have as much as possible of the components integrated on an ASIC. Therefore, to run the digital circuitry, an on-chip clock should be extracted from the inductively coupled high frequency signal on the ASIC. An external quartz oscillator should be avoided.

In this work inductive powering is used in combination with a data transmission protocol including a 100 % amplitude shift keying (ASK) scheme, the so called ON-OFF-keying (OOK). I.e. a digital one is transmitted if the HF signal is on and a digital zero is transmitted if the HF signal is off. Therefore no power is transmitted during a digital zero. This is acceptable because large off-chip capacitors, that are needed anyway to stabilize the voltage for high current output peaks, stabilize the rectified voltage. Low data rates with OOK have the disadvantage of possible long periods without HF power signal when many consecutive zeros are transmitted. Thus no clock can be extracted. In the proposed system, a 12 MHz inductive link is used for power transmission at a data rate of 19.2 kHz. Due to the data protocol at most four consecutive digital zeros may occur. For that reason, no clock can be extracted for up to $4 \cdot 1/19.2\,kHz = 208\,\mu s$ equaling 2500 clock cycles.

Several papers have been published regarding clock recovery with ASK [2] [3], but there a maximal 90 % ASK scheme is applied and therewith the HF signal is never completely off. The critical part concerning missing pulses in the data transmission and clock absence is the Phase Frequency Detector of the PLL. For example the classical Hogge PD [4] can handle missing pulses. But the Hogge-PD can not detect frequency differences. Therefore there is consequently the disadvantage of a false lock. Either the Hogge-PD must be extended by a frequency detection circuit or a real PFD has to be used to avoid false lock [5]. This PFD is only useful in applications with continuous pulses like frequency synthesizers or with fewer missing pulses because it produces false pulses on its output. As mentioned, state of the art PFDs in Phase Locked Loops (PLL) have the disadvantage of tracking the input all the time. If the extracted clock frequency from the HF power signal is for a while zero due to the 100 % ASK scheme, the state of the art PLL will decrease its output to track the input. If the frequency of the extracted clock equals the data rate and only some pulses are missing, the loop filter can be adapted to avoid large frequency changes on the output [6]. This has the disadvantage of having a smaller lock range of the PLL [7]. In our case the difference between the frequency of the extracted clock and the data rate is too big to adapt the loop filter on the ASIC.

The presented Gated Phase Locked Loop (GPLL) avoids frequency changes and false pulses by stopping the PFD of the PLL if the input data is gone. It is capable of delivering the clock to the digital circuitry, even when the power HF signal is absent for a long time.

II. Architecture

The inductive link feeds a rectifier and positive and negative voltage regulators to generate the positive (VDD, +2 V) and the negative (VSS, -2 V) supply voltages of the chip. The HF signal is also connected to a clock extraction circuit

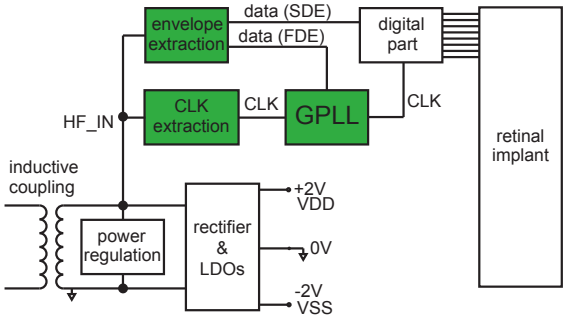

Fig. 1. Architecture of the System

to extract a 12 MHz clock out of the 12 MHz sinusoidal input signal. Because ON-OFF-keying is used, there is no sinusoidal signal during transmitting a digital zero and no clock can be recovered. The extracted clock is the input signal of the Gated Phase Locked Loop (GPLL) (Figure 2) to generate a constant output clock even when no HF signal is transmitted. To achieve this the GPLL has two operating modes.

In the first operating mode, the GPLL tracks the 12 MHz input clock and the feedback output follows the input to minimize phase and frequency difference to the input. Therefore the output of the voltage controlled oscillator (VCO) is fed back to the second input of the phase frequency detector (PFD) to generate a low pass filtered voltage on the input of the VCO dependent on the phase and frequency differences of feedback and input signals.

In the second operating mode, the GPLL works like an oscillator because no clock can be extracted if no HF signal is inductively transmitted during a digital zero transmission. The oscillation frequency has to be the last operating frequency of the voltage controlled oscillator (VCO). This is achieved by breaking the loop of the PLL and therewith stopping the PLL, until the HF signal is back again. The input of the VCO stays constant, so the VCO frequency does not change. The output frequency remains the same even if the extracted clock input signal is constantly zero.

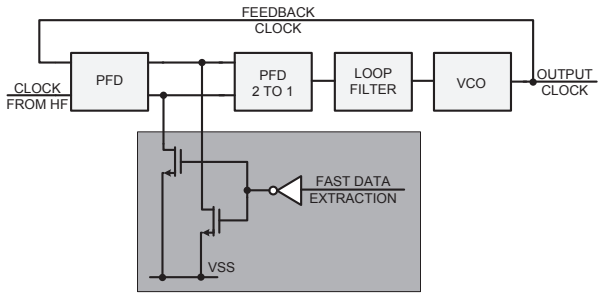

Fig. 2. Block diagram of the Gated Phase Locked Loop

III. Clock Extraction and Envelope Detection

The clock signal is extracted from the AC voltage on the secondary coil of the inductive link. Figure 3 shows how the clock is extracted by the use of two inverters. The first inverter uses special high voltage PMOS and NMOS transistors that can handle the high voltage range of the inductive link. The positive and negative peaks of the HF signal can be as high as $\pm 10\,V$. Both inverters are supplied by $\pm 2\,V$ because the GPLL has the same operating range. The extracted clock has a duty cycle of 50 %. Simulation results are shown in Figure 4.

The inductive link transfers not only power but also data by amplitude modulation as described in section II. The data extraction is done for the digital part through *slow data extraction* (SDE) and for the GPLL through *fast data extraction* (FDE). As the GPLL should be gated fast when the HF signal is gone, the extraction has to be fast too. Slow gating of the PLL would lead to a decrease of the output frequency. A short interruption of the HF signal does not affect GPLL operation, it retains a constant frequency at its output even if the HF signal is off for a period of time.

The envelope of the HF signal is extracted (Figure 5) with a diode to rectify the incoming HF AC signal together with the following capacitor. As there are only the two states one and zero, it is reasonable to use an inverter to detect the levels of the data transmission. To get the right polarization and steep edges the signal is inverted again between VDD and VSS. The data for the digital part has to be filtered so that a short interruption of the HF signal is not recognized as a zero. That means that the SDE signal has to be low pass filtered. This is done with two slow inverters and one capacitor. The resulting signal is level shifted to the supply levels VSS (-2 V) and GND (0 V) of the digital part which receives the transmitted data.

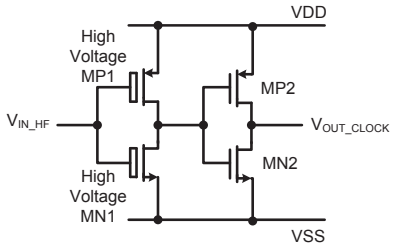

Fig. 3. Clock extraction circuit

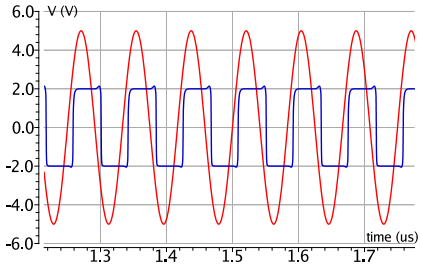

Fig. 4. Simulation results of clock extraction

IV. Phase Frequency Detector and loop filter

The applied type of Phase Frequency Detector (PFD) [8] is also called a ”sequential phase detector” (Figure 6). Its outputs depend on both the frequency and the phase of the inputs. The PFD consists of two parts. In the first part the two registers detect positive edges of the input signals *extracted_clock* and *feedback_clock* respectively. If an edge is detected the output of the registers goes high. If both outputs are high the registers are reset so both outputs become low. Now it has to be differentiated whether the rising edge of the *extracted_clock* leads the rising edge of the *feedback_clock* or the other way round.

If the rising edge of the *extracted_clock* leads the rising edge of the *feedback_clock*, the UP-signal is one in order to increase the input voltage of the loop filter. This in

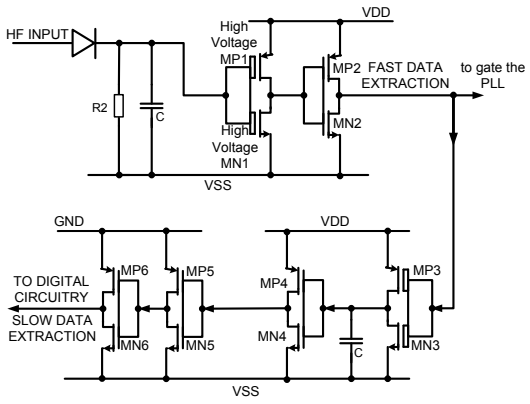

Fig. 5. Envelope Detection Circuit: FAST DATA EXTRACTION (-2V to 2V) to gate the PLL and low pass filtered SLOW DATA EXTRACTION (-2V to 0V) for digital circuit for receiving the transmitted data

turn increases the input of the Voltage Controlled Oscillator (VCO) to increase the output frequency to move the edges closer together.

Otherwise if the rising edge of the *feedback_clock* leads the one from the *extracted_clock*, the DOWN-signal will become high in order to decrease the input voltage of the loop filter and consequently the output frequency.

If the PFD is locked and frequency and phase of both input signals are the same the UP- and the DOWN-signals are zero. Both outputs of the registers of the first stage are combined to a tristate single output to drive the loop filter.

The loop filter determines how fast the PLL reacts to differences of the input signals [8]. Its principle can be seen in Figure 7. For fast variations the loop filter works like a resistive divider to track fast changes of the phases. If the changes are slow the loop filter works like an integrator averaging the outputs of the PFD.

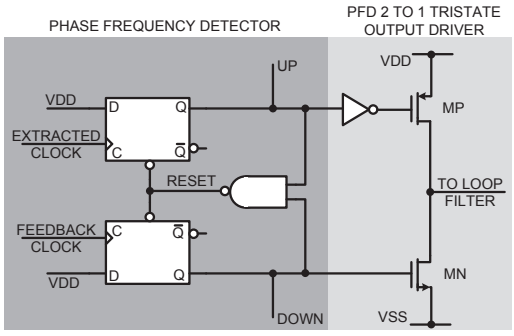

Fig. 6. Phase Frequency Detector and tristate output driver

V. Voltage Controlled Oscillator

The Voltage Controlled Oscillator (VCO) generates the output and feedback clock of the PLL (Figure 8). The output of the loop filter is connected to the wide gate NMOS transistor MN1 with the high ohmic resistor R at the source to linearize the current. This voltage dependent current is mirrored with the PMOS current mirror (MP1 and MP2)

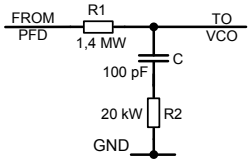

Fig. 7. Schematic of the loop filter

and charges the capacitor C from VSS (-2V) up to GND (0V). The voltage over the capacitor is monitored with a comparator. If the voltage reaches GND the output of the comparator goes high and opens the switch MN3 to quickly discharge C.

If the input voltage increases, the current increases and the capacitor is charged faster. If the input voltage decreases the current decreases and the capacitor is charged slower. This leads to an increase or decrease of the switching frequency of the comparator output. At every rising edge of this output, the following register toggles to generate a clock with a duty cycle of 50 %.

The VCO characteristic over the operating range is shown in Figure 9. The output frequency can vary linearly between 0 Hz at -1.4 V and around 19 MHz at +1 V. The aimed frequency is 12 MHz at an input voltage of 0 V. The level of 0 V is selected to have a fast startup when the input voltage is 0 V.

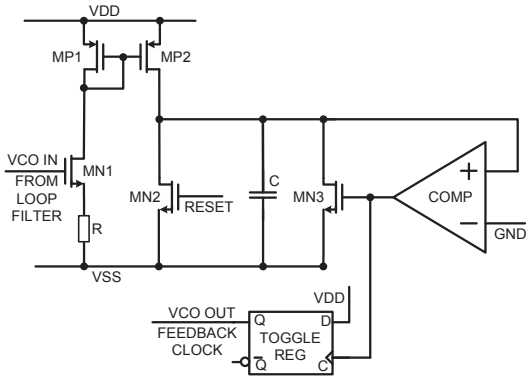

Fig. 8. Schematic of Voltage Controlled Oscillator

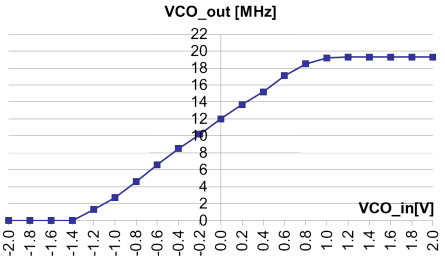

Fig. 9. VCO output frequency versus input control voltage

VI. Gated Phase Locked Loop

The implemented Gated Phase Locked Loop (GPLL) has two operating modes.

In the first mode the GPLL behaves like a typical PLL and the output clock follows the input data. The PFD compares phase and frequency of the feedback clock out of the VCO with the extracted clock out of the clock extraction circuit. The resulting clock can change between DC voltage up to a frequency of around 19 MHz. The upper frequency is limited by the maximum frequency of the VCO. In this operating mode the gray colored block in Figure 2 for stopping the PFD of the PLL is disabled.

In the second operating mode the GPLL imitates the locked state of the PLL. The PLL output stays constant because the PLL acts like when the inputs are equal in phase and frequency. The PLL is disabled by pulling the UP and DOWN output signals of the PFD to VSS. These signals lead normally to a charge or discharge of the input of the loop filter to increase or decrease the VCO input voltage. This increases or decreases normally the output of the VCO until the loop is locked and the output frequency stays constant. For pulling the UP and DOWN signals down the *fast data extraction* signal is used. If there is a zero transmitted, the *fast data extraction* signal is zero and the switches are closed to break the PLL loop. The output of the PFD output driver is in a tristate operating mode and the input of the loop filter stays constant. The GPLL works like an adjustable oscillator at the last used frequency. When the disable signal is active the output frequency stays constant for a long time.

VII. Measurement Results

The Gated PLL has been fabricated in 350 nm High Voltage CMOS technology. The microphotograph is shown in Figure 10. The GPLL is included in a complete receiver module system. Power and data are transferred over the inductive link. The GPLL works exactly as expected from the simulations.

In Figure 11 measurement results are shown. On the bottom (5) the input HF signal is illustrated. Before the inductive HF input signal (5) is turned of at $0\mu s$ the *fast data extraction* and *slow data extraction* (3, 4) are one. After the HF input goes to zero, after $1\mu s$ signal (4) goes to zero, too, to stop the PFD of the GPLL.

As the digital circuit needs a 4 MHz clock the 12 MHz clock of the GPLL (1) is divided and level shifted. The measured 4 MHz clock (2) drops from 4.0 MHz at not gated PLL operation to 3,85 MHz until the GPLL disables the loop at $1\mu s$.

Measurements have shown that this frequency stays constant for more than some minutes even if no input signal for synchronization is there.

VIII. Conclusion

A Gated Phase Locked Loop for clock recovery in an inductively powered retinal implant system with really low data rates in ON-OFF-keying is proposed. The GPLL can either work in normal operation mode to track the input frequency or as an oscillator at the last locked frequency.

The proposed system has been verified by simulations and fabricated in a 350 nm High Voltage CMOS process.

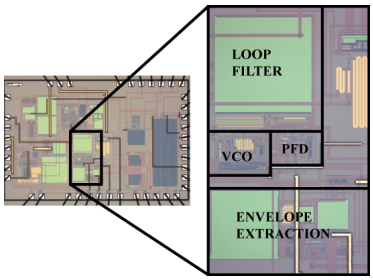

Fig. 10. Microphotograph of the Gated PLL. The size is 560 μm to 870 μm.

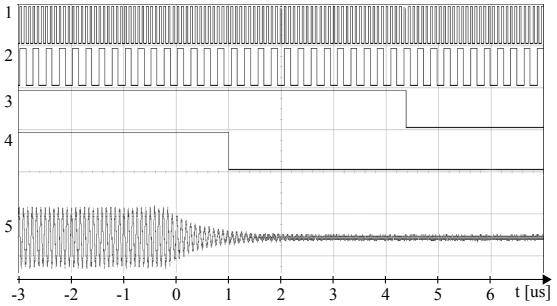

Fig. 11. Measurement results. Signal 1 is the measured 12MHz output frequency of the GPLL swinging between -2 and 2V. Signal 2 is the 12 MHz clock divided by 3 and level shifted to achieve a 4MHz clock for the digital part between -2 and 0V. Signals 3 and 4 is the slow and fast data extraction signal and signal 5 is the inductive input HF signal. The HF signal is turned off at $0\mu s$. The fast data extraction needs $1\mu s$ to change and therewith to gate the PLL. The frequency drops from 4 MHz to 3.85 MHz during that $1\mu s$. After gating the PLL the clock stays constant at 3.85 MHz.

Measurement results show that the proposed circuit can continue recovering the clock in the off state of an ON-OFF-keying modulated signal.

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