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An RFID Tag System-on-Chip with Wireless ECG Monitoring for Intelligent Healthcare Systems

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***Abstract*—This paper presents a low-power wireless ECG acquisition system-on-chip (SoC), including an RF front-end circuit, a power unit, an analog front-end circuit, and a digital circuitry. The proposed RF front-end circuit can provide the amplitude shift keying demodulation and distance to digital conversion to accurately receive the data from the reader. The received data will wake up the power unit to provide the required supply voltages of analog front-end (AFE) and digital circuitry. The AFE, including a pre-amplifier, an analog filter, a post-amplifier, and an analog-to-digital converter, is used for the ECG acquisition. Moreover, the EPC Class I Gen 2 UHF standard is employed in the digital circuitry for the handshaking of communication and the control of the system. The proposed SoC has been implemented in 0.18-µm standard CMOS process and the measured results reveal the communication is compatible to the RFID protocol. The average power consumption for the operating chip is 12 µW. Using a Sony PR44 battery to the supply power (605mAh@1.4V), the RFID tag SoC operates continuously for about 50,000 hours (>5 years), which is appropriate for wireless wearable ECG monitoring systems.**

I. Introduction

With the development of healthcare system in recent years, the demands of wireless bio-signal monitoring systems (WBSMSs) are increasing. In body sensor networks (BSNs), battery life is dominated by the power consumption of wireless communication circuits [1], especially in RF front end circuits. Moreover, the interference in the BSN results in the wrong information, which cannot be accepted by the requirements of WBSMSs. In this study, RFID systems [2] [3] with data correction are employed to fulfill the requirements of low-power WBSMSs.

The structure of this paper is as follows. Section II describes the proposed RFID tag system-on-chip (SoC) and the measurement results are shown in Section III. Finally, Section IV is the conclusion of the paper.

II. System Overview

Fig. 1 shows the proposed low-power SoC according to the EPC Class 1 Gen 2 UHF standard, including a RF front end circuit, a power unit, an analog front end (AFE), and a digital circuitry. The bio-signal processing and the system controller with error correction have been implemented in the AFE and the digital circuitry for the monitoring of wireless ECG signal. Moreover, the battery-assisted passive RFID structure and power management are also realized in the RF front end and the power unit for extending the battery life.

A. RF front-end circuits

The detailed RF front end circuits are shown in Fig. 2. Conventional amplitude shift keying (ASK) demodulation [4] requires at least two large resistors to implement the envelop detector and the low-pass filter. In this paper, the required resistor for the envelope detector is replaced with a current source combined with a capacitor array, and the RC low-pass filter is substituted with a mean value generator with a low V_{TH} diode and a capacitor. Therefore, an ASK without resistors is proposed to reduce the chip area. However, the time constant produced by the current source and the capacitor are dependent on the process–voltage–temperature (PVT) variation of MOSFET. Moreover, the distance between the reader and the tag will vary the internal output voltage of the charge pump, which will also result in an error in the demodulated data. Therefore, the calibration technique is employed in these circuits.

In the ASK demodulator, the duty cycle of the demodulated data is dominated by a time delay produced by the discharge path of the envelope detector. Equation (1) illustrates the derived formula for delay time, which is composed of discharged capacitance (C), discharging current (I_D), output voltage of charge pump (V_{cp4}), and output impedance (r_o). PVT variation mainly influences the discharging current and the output impedance. However, the output voltage of the charge pump varies with the distance between the reader and the tag. Detection of distance based on the output voltage of the charge pump can be employed to correct the time delay with programming the capacitor array.

$$\text{delay time} = r_o C \ln\left[\frac{V_{cp4} + I_D r_o}{V_{cp4} e^{-1} + I_D r_o}\right] \quad (1)$$

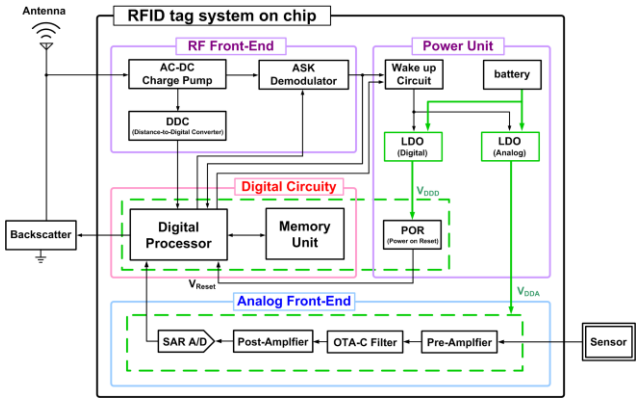

Fig. 1. Block diagram of RFID tag System-on-Chip

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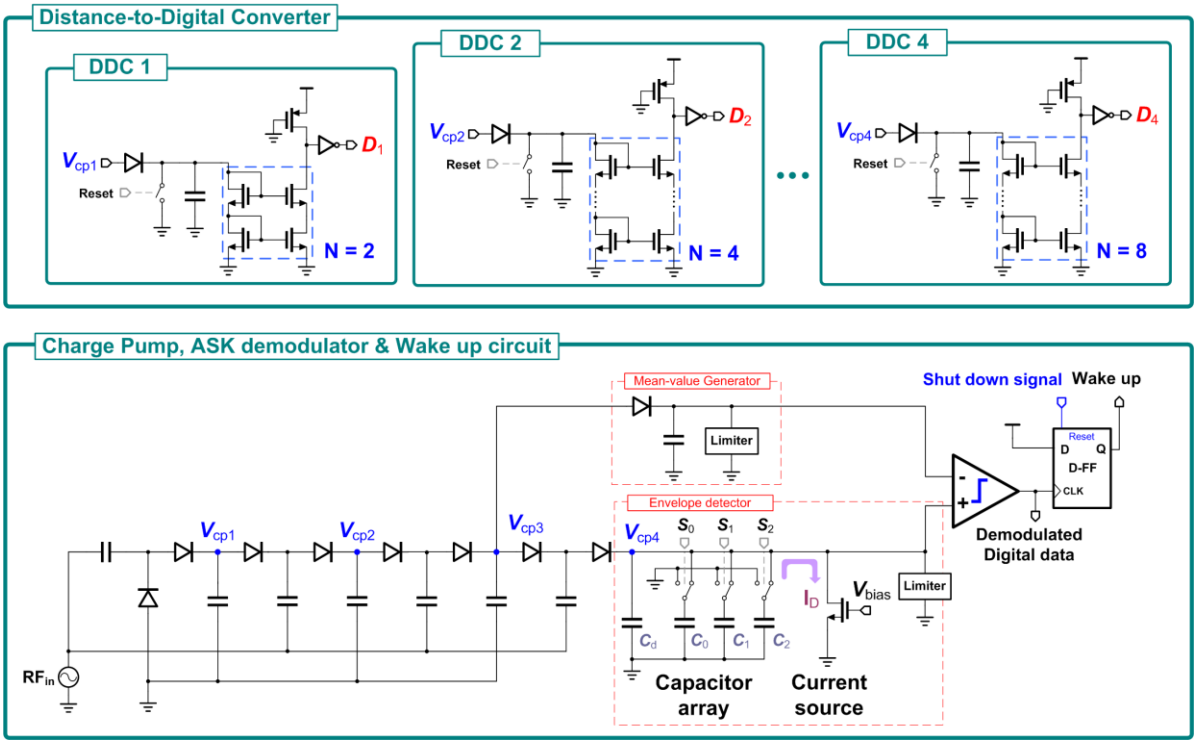


Fig. 2. RF front-end circuits with proposed ASK demodulation

A distance-to-digital converter (DDC), which is composed of multi-cascode ultra-low V_{th} native NMOSFETs and a PMOSFET load, is adopted to detect the internal output voltage of the charge pump (V_{cp1}–V_{cp4}). DDC is also a limiter, and it is used to detect the distance between the reader and the tag. Considering the output voltage of the charge pump achieves the transition point, the MOS diode is turned on and a saturation current is produced to limit the voltage at the MOS diode output. In the meantime, the DDC output is 1. If the output of one of the two DDCs is 1, the distance between the reader and the tag is closer than that of the DDC with an output of 1. The warning message caused by the variation in distance is transmitted to the digital processor to control the capacitor array of the envelop detector and to calibrate the delay time. The time delay should be maintained and fitted for the standard communication protocol (<2.5%). The proposed method features real-time correction, it detects the output voltage of the charge pump, and corrects the time constant once the tag receives the select command from the reader. This design will overcome the problem caused by the MOSFET PVT and the variations in communication distance.

A D flip-flop controlled by the demodulated digital data is employed as a wake-up circuit to enable and disable a low-dropout regulator (LDO) for power saving. When the LDO is enabled, the data in the digital processor is reset by a power-on-reset (POR) circuit and ready to receive the command from the reader. Otherwise, the system will be in sleep mode as the demodulated digital data are 0 for a long interval and then the LDO is disabled, which can save most of power if there is no request for ECG signal monitoring from the reader.

B. *Analog front-end circuits*

To separate the common mode voltage of the input signal and the AFE circuit, a difference differential amplifier (DDA) is popularly implemented in the preamplifier, which has a power consumption of 285nW and an input-referred noise of 5.587μV_{RMS}. A bandpass function with a bandwidth between 0.1Hz and 11kHz is also achieved with the feedback network using a pseudoresistor and capacitor.

A 5th order low-pass operational transconductance amplifier (OTA)-C filter with a bandwidth of 250Hz (Fig. 3) is implemented to reject the high-frequency interference from the body. Using the proposed OTA structure with a multiple output differential input technique reduces the number of OTAs from 11 to 6 [5], which saves 30% of the power consumption compared with that in a previous work [5].

A programmable gain post amplifier prior to the successive approximation analog-to-digital converter (SAADC) is developed with a gain of 20/30 times, respectively. The fully-differential SAR ADC with monotonic capacitor switching procedure [6] (Fig. 4) can reduce the input capacitance of charge distribution digital-to-analog converter (DAC) effectively. The measured ADC consumes 760nW to FOM of the 742fJ/conversion-step under an ENOB of 7.6 bits and a sampling rate of 2kHz.

C. *Digital Circuity*

Block diagram of digital circuitry and timing sequence of command (Query, RN16, Ack, and ID/Data) are shown in Fig. 5. The demodulated digital data from RF front end circuit is initially decoded by pulse interval encode (PIE). The decoded data are further processed by the CRC checker for the data correction and the command decoder for the control of protocol. The result triggers the FSM_Core to decide the operation for the next state, which becomes the feedback of RN16 and ID/Data according to the Query and the Ack commands, respectively. Moreover, the pseudorandom number generator (PRNG) provides random data with 16 bits

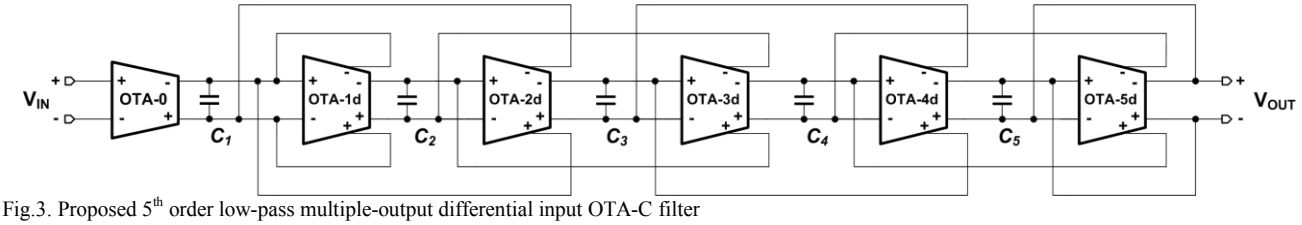
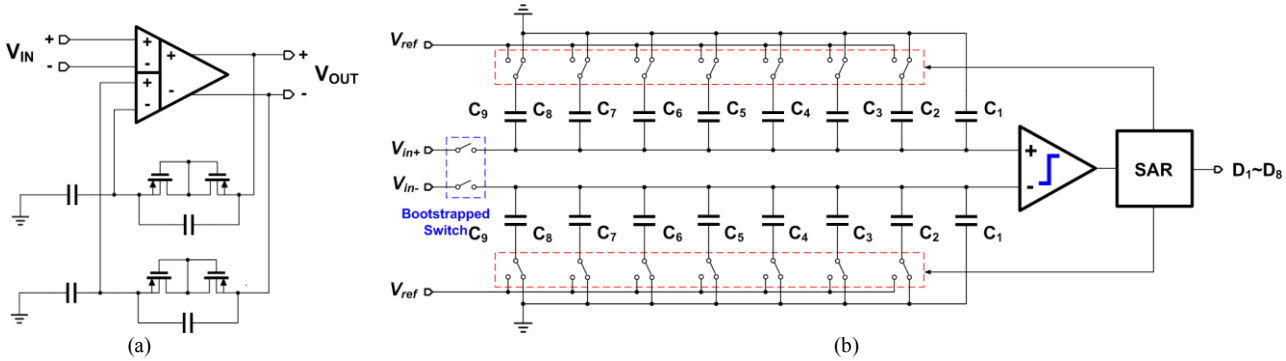


Fig.3. Proposed 5th order low-pass multiple-output differential input OTA-C filter



(a) (b)

Fig.4. (a) Preamplifier and (b) low power and low input capacitance SAR ADC

for handshaking between the tag and the reader, and the BLF clock divider gives the backscatter link clock to the FM0 encoder and FSM_Read. FSM_Read and FSM_Write are finite-state machines for reading and writing SRAM.

Considering the difference between the backscatter link frequency and the sampling rate of physiologic signal is huge, asynchronous control is preferred and implemented in the communication of the digital processor. For example, when the reader transmits the Query command to the tag, the FSM_Core waits for the FSM_Write response and the ECG data from the AFE is written into the SRAM_A memory. If the SRAM_A memory is full, the data is transmitted to the backscatter through the FSM_Read and the FM0 encoder. In the meantime, ECG data are continuously written into the SRAM_B memory until its capacity is full. The exchange between two memories protects the ECG data against loss and avoids the requirement of a large memory capacity to further reduce the power consumption and chip area. The digital processor consumes 3.2μW under the clock frequency of 2MHz, and the average power consumption of the SRAM with 400-bit bank is 2.15μW for writing and 4.83μW for reading, respectively.

III. Measure Result

Fig. 6 demonstrates the measurement result of Real-time ECG data transmission of RFID tag SoC. The design of battery-assisted system can make sure the stability of the chip which is used in medical domain. Channel 1 is the demodulated data at the comparator output of the RF front end, which is also the input of the digital processor, and is encoded by the PIE encoder. Channel 2 is the output of the digital processor, and the ID/Data are the ECG data encoded by the FM0 encoder. They are reconstructed as analog ECG signals by the reader and the off-chip DAC. The average power consumption for the working chip is 12μW. Under the sleep mode, the system-on-chip just leaves the passive RF circuits staying in ready status, and the power consumption for the chip in sleep mode is 900nW only.

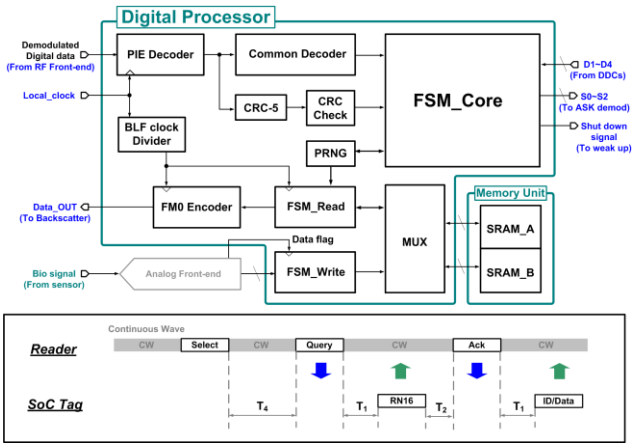


Fig. 5. Block diagram of digital circuitry and timing sequence of command

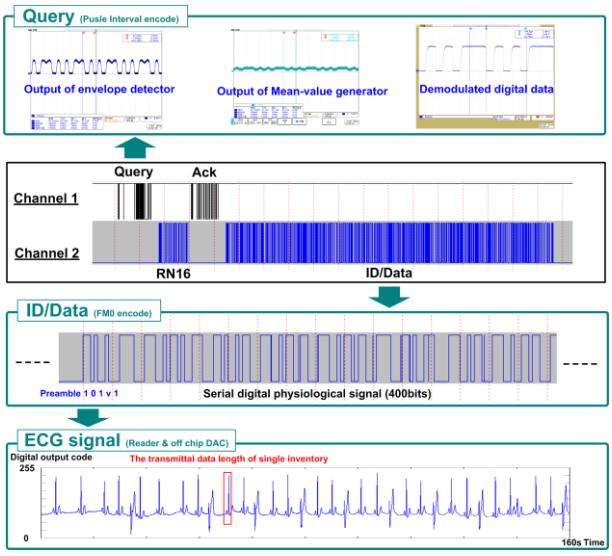


Fig. 6. The measurement result of real-time ECG data transmission of RFID tag

IV. CONCUSION

A low-power wireless communication SoC for ECG acquisition was presented in this paper. The detail performance and power consumption are illustrated in Table I. The proposed circuit was fabricated in a TSMC 0.18μm CMOS process with a core area of 2.25 mm^2 as shown in Fig. 7. Using the Sony PR44 battery to supply power (605mAh @1.4V), this RFID tag SoC can work continuity for more than 50,000 hours. Comparison with previous commercial products is also shown in Table II. The comparison reveals that the proposed SoC with the RFID technique has the lowest power consumption and the biggest breakthrough of this proposed SoC is the substantial extension of the battery life of the device.

TABLE I.
FEATURES AND MEASURED PERFORMANCES SUMMARY

Specification of RFID tag SoC	
Architecture	Battery-assisted passive tag
Protocol	EPC Class 1 Generation 2
Operational Frequency	925MHz
Reader maximum tansmit power (P_t)	27dBm
Reader antenna gain (G_T)	6dbi
Tag antenna gain (G_T)	0dbi
Data rate	100kB/s
Modulation	ASK
Local clock	2.15MHz
Distance	0.6m to 1m
Input signal range	0.2V to 0.8V
Battery	Sony PR44 (605mAh; 1.4V)
RF Front End & Power unit (1.4V)	
Duty cycle	1.6% (< 2.5%)
Capacitor	14pF
Charge pump size	257.55μm × 518.37μm
Power cosusmptions	2.8μW
Entire AFE circuit (1V)	
Bandwidth	0.1HZ to 250Hz
SNDR	44.1dB
Power consumption	1.9μW
Digital processor (0.7V)	
Power consumption	3.2μW(@2MHz)
SRAM (0.7V)	
6T cell area	3.4μm × 7.4μm
SRAM area	160μm × 400μm
Memory size	400bits × 2
Average Power consumption	3.8μW

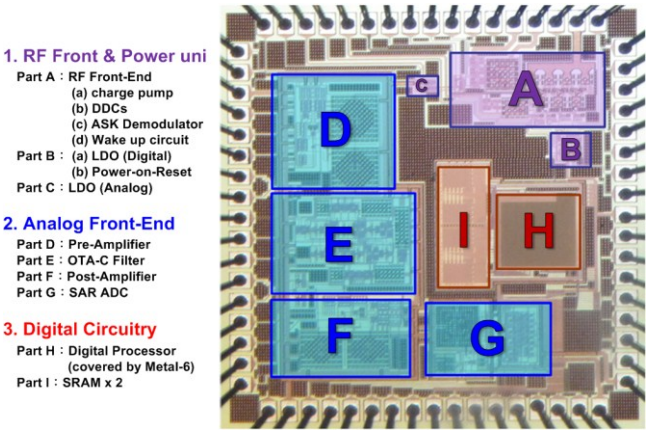


Fig. 7. Microphotograph of the proposed RFID tag System-on-Chip

TABLE II.
COMPARISON WITH PREVIOUS COMMERCIAL PRODUCTS

	IMEC	Zio®	This work
Product	NA	Zio® Patch	NA
Year	2012	2010	2012
Supply voltage	2.1V	NA	1.4V/1V/0.7V
Battery life	1 month	14days	>5 years (Sony PR44 with 605mAh@1.4V)

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REFERENCES

[1] M. Vidojkovic, X. Huang, P. Harpe, S. Rampu, C. Zhou, L. Huang, K. Imamura, B. Busze, F. Bouwens, M. Konijnenburg, J. Santana, A. Breeschoten, J. Huisken, G. Dolmans, and H. de Groot, "A 2.4GHz ULP OOK Single-Chip Transceiver for Healthcare Applications," in Proc. IEEE Int. Solid-State Circuits Conf., Feb. 2011, pp. 458-460.

[2] D. Yeager, F. Zhang, A. Zarrasvand, and B. P. Otis, "A 9.2μA gen 2 compatible UHF RFID sensing tag with −12dBm Sensitivity and 1.25μVrms input-referred noise floor," in Proc. IEEE Int. Solid-State Circuits Conf., Feb. 2010, pp. 52-53.

[3] H. Reinisch, M. Wiessflecker, S. Gruber, H. Unterassinger, G. Hofer, M. Klamminger, W. Pribyl, and G. Holweg, "A 7.9μW remotely powered addressed sensor node using EPC HF and UHF RFID technology with −10.3dBm sensitivity," in Proc. IEEE Int. Solid-State Circuits Conf., Feb. 2011, pp. 454-456.

[4] H. Zong, J. Shen, S. Liu, M. Jiang, Q. Ban, L. Tang, F. Meng, and Xin'an , "An Ultra Low Power ASK Demodulator for Passive UHF RFID Tag" Application-specific integrated circuit conferece, pp 637-640 , Oct.2011

[5] S. Y. Lee and C. J. Cheng "Systematic Design and Modeling of a OTA-C Filter for Portable ECG Detection," IEEE Trans. on Biomedical Circuits and Systems, vol. 3, no. 1, pp. 53-64, Feb. 2009.

[6] C.-C. Liu, S.-J. Chang, G.-Y. Huang and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a Monotonic Capacitor Switching Procedure,"IEEE J. Solid-State Circuits, vol 45, no. 4, pp. 731-740, Apr.2010.