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A MedRadio-Band Low-Energy-Per-Bit 4-Mbps CMOS OOK Receiver for Implantable Medical Devices

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***Abstract*—A 4-Mbps 400-MHz On-Off Keying (OOK) receiver implemented in 0.18-um CMOS technology for implantable epilepsy sense-and-stimulation devices is presented. The proposed receiver is composed of a new current-mode full-wave envelope detector and differential cascaded gain amplifiers which is operated at MedRadio band. The fabricated receiver has power consumption of 0.27 mW and energy consumption of 0.07 nJ per bit at 4-Mbps. The sensitivity of receiver is -45.67 dBm.**

I. Introduction

In 2010, the Federal Communications Commission (FCC) introduced the MedRadio [1] Service band in the range of 401-406 MHz which is a wireless communication regulation for biomedical telemetry. In many implantable devices like neural prosthetic devices, implantable wireless transceivers are required to transmit neural signals and receive control signals from a transceiver outside the body so that the physiological signals can be checked and diagnosed by medical doctors and suitable control signals can be sent to the implanted devices for adjustment.

The design considerations of implantable wireless receivers are low power consumption and high energy efficiency. This enables long-time operation and thus frequently replacement of battery by surgery can be avoided. Moreover, too much heat which increases temperature and causes possible tissue hurt can be avoided, too. Another requirement is small chip size and no external component except antenna is used. Thus the implantable transceiver can be miniaturized to reduce the device size for easy and comfortable implant.

On-Off Keying (OOK) modulation is one of the favorable methods for implantable transceiver due to its simplicity. An OOK receiver adopts an envelope detection architecture, which eliminates the need of local oscillator (LO) and down-conversion mixer for low power consumption and small chip size.

In the design of OOK receiver, envelope detector is a key element. Conventional envelope detectors [3][4] generate a small amplitude of the enveloped signal at the output of RC low-pass filter. Therefore, a baseband amplifier following the output of envelope detector is required to amplify the amplitude of the enveloped signal. The amplifier can be implemented by using sequential gain architecture [3] or two-stage operational amplifier [4]. In another design of half-wave envelope detector [5] proposed by present authors, the received voltage signals from amplifiers are converted to current signals to charge the RC low-pass-filter and achieve the envelop detection.

In this paper, a CMOS wireless OOK receiver in 0.18-μm technology for implantable epilepsy treatment devices is proposed. The receiver is designed in the FCC MedRadio Service band (401-406 MHz) which the maximum equivalent isotropically radiated power (EIRP) is limited to -16 dBm. In the proposed receiver, a new current-mode full-wave envelope detector (demodulator) composed of a full-wave current rectifier and a low-pass RC filter is used to increase the envelope detection efficiency and obtain a large output enveloped signal. Thus extra baseband amplifier is not required to reduce circuit complexity and power dissipation. Moreover, a differential cascaded gain amplifier is adopted. From the measurement results, the fabricated receiver has the lowest energy per bit at a higher data rate of 4 Mbps as compared with other receivers [2]-[6]. Note that the achieved data rate is higher than the regular bandwidth of 300 KHz. The proposed receiver chip has been integrated into a closed-loop epileptic seizure detection and stimulation SOC and animal test has been successfully performed.

II. Receiver Architecture and Circuit

The architecture of the implantable transceiver is shown in Fig. 1. The differential cascaded gain amplifiers with constant current sources are designed in the OOK receiver to minimize the power consumption and chip size. The new full-wave envelope detector architecture is used to decrease the circuit complexity and power consumption.

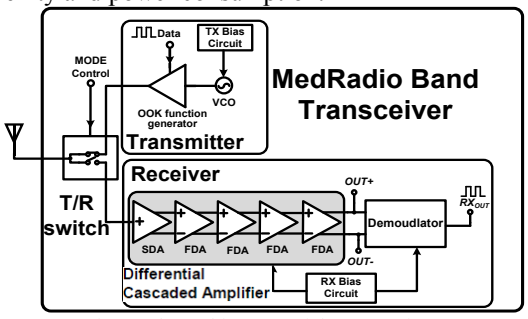

Fig. 1. The architecture of the transceiver.

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A. *Differential Cascaded Gain Amplifier*

The schematic of the proposed differential cascaded gain amplifier is shown in Fig. 2. It is used to provide sufficient gain for the signal received from antenna. The amplifier is controlled by a constant current for lower power dissipation. Each amplifier is designed with smaller gain to increase the amplifier bandwidth. To trade-off the gain stages and power consumption, the 5-stage differential cascaded gain amplifiers is designed, which provide voltage gain of 77 dB and power consumption of 0.57 mW.

The simple amplifier A_1 which is composed of a common source (CS) amplifier and a common gate (CG) amplifier is used to convert received single-ended signals from the antenna into differential signals. Then the differential signals are amplified by other 4-stage fully differential amplifiers A_2-A_5.

In Figs. 2(b) and 2(c), the PMOS active loads (M_3-M_4, M_{15}-M_{16}) with resistors (R_4-R_7) and the bypass capacitors (C_3-C_4) are employed to increase the gain in the high-frequency range. Furthermore, the DC offset problems should be noticed. The DC offset is mainly due to the unbalanced input from the preceding stages and the device mismatches in the amplifiers themselves. Therefore, the capacitor (C_5) is used to memorize and eliminate the offset of each amplifier so that it is not amplified by the next stage.

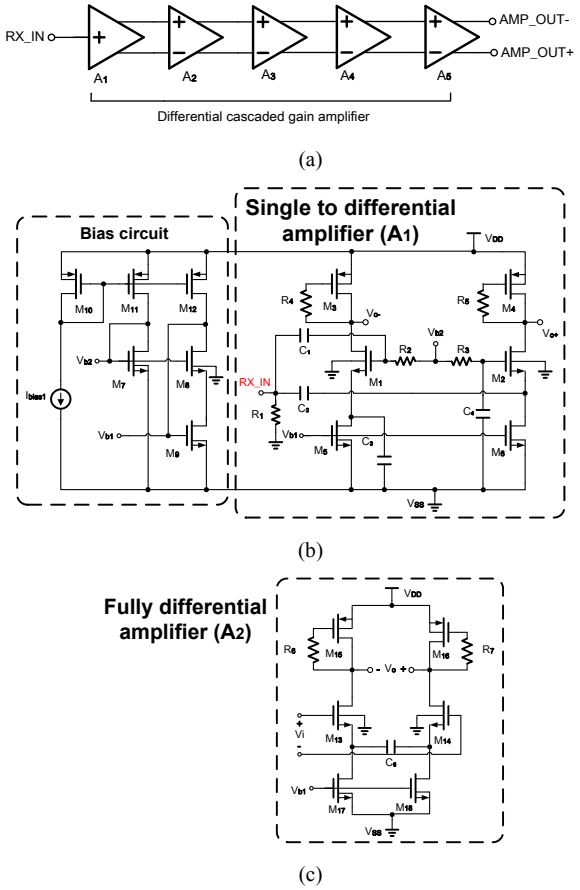

Fig. 2. (a) Schematic of the 5-stage cascaded gain amplifier, (b) circuit of the single to differential amplifier (A1) and bias circuits, and (c) circuit of the fully differential amplifier (A2).

B. *Current-mode Full-wave Envelop Detector (Demodulator)*

One of the key advantages of the proposed receiver architecture is that by employing a 403-MHz envelope detector right after the cascaded gain amplifier, no LO and down-conversion mixer are required to minimize the power consumption. The circuit of the proposed new current-mode full-wave envelope detector is shown in Fig. 3 where the output of the detector is connected to a Schmitt trigger and an output buffer. The received sinusoid voltage signals from AMP_OUT+ and AMP_OUT- are converted to a current signal to charge the RC low-pass-filter (LPF) $R_{10}C_8$ and form a positive level waveform.

When the transmitted data is high, the differential sinusoidal voltage signals AMP_OUT+ and AMP_OUT+ from the differential cascaded gain amplifier are fed into the gate nodes of M_{22} and M_{23}, respectively. At the same time, the average dc voltage of sinusoidal voltage signal AMP_OUT+ (AMP_OUT-) is generated through R_8C_6 (R_9C_7) and applied to the gate node of M_{20} (M_{21}). In the positive half cycle, the gate voltage (AMP_OUT+) of M_4 is larger than the gate voltage of M_2. Therefore, a small-signal drain current of I_1 flowing from the drain terminal of M_{26} is produced. In the negative half cycle, the gate voltage (AMP_OUT-) of M_{23} is larger than the gate voltage of M_{21}, a similar current I_1 is also produced. Thus the full-wave envelope detection is achieved. M_8 and M_9 form a current mirror to amplify I_1 into I_2 with the ratio of ten.

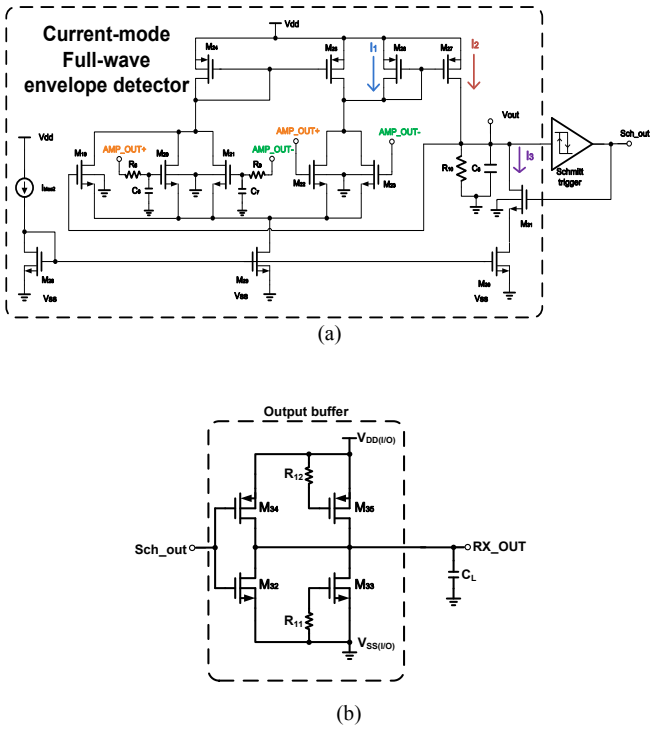

Fig. 3. Circuits of the proposed current-mode full-wave envelope detector with its output connected to a Schmitt trigger and (b) an output buffer.

The amplified current I_2 is fed to the $R_{10}C_8$ LPF to charge the capacitor C_8 and generate the output voltage Vout. Vout is fed back to the gate node of M_{19}. When Vout is high enough, the small-signal current I_1 is reduced to complete the envelope detection function. The NMOS device M_{19} is used to ensure that the DC level of Vout can be controlled no matter how strong the signal strength is. The NMOS devices M_{30}-M_{31} are used as a latch. When the data is low, the current I_3 from the $R_{10}C_8$ LPF discharges the capacitor C_8. A Schmitt trigger is used as the comparator to extract the binary data from the output signal of current-mode full-wave envelope detector. Through the Schmitt trigger, the noise or disturbance voltage on Vout does not affect output data signals at RX_OUT.

III. Measurement Results

The proposed receiver is implemented in TSMC 0.18-µm RF CMOS technology. The chip photograph is shown in Fig. 4. The die area is 0.57 mm^2 including ESD pads. A commercial 390~410 MHz antenna is used in the measurement. A 50-Ω microstrip is used to prevent reflections and mismatch losses between antenna and chip. The losses from the RF cables and adaptors are measured and compensated.

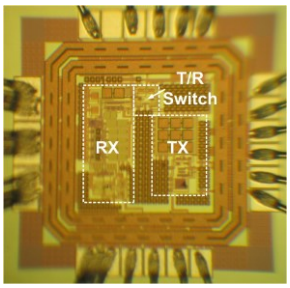

Fig. 4 Chip photomicrograph

The post-simulation waveforms of cascaded gain amplifier are shown in Fig. 5. The 5-stage cascaded gain amplifiers provide 77 dB of voltage gain at 403 MHz. In addition, the DC voltage gain of each amplifier is very small due to the effect of the capacitor (C_5) in each fully differential amplifier.

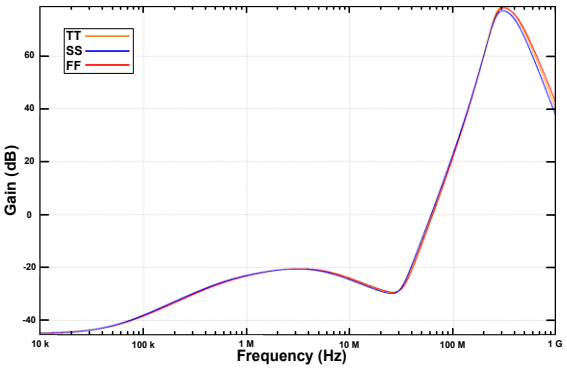

Fig. 5 The post-simulation waveforms of the differential cascaded gain amplifier.

The measurement results of the fabricated receiver have a bit rate up to 4M bps with power consumption of 0.27 mW. The output channel power is -15.55 dBm. The phase noise is -99.53dBc/Hz.

When VDDTX is 1.8 V, the distance of antennas is 6 cm, and input power is -42 dBm, the sensitivity is -45.67 dBm at 4 Mbps of data rate. The sensitivity is measured by observing the minimum signal amplitude that the receiver can receive and resolve to correct digital data. The energy per bit of 0.07 nJ/bit is achieved for the fabricated receiver. The post-simulation input referred noise integrated from 240 MHz to 410 MHz is 20 µV rms. Fig. 6 shows the measured time-domain signals of Data, RX-IN and RX_OUT from the fabricated receiver. This verifies the correct function of the proposed receiver.

The measured performance of the fabricated receiver is summarized in Table I with comparisons to other receivers. The proposed receiver has the lowest energy per bit at a higher data rate of 4 Mbps as compared to other receivers.

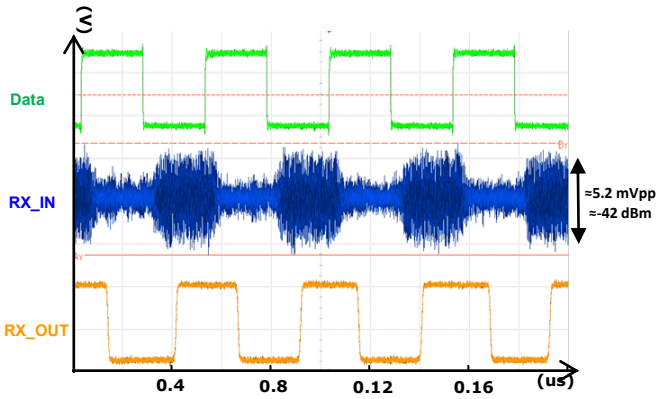

Fig. 6 The measured time-domain signals of the fabricated receiver.

Table I Performance Comparison of receivers

	[7] 2005 ASSCC	*[3] 2007 JSSC*	*[6] 2009 JSSC*	*[8] 2010 JSSC*	*This work*
Type	Receiver	Receiver in transceiver	Receiver in Transceiver (SRR)	Receiver	Receiver in transceiver
Technology	0.18µm	0.18 µm	90 nm	0.18 µm	0.18 µm
VDD (V)	0.5	0.8/1.4	0.7	1.3	1.8
Frequency Band	433 MHz	916.5 MHz	MICS (402-405 MHz)	MICS (402-405 MHz)	MedRadio (401-406 MHz)
Modulation	OOK	OOK	MSK/ OOK	ASK	OOK
Sensitivity (dBm)	-50	-65~-37	-93	-76	-45.67
Data Rate (bps)	2 M	1 M	120 k	312 k	4 M
Average Power (W)	3.1 m	2.5~0.5 m	400 µ	910 µ	0.27 m
Energy per Bit (J/bit)	1.5 n	0.5 n	3.3 n	2.9 n	0.07 n

IV. Conclusion

A wireless receiver in the MedRadio band (401~406 MHz) is designed, fabricated, and measured in 0.18-μm CMOS technology. The architecture of the receiver is simple and suitable for low power and high data rate implantable devices. The fabricated receiver is designed at 1.8 V supply voltage. The measurement results show that the receiver has a sensitivity of -45 dBm at 4 Mbps with the average power consumption of 0.27 mW. The proposed receiver has a low energy per bit of 0.07 nJ/bit. The proposed receiver has been integrated into a closed-loop epileptic treatment SOC and its function has been successfully verified in the animal test.

Acknowledgment

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