Segmentation of MR Images by Using Grow and Learn Network on FPGAs*

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Abstract— Image segmentation is one of the mostly used procedures in the medical image processing applications. Due to the high resolution characteristics of the medical images and a large amount of computational load in mathematical methods, medical image segmentation process has an excessive computational complexity. Recently, FPGA implementation has been applied in many areas due to its parallel processing capability. In this study, neighbor-pixel-intensity based method for feature extraction and Grow and Learn (GAL) network for segmentation process are proposed. The proposed method is comparatively examined on both PC and FPGA platforms.

I. INTRODUCTION

Recently, it is possible to get information about the patient's condition and to diagnose the disease using various imaging techniques without any medical operation. For this purpose, magnetic resonance imaging (MRI) is widely used in hospitals. Computer aided segmentation systems are used to distinguish different tissues on medical images in order to help in diagnosis. Mainly, computer-aided segmentation systems are performed in two stages (Fig. 1): 1) feature extraction, 2) segmentation. Feature extraction is a process to determine tissue characteristics of an image. However, segmentation is performed for determination of different (discriminating) tissue patterns in the image.

At first, the extraction of features from tissues is required for the segmentation process. Feature extraction procedure directly affects segmentation performance. In literature, many methods are proposed for the extraction of features from tissues. These methods can be collected into three main groups: 1) statistical methods, 2) model-based (structural) methods, 3) filter-based (spectral) methods [1, 2]. Statistical methods analyze the spatial distribution of gray values at neighborhood pixels of each pixel in the image [3, 4]. Modelbased (structural) methods describe the structural information on the image within a few parameters [5, 6]. In the filteringbased (spectral) methods, tissue in the image is analyzed by decomposition into different frequency and direction components. [7, 8].

Field Programmable Gate Arrays (FPGAs) are userprogrammable integrated circuits in order to realize any digital function by means of logic gates. Capability of parallel processing of FPGAs allows making rapid design and reconfiguration, but also having low costs. In recent years, it has been observed that various image processing applications on FPGA hardware platform were implemented [9, 10]. Since MR images are high-resolution and computer-aided segmentation process has high computational complexity, high-speed computing systems are needed to design for segmentation of MR images. Due to the fact that computational processes in computer-aided simulation applications are running in a sequential order, feature extraction and segmentation processes have high total computation time. Therefore, FPGAs that have the ability to parallel processing are a well-suited alternative method for the segmentation of medical images so as to reduce computation time.

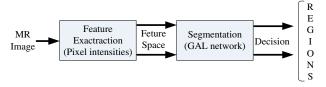


Figure 1. Computer aided segmentation of MR images.

Tahir et al. [9] realized efficient parallel architectures for 1NN classifier on FPGAs in order to classify breast and prostate cancer images. Results have shown that the classification accuracy is exactly same for both FPGAs and μ P based solutions while the FPGA based solution has superior speed performances (average up to 33 times faster). Ryan et al. [10] implemented an iris recognition algorithm, Ridge Energy Direction (RED) algorithm, on an FPGA hardware platform and PlayStation3 (PS3) game console's Cell processor. It is observed that the parallelized algorithm on the FPGA system has 2.5 times better than the Cell processor.

Artificial neural networks (ANNs) have been widely used in many applications for image processing [11, 12]. There are four reasons to use an artificial neural network as a classifier: (i) weights representing the solution are found by iteratively training, (ii) ANN has a simple structure for physical implementation, (iii) ANN can easily map complex class distributions, and (iv) generalization property of the ANN produces appropriate results for the input vectors that are not present in the training set.

In this study, Grow and Learn (GAL) network [13, 14] is proposed to segment the MR images on FPGA hardware platform. The GAL network has a dynamic structure and incremental learning. The weights and the structure of the network are automatically determined during the training. In order to decrease the overall computational time, feature vectors are simply formed by using pixel intensities.

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II. METHODS

A. Feature Extraction Process

Likewise in our previous study [15], feature vectors are formed by the intensity of the central pixel (pixel of interest) and mean value of intensities at one neighborhood of the central pixel, as shown in (1). The central pixel and oneneighborhood pixels are shown in Fig. 2a. Fig. 2b shows the mean value calculation of one-neighborhood-pixel intensities on FPGA hardware platform. Process of each state has a parallel block. Sums of I1+I2, I3+I4, I6+I7, I8+I9 are completed simultaneously. Similarly, parallel blocks are used to compute minimum distance.

$$FV = [FV1, FV2]$$

$$FV1 = I5$$

$$FV2 = (I1 + I2 + I3 + I4 + I6 + I7 + I8 + I9)/8$$
(1)

Here, FV is feature vector that has two feature elements, FV1 is the first element of the feature vector, and FV2 is the second.

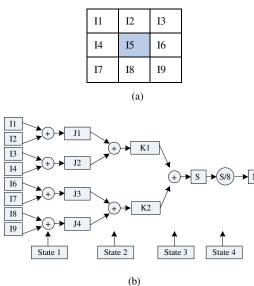


Figure 2. (a) Central pixel and one-neighborhood pixels. (b) Feature extraction process on FPGA hardware platform.

B. Grow and Learn (GAL) Network

Fig. 3 shows the structure of the GAL network. The network grows when it learns category definitions. The network has a dynamic structure; nodes and their connections (weights) are added during learning when necessary. The basic advantage of GAL network is its fast learning.

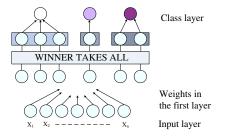


Figure 3. Structure of the GAL network.

The GAL network is an incremental network for supervised learning. The output nodes of the GAL network are formed by choosing vectors from the training set. All vectors in the training set have their own classes. The procedure for the learning algorithm of the GAL network is as follows:

Step 1. Initially choose a number of vectors randomly from the training set as many as the number of classes. Each vector represents only one class. Initialize each chosen vector as an output node of the GAL. Initialize the iteration number to zero value.

Step 2. Increase the iteration number. If the iteration number is equal to the chosen maximum value, terminate the algorithm. Otherwise, go to step 3.

Step 3. Choose one vector denoted by x_i randomly from the training set. Compute the distances between each output node of the GAL and the input vector, and find the minimum distance as follows:

$$D_{j} = \sum_{i=1}^{N} \left(x_{i} - w_{ji} \right)^{2}$$
$$D_{m} = \min_{j} \left\{ D_{j} \right\}$$
(2)

where x_i is the *i*th element of the input vector X, w_{ji} is the *j*th element of the *i*th node of the GAL, and N is the present number of input nodes. Compare the classes of the input vector and the *m*th node nearest to the input vector. If their classes are the same, go to Step 2. Otherwise go to Step 4.

Step 4. Include the input vector in the GAL network as a new output node. The elements of the input vector are assigned as the associated weights of the new output node of the GAL. Go to step 2.

During the learning with GAL, nodes generated depend on the order of the input vectors. A node previously stored may become useless when another node nearer to the class boundary is generated. When a useless node is eliminated from the GAL network, the classification performance of the network does not change. In order to decrease the network size, these nodes are extracted from the GAL by the forgetting algorithm given below.

Step 2. Increase the iteration number. If the iteration number is equal to the maximum value, terminate the algorithm. Otherwise, go to Step 3.

Step 3. Choose the next node from the GAL in an order. This node is extracted from the network and is given as an input vector to the GAL network.

Step 4. Compute Eq. (2). Compare the classes of the input vector and the *m*th node of the GAL. If their classes are not the same, go to Step 5. Otherwise, go to Step 3.

Step 5. Include the input vector again in the GAL. Go to Step 2.

C. Pseudo-Random Generator on FPGAs

Training of the GAL network has a randomization process. In the study, the randomization process is obtained by Linear Feedback Shift Registers (LFSRs). An LFSR is a shift register whose input bit is a linear function of its previous state [16]. Applications of LFSRs are frequently included generating pseudo-random numbers.

D. Segmentation Process on FPGA

The scheme for segmentation of MR images on FPGA hardware platform is described in Fig. 4. The original MR image, training set and test set are sent serially to FPGA platform by using a software interface which is compiled with Visual C#. The data is stored in an SSRAM. When data transfer is finished, feature extraction and then segmentation processes is started. The software interface which sends all the data (image, training and test sets) from the computer to FPGA platform, and vice versa is shown in Fig. 5.

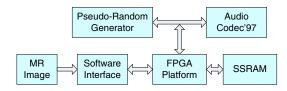


Figure 4. The scheme for segmentation process on FPGA.

III. RESULTS AND CONCLUSION

In this study, an original MR-brain image is segmented by using Matlab software on PC with the speed of 2.67 GHz and 4 GB RAM (Intel Core i7 CPU M620). Afterwards, the same image is segmented on the FPGA platform Xilinx Virtex-5 with 100.5 MHz clock frequency. Size of the image is 300x346 with the resolution of 8-bit. IEEE 754 32-bit floating point number standard is used to increase accuracy of the arithmetic operations.

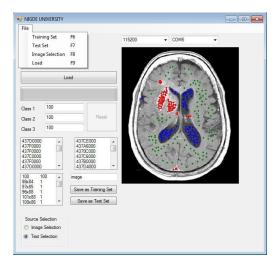


Figure 5. The software interface for sending image and data.

Fig. 6(a), (b) and (c) show original, segmented images on PC with Matlab software and on FPGA hardware platform, respectively. As the segmentation results of the Matlab and FPGA is compared, it is observed that the segmentation results obtained from both platforms have high accuracy

performance and they produce very similar segmentation results.

The performance of the proposed method is measured in terms of the number of nodes (NoN), training time (TT) of the GAL network, segmentation time (ST) and accuracy for both platforms and results are presented in Table 1. It is observed that the hardware implementation with FPGA consumes much less time than the computer simulation with Matlab for both the training and the segmentation processes. In order to test and compare the performances of the network quantitatively, a test set (which is different from the training set) is formed for the image by selecting a total of 150 features from each tissue. Accuracy features, 50 performances for both platforms are obtained 99.80% and 99.60% for Matlab software and FPGA hardware platforms, respectively, as presented in Table 1. It is observed that the segmentation process of the MR-brain image by using the FPGA hardware platform is about 415 times for training time and 120 times for segmentation time faster than the computer simulation platform with MATLAB software.

Although accuracy performances for both platforms are quite close, total computational time of the FPGA hardware platform is superior to computer simulation platform. Thus, segmentation of MR images on FPGAs can be successfully implemented in real-time. Because of the flexibility in design and reconfigurability of FPGAs, it has many advantages for designers both in terms of cost and implementation of new algorithms. In future studies, we will concentrate on the implementation of the segmentation for medical images on multi-core processors such as graphics processing unit (GPU).

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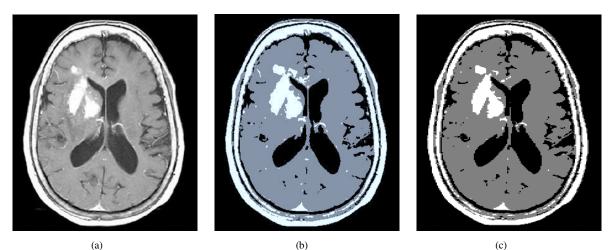


Figure 6. (a) Original MR image, Segmented MR image (b) on PC with Matlab software and (c) on FPGA platform.

TABLE I. PERFORMANCE RESULTS OF THE COMPUTER SIMULATION AND THE FPGA

Platform		Processor (MHz)	NoN	TT (ms)	ST (ms)	Accuracy (%)
Computer simulation	Matlab	2400	4	108	8830	99.80
FPGA	Xilinx Virtex-5	100.5	4	0.26	73.68	99.60

NoN: number of nodes, TT: training time, and ST: segmentation time