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1.2V Constant-gm Rail-to-Rail CMOS Op-Amp Input Stage with New Overlapped Transition Regions Technique for ECG Amplifier

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Abstract— **The conventional technique of overlapped transition regions for producing a constant transconductance rail to rail Op-Amp input stage can only tolerate a limited amount of voltage shifting. This is limited by the minimum Vgs required for active mode operation of transistors. In this paper, we present a novel overlapped transition regions technique that overcomes the limitation of the conventional technique. This new overlapped transition regions technique has no voltage shifting limit. For both N-type and P-type conventional complementary differential input pairs, one source follower and one MOSFET are added to control the saturation point of current of input pairs. For 1.2V single supply voltage, simulation results demonstrate ±3.71% of overall transconductance variation. Cadence SPECTRE simulator and TSMC 0.25-µm CMOS technology are used to layout and simulate this work.**

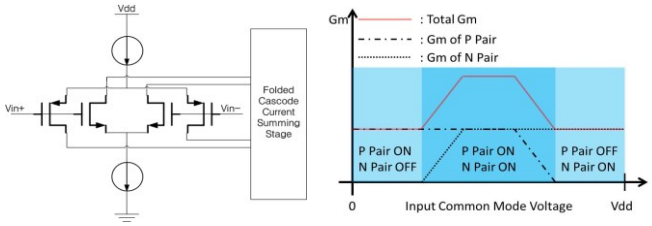
I. Introduction

The operational amplifier is one of the most widely used building blocks in analog IC and mixed-mode circuits. With the trend of battery powered health monitoring systems, portable ECG for example, portable biomedical devices demand circuits operating in low supply voltage environments for lower power consumption and the result of lowered supply voltage is a reduced input common-mode range (ICMR) of the op-amp. Commonly used way to overcome reduced ICMR and ensure rail to rail input common-mode signal is complementary differential pairs operated in parallel.

One problem with the complementary differential pairs structure, however, is overall transconductance (gm) variation in the middle range of common-mode input signal. Fig 1 shows complementary differential pairs structure and overall gm variation of that structure. In Fig 1, both N-channel and P-channel input differential pairs are turned on at the same time in the middle range of common-mode input signal and that causes about 2 times the transconductance variation which results in a variable unity gain frequency and stability problems. In the past years, a number of constant-gm techniques for the complementary differential pairs structure have been proposed and the overlapped transition regions technique is one of those techniques [1-3]. The advantages of conventional and modified overlapped transition regions techniques using voltage level shifting are simplicity and high CMRR.

One of the main drawbacks of those techniques, however, is a limited amount of voltage shifting. In [1] and [2], the conventional and modified overlapped transition regions techniques are introduced and the supply voltages of those techniques are 3V and 1.6V respectively. However, if supply voltage is lower than 1.6V, required amount of voltage shifting for a constant-gm is smaller than what is required for a 1.6V supply voltage. Because of the minimum Vgs required for active mode operation of transistors, the voltage shifting amount of input common-mode signal cannot be lower than the power supply limited amount of voltage shifting. Even if the shifted amount of input common-mode signal is lower than the limited amount using sub-threshold current, the aspect ratio of transistors which are used to shift common-mode input signal should be extremely large and those transistors cannot be used practically. In this paper, a novel overlapped transition regions technique is proposed. The new technique has no limitation of voltage shifting amount without significant degradation of advantages of previously introduced techniques.

The conventional and modified overlapped transition regions techniques are briefly explained in Section II, and Section III presents a novel overlapped transition regions technique with simulation results. Conclusion is given in Section IV.

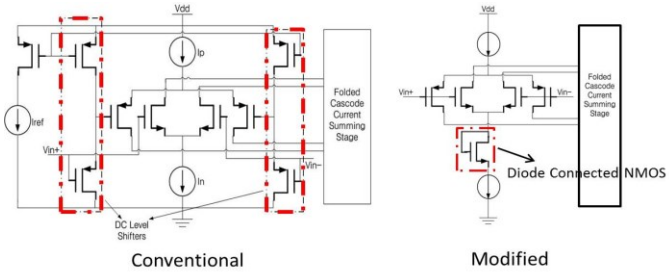


[Fig 1. Conventional Complementary Differential Pairs]

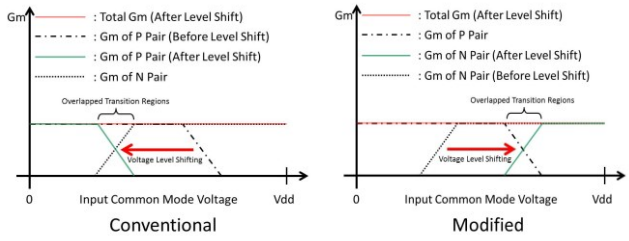
II. Conventional and Modified Overlapped Transition Regions Technique

In [1], the overlapped transition regions technique using DC voltage level shifting has been proposed. This technique uses two PMOS source followers to shift DC voltage level and Fig 2 shows the structure and working principle of this technique. The input signal of the amplifier is directly connected to the input of a PMOS source follower and N-channel input differential pair, and the output of the PMOS source follower is connected to the input of the P-channel differential pair. Thus, shifted input signal is fed to the input of the P-channel differential pair and the voltage shifting amount is voltage difference between gate and source of PMOS of source follower (|Vgsp|). However, this technique has a limited amount of voltage shifting. Fig 3 shows the simulation results with the supply voltage of 1.6V, 1.4V, and 1.2V. TSMC 0.25-µm technology is used to simulate this

work and the minimum threshold voltage of PMOS is about -500mV which is the minimum Vgs required for active mode operation of PMOS source follower. The required voltage shifting amount for a constant-gm is 550mV, 330mV, and 110mV with 1.6V, 1.4V, and 1.2V of supply voltage respectively. For the case of 1.6V supply voltage, required voltage shifting amount for a constant-gm is 550mV which is larger than the minimum Vgs and the simulation result shows ±4.97% variation of overall transconductance with aspect ratio of (350/1) for PMOS source follower (Fig 3(a)). However, with the same aspect ratio of PMOS source follower, Fig 3(b) and (c) show that overall transconductances cannot be kept constant because required voltage shifting amount for a constant-gm is smaller than the minimum Vgs. Using sub-threshold drain current, overall transconductance can be kept constant, but the aspect ratio of PMOS source follower would need to be $(10^6/1)$ and $(10^9/1)$ with 1.4V and 1.2V supply voltages, respectively. Those aspect ratios are obviously impractical and the conventional overlapped transition regions technique has a limited amount of voltage shifting as a result.



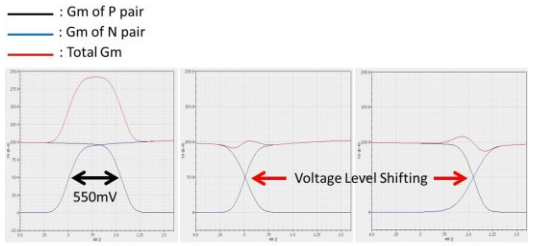
(a) Structure of Conventional and Modified Overlapped Transition regions technique



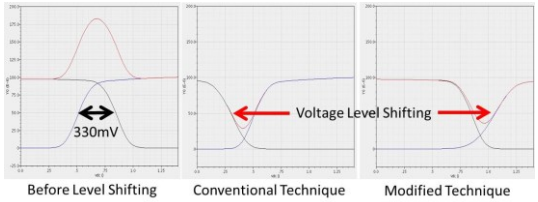
(b) Working Principle

[Fig 2. Conventional and Modified Overlapped Transition Regions Technique]

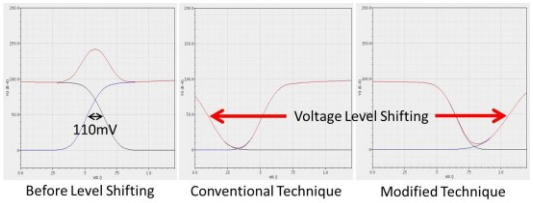
The modified overlapped transition regions technique is proposed in [2]. The structure of this technique is shown in Fig 2(a). One diode connected NMOS is added above the tail current source of the N-channel differential input pair. The input common-mode voltage of N pair requires one more gate-source voltage of NMOS (Vgsn) to be turned on because of diode connected NMOS and the voltage level of the N-channel differential input pair is shifted. The modified overlapped transition regions technique still has a limited amount of voltage shifting. The minimum threshold voltage of NMOS is about 450mV which is smaller than required voltage shifting amount for a constant-gm of 1.6V supply voltage. The aspect ratio of diode connected NMOS is (77.5/1) and the variation of overall transconductance is ±8.66% with 1.6V supply voltage (Fig 3(a)). But for the case of 1.4V and 1.2V supply voltage, required voltage shifting amount for a constant transconductance is smaller than the minimum Vgs, and overall transconductance cannot be kept constant with the same aspect ratio of diode connected NMOS (Fig 3(b) and (c)). Even if we use sub-threshold current, $(3\times10^4/1)$ and $(3\times10^7/1)$ of aspect ratio of diode connected NMOS are required with 1.4V and 1.2V of supply voltage and those transistors are impractical too.



(a) 1.6V Supply Voltage

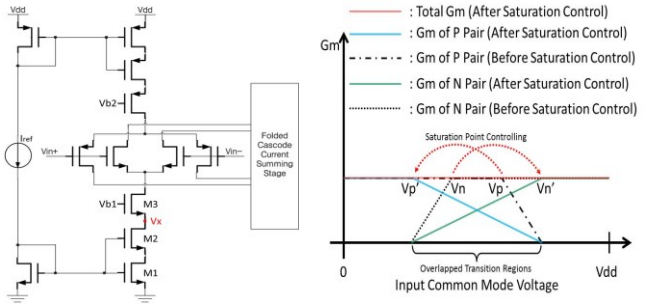


(b) 1.4V Supply Voltage

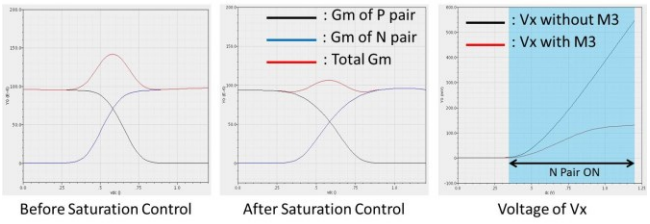


(c) 1.2V Supply Voltage

[Fig 3. Limitation of Minimum Voltage Shifting Amount]



(a) Structure and Working Principle of New Overlapped Transition Regions Technique



(b) Simulation Results with 1.2V Supply Voltage

[Fig 4. New Overlapped Transition Regions Technique]

III. New Overlapped Transition Regions Technique

With the DC voltage level shifting technique, another type of overlapped transition regions technique is also introduced in [1]. The main concept of that technique is saturation point control of current in N- and P-channel differential input pairs. This type of overlapped transition regions technique does not have a limited amount of voltage shifting. Proposed technique controls the aspect ratios of the input differential pairs transistors and the optimized aspect ratios for constant-gm are 1/5 and 1 for NMOS and PMOS respectively. As mentioned in [1], those aspect ratios are too small and degrade the noise performance and transistors mismatch insensitivity.

A novel overlapped transition regions technique proposed in this section has the same basic concept as a previously introduced technique that controls the current saturation points of differential input pairs. We do not control the aspect ratios of differential input pairs transistors, but rather control the saturation point of a current source.

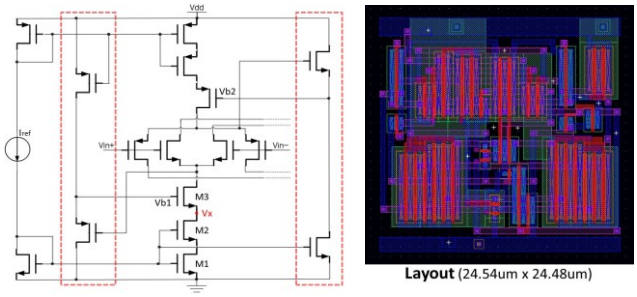
Fig 4 shows the structure and the basic working principle of the new overlapped transition regions technique with simulation results. M1 and M2 in Fig 4(a) are the current source of the N-channel input pair and M2 is added to lower transconductance variation in the saturation region. In Fig 4(a), without saturation point control, the saturation point of current of the N-channel input pair is indicated as Vn. Without saturation point control, M3 is not added and Vx is voltage of sources of the N-channel input pair. With this condition, in the turn-on region, the triode region and the saturation region of N-channel differential input pair, the voltage of Vx varies along with input common-mode voltage (Fig 4(b)). However, with saturation point control, the voltage of Vx is lowered because of the addition of M3 (Fig 4(b)) and the voltage difference between the drain and source of M2 (Vdsm2) is lowered. As a result, a larger input common-mode voltage is needed to saturate M2 and the saturation point, Vn, is shifted to Vn' (Fig 4(a)). In Fig 4(b), the cut off voltage of the PMOS input pair is about 850mV of the input common-mode voltage and that voltage must be the same as the shifted saturation point voltage of NMOS input pair, Vn'. For the saturation of M2 at 850mV of input common-mode voltage, the voltage difference of Vgsm2 and Vthm2 must be the same as Vdsm2 (1.1). Vgsm2, Vthm2, and Vdsm2 are the gate-source voltage, threshold voltage, and drain-source voltage of M2 respectively. From the (1.1), (1.2), and (1.3), the value of Vx is about 160mV at 850mV of input common-mode voltage and from the (2), Vb1 should be 880mV. The case of the P-channel input pair is symmetric with the case of the N-channel input pair and the value of Vb2 is about 360mV when there is 300mV of input common-mode voltage, which is the cut off voltage of N-channel input pair. The simulation result of saturation point control is shown in Fig 4(b). For this simulation, 1.2V single supply voltage is used.

$$V_{gsm2} - V_{thm2} = V_{dsm2}\ \text{(Saturation of M2)} \quad (1.1)$$

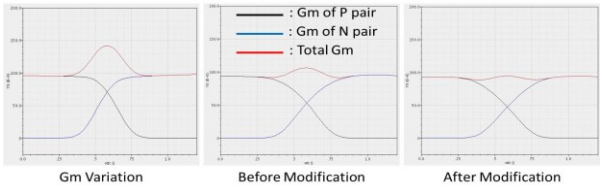
$$V_{gm2} - V_{sm2} - V_{thm2} = V_{dm2} - V_{sm2} \quad (1.2)$$

$$V_{gm2} - V_{thm2} = V_{dm2} = V_x \quad (1.3)$$

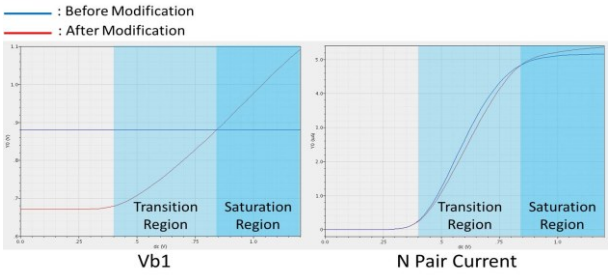
$$\left(\frac{1}{2}\right)\mu_n C_{ox}\left(\frac{W_{m3}}{L_{m3}}\right)(V_{b1} - V_x - V_{thm3})^2 = I_{sat\text{-}m3} \quad (2)$$



(a) Structure and Layout of Modified New Overlapped Transition Regions Technique



(b) Simulation Results with 1.2V Supply Voltage

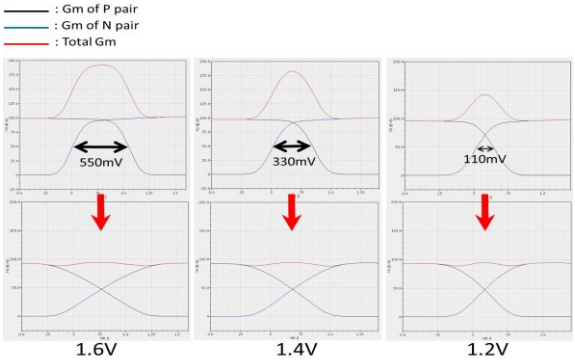


(c) Comparison of Before and After Modification

[Fig 5. Modified New Overlapped Transition Regions Technique]

The simulation result of Fig 4(b) shows ±7.48% variation of overall gm and for better performance, some modification is required. Shifted saturation points, Vn' and Vp', are well controlled, but the variation of overall gm in the overlapped transition regions degrade the performance. To decrease this variation, the voltage of Vb1 and Vb2 are modified. Fig 5(a) shows the structure and layout of modified new overlapped transition regions technique. PMOS and NMOS source followers are added to control the voltage of Vb1 and Vb2 respectively. The input signal of the PMOS source follower comes from the sources of the N-channel input pair and this signal is the same as the signal of 'Vx without M3' of Fig 4(b). PMOS source follower shifts this signal as much as Vgs of PMOS and this shifted signal is connected to Vb1. Fig 5(c) shows that before modification, Vb1 is constant and cannot control the current of the N-channel input pair in the transition region. Vb1 of the modified technique, however, varies along with the input common-mode voltage and set to 880mV at 850mV of input common-mode voltage to control Vn'. Thus, in the transition region of the modified technique, Vb1 and Vgs of M3 are smaller than those of the unmodified technique. As a result, because of lowered Vgs of M3, the current of N-channel input pair is lowered in the transition

region and the shape of gm is more linear than unmodified one (Fig 5(b)). The case of the P-channel input pair is symmetric with the case of the N-channel input pair. The simulation result shows that the variation of overall gm of the modified new transition regions technique is ±3.35%. The results of post layout simulation are shown in Table 2, and the variation of overall gm of the modified new transition regions technique is ±3.71%.



[Fig 6. Simulation Results of Overall Gm Variation with New Overlapped Transition regions technique]

Fig 6 shows the schematic simulation results of overall gm variation with supply voltage of 1.6V, 1.4V and 1.2V using the saturation point control technique which is the new overlapped transition regions technique proposed in this paper. These results demonstrate that if overall gm is larger than the gm of N- or P-channel input pair in the middle range of common-mode input signal, the saturation point control technique can be used with any supply voltage without limited amount of voltage shifting. In addition, with 1.6V supply voltage, the overall gm variation of the proposed technique is ±3.35% and better than the conventional and modified overlapped transition regions technique. Overall gm variations of the conventional and modified overlapped transition regions technique are ±4.97% and ±8.66%, respectively. The proposed saturation point control technique is compared with the conventional and modified overlapped transition regions technique in table 1.

IV. Conclusion

A novel overlapped transition regions technique for a portable ECG rail to rail amplifier with constant-gm is proposed. Previously introduced techniques (conventional and modified overlapped transition regions techniques) have a limited amount of allowed voltage shifting that is overcome with the solution demonstrated here. Using Cadence SPECTRE simulation with TSMC 0.25µm technology, results show that previously introduced techniques can be used with 1.6V supply voltage, but because of the minimum Vgs required for active mode operation of transistors, 1.4V or 1.2V supply voltage cannot be used. The saturation point control technique which is the new overlapped transition regions technique proposed in this paper, however, has no limited amount of voltage shifting and works well with 1.2V supply voltage as well as 1.4V and 1.6V supply voltage. Overall gm variation is ±3.35% (±3.71% with post layout simulation), ±3.49%, and ±3.35% with 1.2V, 1.4V and 1.6V supply voltage respectively. In addition, overall gm variation of proposed technique is smaller than that of previously introduced techniques for 1.6V supply voltage.

	Conventional Overlapped Transition Regions Technique	Modified Overlapped Transition Regions Technique	New Overlapped Transition Regions Technique
Supply Voltage	1.6V	1.6V	1.2V
ICMR	Rail-to-Rail	Rail-to-Rail	Rail-to-Rail
Gm Variation	±4.97%	±8.66%	±3.35%
Gain	74.89dB	75.98dB	74.94dB
UGF	1.106MHz	1.269 MHz	0.998 MHz
Phase Margin	60.45º	57.2 º	59.1 º
CMRR	≥80dB	≥73.29dB	≥80.27dB
Avg. Power Consumption	79.48µW	69.14µW	62.17µW
Limitation of V Shifting	Limitation Exists	Limitation Exists	No Limitation

[Table 1. Comparison of 3 techniques]

	Post Layout Simulation Results
Supply Voltage	1.2V
Gm Variation	±3.71%
Gain	75.31dB
UGF	1.001MHz
Phase Margin	59.1º
CMRR	≥80.18dB
Avg. Power Consumption	62.21µW

[Table 2. Results of Post Layout Simulation]

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