35th Annual International Conference of the IEEE EMBS
Osaka, Japan, 3 - 7 July, 2013

A Full Custom Analog Front-End for Long-time ECG Monitoring

Meiying Wen, Yayu Cheng, Ye Li*

Abstract—**An analog front-end (AFE) used in portable electrocardiogram (ECG) monitoring devices is proposed. This AFE has included all necessary functions for the commercial applications. The core circuit consists of the instrumentation amplifier (IA), a 2nd order Butterworth low pass filter, and the second amplifying stage. The driven-right-leg circuit is integrated in the IA to effectively suppress the common mode interference. And the power management circuits provide a stable supply voltage, bias current and reference voltage for the other circuits. To guarantee the validity of the continuous monitoring data, the leadoff monitoring circuit is developed to monitor the connection of the leads. The chip is taped out with SMIC 0.18μm CMOS process, and the measured results show that the common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) achieve 75dB and 90dB respectively, and the equivalent input referred noise is 12μV.**

Keywords: ECG, AFE, analog front-end, LDO, CMRR

I. Introduction

Cardiovascular disease becomes an important issue of public health. The report [1] said the cardiovascular disease is the first cause of death in China, especially some heart disease always happens in a sudden. Therefore early diagnosis is important to the prevention of the heart related diseases. However, the traditional holter in hospital is bulky with many wires. It's not convenient in the daily life. Internet of Things [2] for Healthcare proposes family healthcare monitoring in the daily life, which is different from the diagnosis and therapy for the patients of the hospital. And the bio-sensors, such as the portable ECG measurement device, are the key technology of Internet of Things for Healthcare. The traditional portable ECG measurement devices are composed of discrete components on PCB; however, it takes more time and money to maintain. So the ECG AFE with high integration is more suitable for long-time monitoring and mass production.

Due to the weak amplitude and low frequency characteristics, e.g. the amplitude of the ECG signal is around tens of μV to several mV, physiological signals are easy to be influenced by the environment, such as the 50Hz power line interference. And in the CMOS IC manufacture process, the flicker (1/*f*) noise is serious at low frequency. So the common mode rejection and power supply rejection performance of the AFE determines the quality of the ECG signal acquired. And low power [3] and low noise design are desired for longer battery lifetime or even self-powered operation.

This research was supported by the Shenzhen Research Grants of ZDPT201110260075A, CG201007290007A and CXB201104220026A.

Meiying Wen; Yayu Cheng; Ye Li*: Authors are Shenzhen Institutes of Advanced Technology (SIAT), Key Lab of Health Informatics, Chinese Academy of Sciences, Shenzhen 518055, P.R. China (corresponding author, Ye Li, e-mail: ye.li@siat.ac.cn).

There are some AFE for ECG signal measurement reported [4-8]. However, most of them just only have integrated the amplifying circuit and filter. In this paper, besides the amplifying circuit and the filter circuit, all the necessary commercial functions are fully integrated on this AFE, which can be applied to biometrics authentication of information security for body sensor networks [9], the portable data acquisition devices for ubiquitous healthcare services [10] and MP3 for music therapy on hypertension [11]. The high PSRR low dropout voltage regulator (LDO) is designed within the power management circuits to improve the power supply rejection performance of the system. And the high CMRR instrumentation amplifier (IA) with driven-right-leg (DRL) circuit is designed to suppress the 50Hz power line interference more effectively. To guarantee the continuous data validity, the leadoff monitoring circuit is integrated to monitor the connection of electrodes on the human body.

The system architecture of the AFE is given in section II. The circuit design and the measured results are presented in section III and section IV.

II. System Architecture

The system architecture of the portable ECG monitoring device used as a bio-sensor is shown in Figure.1. The ECG signal detected with the electrodes is amplified and filtered by the AFE. After processed by MCU, the signal displays on the terminal devices by wireless or USB way. And the most important component of the ECG monitoring device is the ECG detection AFE, which is presented in this paper.

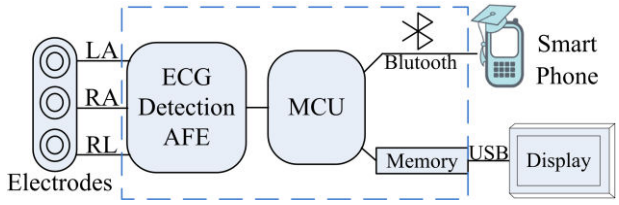


Fig.1. System Architecture of the Portable ECG Monitoring Device

The block diagram of the ECG detection AFE is shown in Fig.2, which consists of three electrodes (LA, RA, RL), power management circuits, high CMRR IA, 2nd order Butterworth low pass filter (LPF), the second amplifying stage, and the leadoff monitoring circuit. The power management circuits, which consist of LDO and some buffers, provide stable voltage and bias current and reference voltage for the other sub-circuits. The ECG signal is detected through left arm (LA) and right arm (RA) electrodes in the presence of IA's input differential, and the right leg (RL) electrode is connected to DRL circuit. And then the amplified ECG signal goes through a 2nd order Butterworth LPF. Following the LPF is the second amplifying stage. The DC blocks that consist of capacitor and resistor between the IA and LPF and the amplifying stage will

suppress the offset of baseline voltage to guarantee the DC level of the signal and work as high pass filters. And if any electrode of LA, RA, or RL is disconnected with the body, the leadoff monitoring circuit would give the alarm.

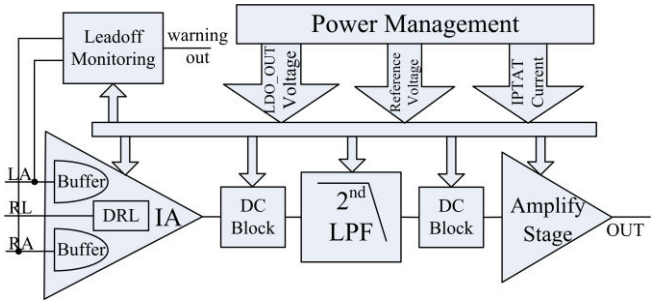


Fig.2. Block Diagram of the AFE

III. CIRCUIT DESIGN

A. Low Dropout Voltage Regulator (LDO)

For the battery power supply voltage declines while operating, it's necessary to include a LDO in the AFE. The LDO provides a stable supply voltage when the input voltage varies. As shown in Fig.3, the LDO consists of a high PSRR bandgap reference circuit, a folded cascode differential amplifier as error amplifier (EA), a source follower as buffer, the power transistor MP and the feedback resistors R_{f1} and R_{f2}. The sampled voltage VFB detected by the feedback resistors is fed back to the EA, which has a high voltage gain. Even if the supply voltage VDD varies, the output of LDO (LDO_OUT) is kept at a stable voltage by the negative feedback network, as seen from the following:

$$\text{LDO\_OUT} = \text{VBG} \times \left(1 + \frac{R_{f1}}{R_{f2}}\right) \tag{1}$$

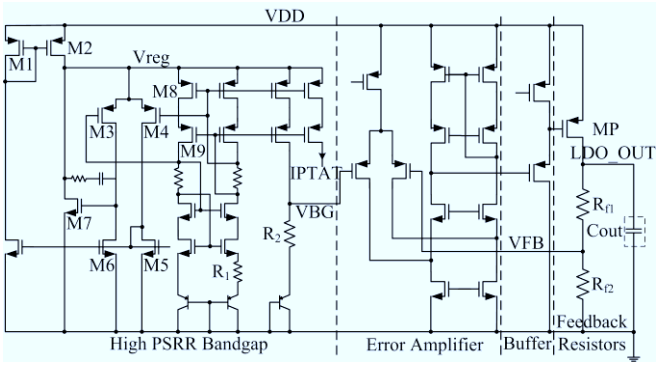


Fig.3. Circuit of The high PSRR LDO

Here VBG is the reference voltage (in this paper, it's 1.19V) generated by the high PSRR bandgap circuit as shown in Fig.3. The bandgap circuit is similar to the high PSRR bandgap reference in [12]. It employs the amplifier consists of M2~M7 to pre-regulate the supply voltage VDD to improve PSRR of the bandgap. The pre-regulated voltage Vreg works as the supply voltage for the core circuit of bandgap. And the error amplifier utilizes the cascode structure as the output stage to achieve high voltage gain. The high PSRR bandgap reference and the high voltage gain EA contribute to the high PSRR LDO. The current IPTAT (PTAT, proportional to absolute temperature) generated by the bandgap is used to provide bias current for the other sub-circuits (in this paper, it is 500nA). And the off-chip capacitor C_{out} as shown in Fig.3 is necessary to assure the LDO's stability and the transient performance.

B. Instrumentation Amplifier (IA)

As illustrated in Fig.4, the IA consists of four operational amplifiers (OP) (A1~A4), the poly resistors and three buffers. Several ways are adopted to improve the CMRR of IA. 1) Improve the circuit's symmetry by the optimization of the symmetric layout work; 2) Improve the performance of OP; 3) Integrate the DRL circuit with the IA.

To make the OP's performance more close to the ideal characteristics, the OP is designed with high voltage gain and stable performance under different corners or temperature. In this paper each OP is designed as a two stage folded rail to rail input differential cascode amplifier. To achieve the stable high performance under different corners, the W/L ratio of the transistors should be designed properly. The two input buffers in Figure.4, connected to LA and RA, are utilized to increase the equivalent input impedance (it's hundreds of MΩ in this paper) to meet the match with the high impedance of the body. If $R_{0a}=R_{0b}=R_0$, $R_{1a}=R_{1b}=R_1$, $R_{2a}=R_{2b}=R_2$, and $R_{3a}=R_{3b}=R_3$, the DC gain of the IA can be approximated by the following:

$$\text{Gain} = \left(1 + \frac{R_1}{R_0}\right)\frac{R_3}{R_2} \tag{2}$$

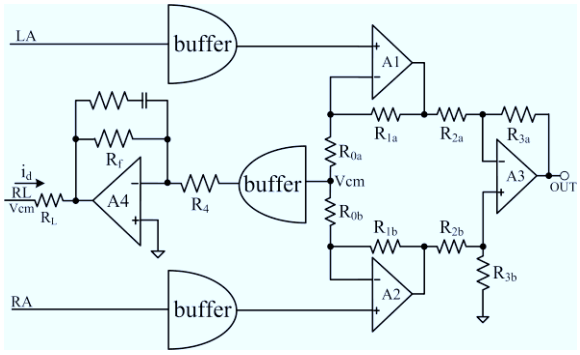


Fig.4. Architecture of Instrumentation Amplifier

The DRL circuit which consists of A4 and another buffer in Fig.4 is used to suppress the common mode interference more effectively. The common mode voltage on the human body Vcm is sensed and connected to the DRL circuit. The sensed voltage, Vcm, is inverted, amplified and fed back to the right leg [13], and then the feedback loop makes the common mode voltage decrease. Vcm can reduce more by increasing the gain of the amplify circuit (R_f/R_4), as seen from (3), where i_d is the body's current caused by the power line interference.

$$V_{cm} = \frac{i_d \times R_L}{1 + R_f/R_4} \tag{3}$$

C. Low Pass Filter and the Amplify Stage

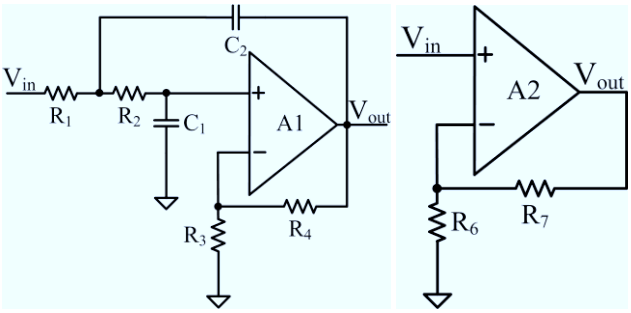
Following the IA is a 2nd order Sallen-Key low pass filter with the voltage gain ($1+R_4/R_3$), as shown in Fig.5(a). To meet the pass-band of ECG monitoring mode, 0.5Hz~50Hz [14], the cutoff frequency f_c of the filter, as seen from (4), is set to be 100Hz. All the capacitors and resistors are off chip, so the

cutoff frequency is easy to adjust by changing the resistors and capacitors.

The circuit that consists of A2, R_6 and R_7 in Fig.5(b) is the second amplifying stage, which would amplify the filtered signal by the voltage gain in (5).

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \tag{4}$$

$$\text{Gain} = 1 + \frac{R_7}{R_6} \tag{5}$$



(a) (b)

Fig.5. (a)Schematic of Low Pass Filter (b)The second Amplify Stage

D. Leadoff Monitoring Circuit

The leadoff monitoring circuit is presented in Fig.6. The simple two-stage open loop amplifier, A1 and A2, working as comparators, compares the voltage at the electrodes, which is about the reference voltage 1.5V while operating well, with the voltage 2.8V. If any electrodes of LA, RA or RL is disconnected with the human body, the voltage at the electrode is pulled to the power supply voltage (VDD) that is higher than 2.8. And the leadoff monitoring circuit changes the output from '0' to '1', giving the leadoff alarm.

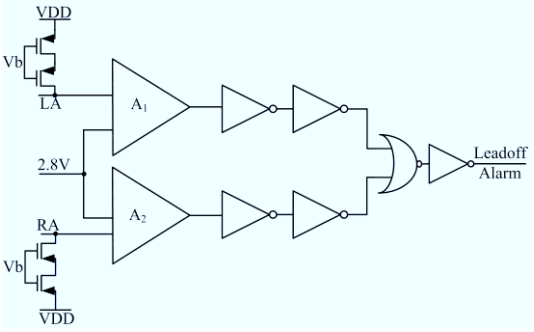


Fig.6. Leadoff monitoring circuit

IV. MEASURED RESULTS AND DISCUSSION

The proposed full custom AFE for ECG measurement is designed and fabricated with SMIC 0.18μm process. The chip area is 1.1mm×1.3mm as shown in Figure.7, and it consumes 190μA while operating with 3V supply voltage. The measured amplitude frequency response of the system is shown in Figure.8, the mid-band (0.5Hz~100Hz) voltage gain is about 51dB. And the measured equivalent input referred noise in 10 seconds is shown in Figure.9. It is around 12μVpp, where the 1/*f* noise occupies the largest proportion. The LDO is employed to provide a stable supply voltage for the other circuits to improve the PSRR. When the supply voltage varies from 2.9V~5.5V, the output voltage of the LDO (LDO_OUT) stays at 2.8V as shown in Figure.10. When VDD is low, LDO_OUT follows it.

Fig.11 shows the ECG signal measured on the human body by this proposed AFE and its FFT analysis results. It is a weak signal at 0.912Hz. The results demonstrate that the proposed AFE has detected the ECG signal successfully.

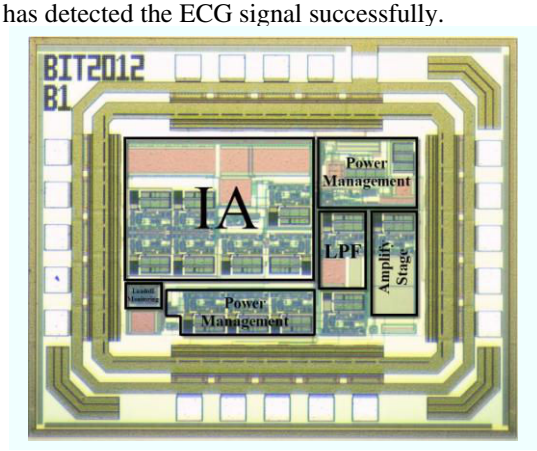


Fig.7. Micrograph of proposed AFE

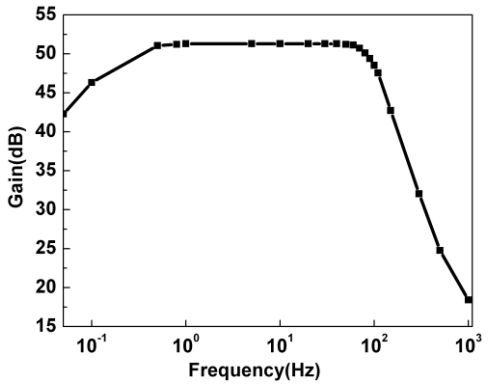


Fig.8. Measured Frequency Response of the system

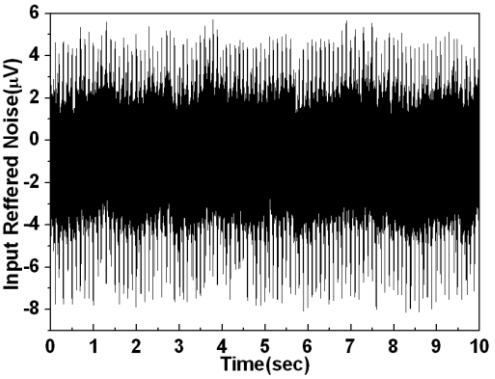


Fig.9. Measured Input Referred Noise

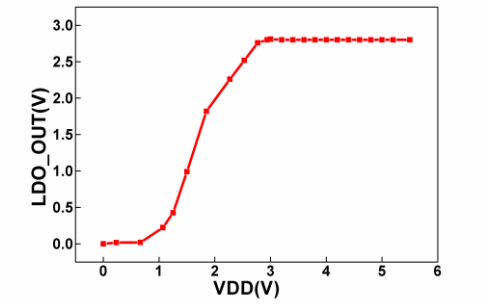
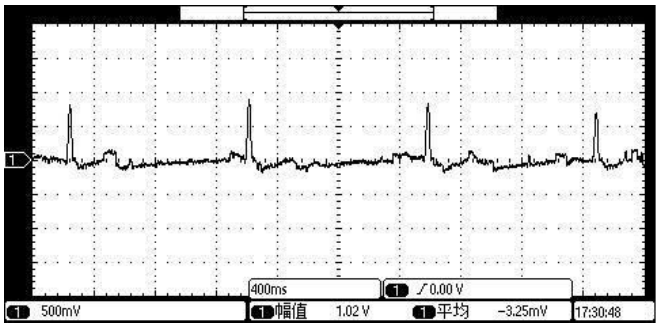
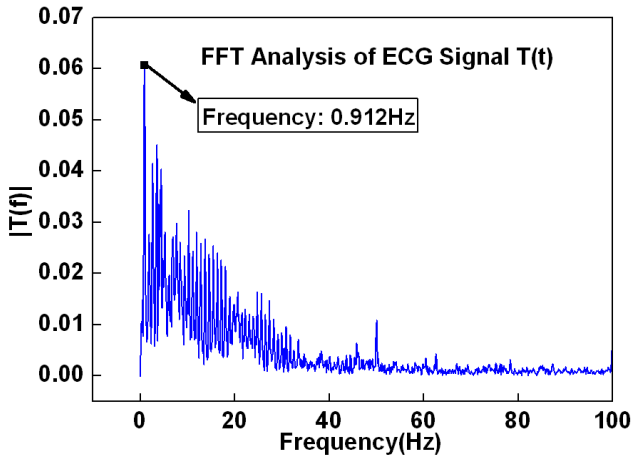


Fig.10. Measured results of the LDO_OUT versus VDD



(a)



(b)

Fig.11. (a)Measured ECG Signal (b) FFT Analysis of the measured signal

Table I summarizes the system specifications compared to other reported works. The design in [16] of ADI has lower power consumption and higher CMRR for its advanced process and its different IA structure. However, the AFE in this paper can work with a wider range of supply voltage and performs higher PSRR and lower equivalent input referred noise with the help of the high PSRR LDO. It can be seen that this work offers comparable performance of high CMRR, high PSRR, wide range of supply voltage and low noise, even though some technologies, such as lowering down the bias currents and optimizing the structure of IA, can be studied to reduce the power consumption further.

TABLE I. Specifications Comparison With Other Works

Parameters	This work	2011[15]	2012[16]
Technology	CMOS 0.18μm	CMOS 0.35μm	DMOS 0.35μm
Supply(V)	2.9~5.5	3.3	2.0~3.5
Mid-Band Gain	51dB	66.5dB	100
Bandwidth(Hz)	0.5~100	0.01~100	0.5~40
Current Consumption	190μA	725μA	170μA
CMRR	75dB	>70dB	80dB
PSRR	95dB	>73dB	90
Input Referred Noise	12μVpp	2.3μVrms	14μVpp
Leadoff Monitoring Circuit	Yes	No	Yes

V. CONCLUSION

A full custom AFE for ECG acquisition system is presented in this paper. All the necessary functions have been integrated in the proposed AFE, besides the essential amplify and filter circuits. Some novel techniques are adopted to improve the CMRR and PSRR. The measured results for the ECG chip have demonstrated the functionalities successfully. It is suitable for portable long-time ECG monitoring devices applied in personal and family health caring.

REFERENCES

[1] The Report on Cardiovascular Disease in China, 2011, unpublished.

[2] J. Couturier, D. Sola, G. Scarso Borioli, C.Raiciu, "How can the Internet of Things help to overcome current healthcare challenges", *Digiworld Economic Journal*,*Communications & Strategies*, no.87,3rd Q. pp.67-81,2012.

[3] Ye Li; Bakkaloglu, B.; Chakrabarti, C., "A System Level Energy Model and Energy-Quality Evaluation for Integrated Transceiver Front-Ends", *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on* , vol.15, no.1, pp.90-103, Jan. 2007

[4] Honglei Wu, and Yong Ping Xu, "A 1V 2.3μW biomedical signal acquisition IC," *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, pp.119-128, 6-9 Feb. 2006.

[5] Chun-Chieh Huang; Shao-Hang Hung; Jen-Feng Chung; Van, L.-D.; Chin-Teng Lin;, "Front-end amplifier of low-noise and tunable BW/gain for portable biomedical signal acquisition," *Circuits and Systems, ISCAS, IEEE International Symposium on*, pp.2717-2720, 18-21 May, 2008.

[6] Trakimas, M.; Sungkil Hwang.; Sonkusale, S.;, "Low Power Asynchronous Data Acquisition Front End for Wireless Body Sensor Area Network," *VLSI Design, 24th International Conference on*, pp.244-249, 2-7 Jan. 2011.

[7] Weibo Hu, Yen-Ting Liu, Das V, "An ultra-low power interface CMOS IC design for biosensor applications," *Circuits and Systems, IEEE 55th International Midwest Symposium on*, pp.1196-1199, 5-8 Aug. 2012.

[8] Low power, 8-Channel, 24-Bit Analog Front-End for Biopotential Measurements, TI ADS1298.

[9] Fen Miao; Lei Jiang; Ye Li; Yuan-Ting Zhang, "Biometrics based novel key distribution solution for body sensor networks", *EMBC 2009. Annual International Conference of the IEEE*, vol., no., pp.2458-2461, 3-6 Sept. 2009.

[10] Chenguang He; Xiaomao Fan; Ye Li, "Toward Ubiquitous Healthcare Services With a Novel Efficient Cloud Platform", *Biomedical Engineering ,IEEE Transactions on*,vol.60,no.1,pp.230-234,Jan.2013.

[11] Yu, J.Y.; Huang, D. F.; Li, Y.; Zhang, Y.T., "Implementation of MP3 player for music therapy on hypertension", *EMBC 2009. Annual International Conference of the IEEE* , vol., no., pp.6444-6447, 3-6 Sept. 2009

[12] K.M. Tham and K. Nagaraj, "A low supply voltage high PSRR voltage reference in CMOS process" *IEEE Journal of Solid-State Circuit*, vol.30, No.5, pp.586-590, May.1995.

[13] Bruce B. Winter, and John G. Webster, "Driven-right-leg circuit design," *IEEE Transactions on Biomedical Engineering*, vol.BME-30, no.1, pp.62-66, Jan. 1983.

[14] Mark JB, *Atlas of cardiovascular monitoring*, New York: Churchill Livingstone, 1998, pp.130.

[15] Liang Kai; Xu Zhang; Yuan Wang; Huang Suibiao; Guan Ning; Pang Wangyong; Li Bin; HongDa Chen, "A system of portable ECG monitoring based on Bluetooth mobile phone", *ITME 2011, International Symposium on*, vol.2,no., pp.309-312, 9-11 Dec. 2011.

[16] Single-Lead, Heart Rate Monitor Front End, ADI AD8232, 2012.