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A 13μW 87dB Dynamic Range Implantable $\Delta\Sigma$ Modulator for Full-Spectrum Neural Recording

Jian Xu, Md. Kafiul Islam, Shuo Wang, and Zhi Yang

***Abstract*— Experiment analysis on in-*vivo* data sequences suggests a wide system dynamic range (*DR*) is required to simultaneously record local field potentials (LFPs), extra-cellular spikes, and artifacts/interferences. In this paper, we present a 13 μW 87 dB *DR* $\Delta\Sigma$ modulator for full-spectrum neural recording. To achieve a wide *DR* and low power consumption, a fully-differential topology is used with multi-bit (MB) quantization scheme and switched-opamp (SO) technique. By adopting a novel fully-clocked scheme, a power-efficient current-mirror SO is developed with 50% power saving, which doubles the figure-of-merit (*FOM*) over its counterpart. A new static power-less multi-bit quantizer with 96% power and 69% area reduction is also introduced. Besides, instead of metal-insulator-metal (MIM) capacitor, three high-density MOS capacitor (MOSCAP) structures are employed to reduce circuit area. Measurement results show a peak signal-to-noise and distortion ratio (*SNDR*) of 85 dB with 10 kHz bandwidth at 1.0 V supply, corresponding to an *FOM* of 45 fJ/conv.-step.which is implemented in a 0.18 μm CMOS**

***Index Terms*— $\Delta\Sigma$ modulator, wide system dynamic range, low voltage low power design, full-spectrum recording**

I. Introduction

Growing concern for human health has stimulated the development of biomedical devices, such as neural recording chips [1]–[4]. Fig. 1 shows the main components required in a fully implantable wireless neural recording microsystem [1]. To provide on-chip signal processing and closed-loop control, an analog-to-digital converter (ADC) is required for digitizing the recorded neural data from each electrode. It is also considered as a key circuit block of the frontend circuits that is crucial to system performance. Recent researches have shown that neural data include several components: LFPs (0.1-300 Hz), extra-cellular spikes (500 Hz-10 kHz), and artifacts/interferences. The amplitude of full-spectrum neural data and artifacts/interferences varies from several μV to tens of mV. Therefore, to record full-spectrum neural data, a high precision ADC is required. The designed ADC is also desirably to consume low power and small circuit area to support implantable wireless neural recording systems.

In this paper, a new $\Delta\Sigma$ ADC implementation with an 87 dB *DR* and 10 kHz bandwidth is presented for full-spectrum neural recording. Compared with a number of recent research works [5]–[8] on $\Delta\Sigma$ ADC design, we propose a new efficient structure to support ultra-low power, low *FOM*, high resolution and low area cost: 1) MIM capacitor is replaced by high density MOSCAPs to improve area efficiency [9]; 2) to reduce power and *FOM* actively, non-opamp based techniques such as inverter-based technique are reported in [5]. However, none of them seem a perfect solution due to their design complexity and resolution restriction [10]. Thus, an opamp-based modulator structure only with MBSO technique is used to achieve ultra-low power and high precision targets.

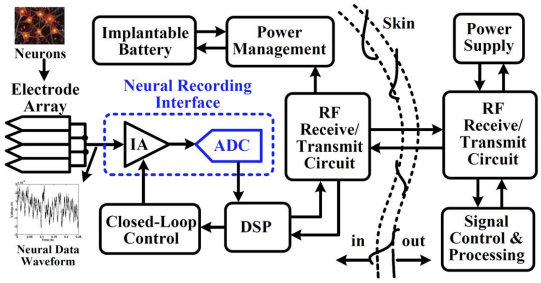

Fig. 1. Block diagram of an implantable wireless neural recording system.

To achieve high performance in the proposed MBSO architecture, several techniques are employed in this design. Firstly, the characteristics of MOSCAP types largely depend on its implementation structures. Thus, to get high area efficiency and low harmonic distortions, it is necessary to select appropriate MOSCAP types for each integrator. Secondly, to reduce power greatly, a novel power-efficient fully-clocked SO with 50% power saving and a new static power-less multi-bit quantizer with nano-watt power consuming are used. Thirdly, for in-band quantization noise improvement, a new efficient half-cycle operating resonator scheme suitable for SO technique is designed and implemented.

II. Dynamic Range Analysis

In-*vivo* neural data recorded from extra-cellular space consist of both LFPs and extra-cellular spikes, which exhibit a wide *DR* starting from several μV to tens of mV. The amplitude of extra-cellular spikes is inversely proportional to the distance between the recording electrode site and the neuron [11]. The variation can be from as low as a few μV (the recording site is about 300 μm away from the neuron) to as high as several hundred μV (the recording site is closest to the neuron). As mentioned in [11], the amplitude of LFPs is approximately between tens of μV to several mV. Moreover, artifacts and interferences that often appear in the recording experiments with freely moving or behaving animals not only misinterpret the original neural recordings but also sometimes saturate the recording electronics due to their large magnitudes (tens of mV) as shown in Fig. 2.

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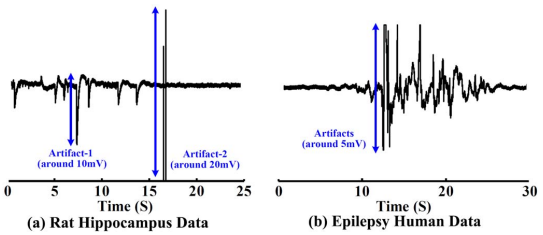


Fig. 2. Data segments in time-domain of (a) rat hippcocampus data (b) epilepsy patient data.

TABLE I

AVERAGED SYSTEM *DR* OF IN-*Vivo* NEURAL DATA

Parameter	Rat Hippocampus (0.1 Hz-10 kHz)	Epilepsy Patient Data (0.5 Hz-9 kHz)
Sequence Number and Length	134 (15 min)	64 (18 min)
DR without Artifacts	69.01±2.10 dB	34.45±3.42 dB
DR with Artifacts	82.44±4.21 dB	64.36±3.42 dB
Increase in *DR*	13.43 dB	29.90 dB

To study the required system *DR* to accommodate artifacts /interferences, we have analyzed neural data recorded from different setups: 1) Rat hippocampus recording sampled at a 40 kHz clock; 2) Full-spectrum recording from epilepsy patients sampled at a 32 kHz clock. Table I summarizes the averaged system *DR* with/without artifacts from different data sequences. Here, the circuit noise of the frontend amplifier is supposed to be 2 μVrms [12]. Based on the experimental results as shown in Table I, the system *DR* with artifacts reaches more than 80 dB. As a result, to get a minimum 10 dB *SNDR* at all frequencies, an ADC with a resolution up to 14-bit is needed for full-spectrum recording, which can be also verified from the power spectrum of neural data that is plotted against amplifier circuit noise floor [12] and ADC noise floor in Fig. 3.

III. MBSO MODULATOR DESIGN AND IMPLEMENTATION

A. *MBSO Based Modulator Topology*

Fig. 4 shows a proposed 4th-order fully feed-forward MB-SO based $\Delta\Sigma$ modulator topology with a 9-level quantization and an over-sampling ratio (*OSR*) of 32. To achieve high precision at a low power target, MB quantization technique and a local resonator with a coefficient of 1/50 are employed to reduce in-band quantization noise. As described in [13], the amplifier in a switched-capacitor (SC) integrator can be powered off after each integrating phase. Hence, SO technique is used to further optimize power consuming by turning the amplifier off during each sampling phase. Half-delay integrators are adopted on the demand of SO technique. In addition, a pseudo data weighted averaging (DWA) is used to suppress harmonic distortions causing from capacitance mismatch in the feedback digital-to-analog converter (DAC). Substantial signal processing time is given to guarantee system stability. For example, MB quantizer and pseudo DWA operate normally during Φ_1 while the feedback DAC converts the digital quantization signals in the first integrator during Φ_2 , where Φ_1 and Φ_2 are two non-overlapping clock signals, generating from sampling clock Φ_S. Thus,

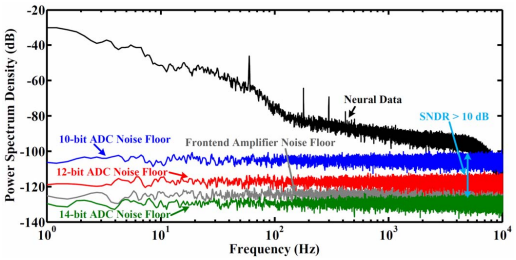


Fig. 3. Power spectral density of neural data, amplifier circuit noise floor, and ADC noise floor.

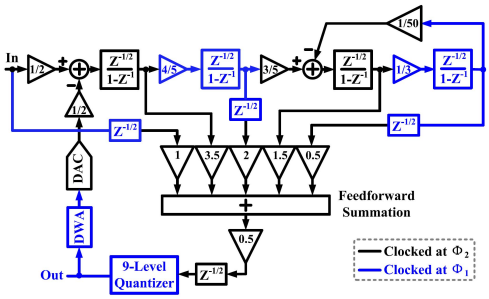


Fig. 4. Block diagram of the proposed MBSO based $\Delta\Sigma$ modulator.

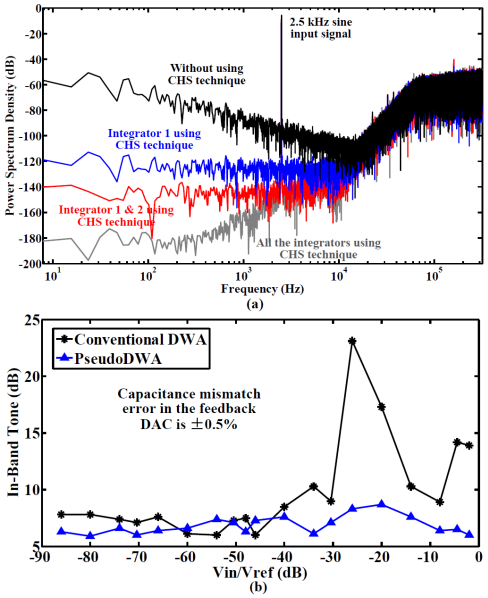


Fig. 5. (a) the simulated output spectrum of the proposed modulator with CHS technique in each integrator (b) the simulated in-band tone performance with pseudo DWA technique

the proposed MBSO modulator topology is supposed to be suitable for ultra-low power high-precision applications [13].

B. *Analysis of Non-ideal Factors*

To achieve high noise performance over the required bandwidth from 1 Hz to 10 kHz, 1/f noise has to be removed. Chopper stabilization (CHS) technique and correlated double sampling (CDS) technique are two widely used solutions for low frequency noise cancellation and DC offset removal [14]. However, CDS technique is not suitable for SO technique because it requires the amplifier to be powered on continuously over the complete clock cycle. Hence, CHS technique that is suitable for SO technique is used due to its simple circuit implementation. Fig. 5 (a) shows the modulator output spectrum after employing CHS technique in each integrator

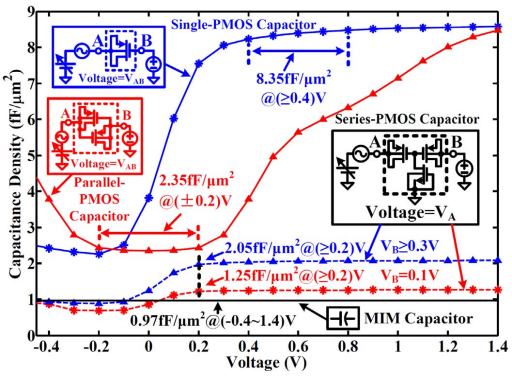


Fig. 6. Simulated C-V curves of the proposed MOSCAPs in 0.18 μm CMOS.

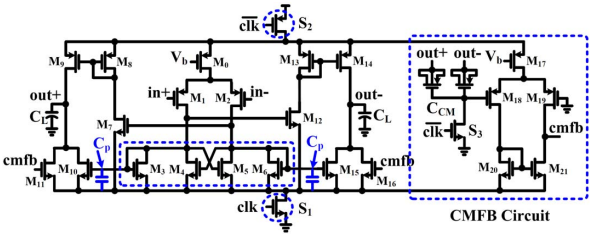


Fig. 7. The proposed fully-clocked power-efficient SO structures with the corresponding CMFB.

when considering 1/f noise in all the integrators. Through comparative simulation results, 1/f noise in the last three integrators is negligible for 14-bit resolution achievement. Thus, CHS technique is only adopted in the first integrator to reduce the effect of 1/f noise. Fig. 5 (b) shows the in-band tone performance with a capacitance mismatch error of $\pm$0.5 % in the feedback DAC. Compared with a conventional DWA, pseudo DWA can effectively suppress in-band tones with different input signal power, and the peak amplitude of harmonic distortions is only 8 dB higher than the ADC noise floor.

C. High Density MOSCAPs

As to area efficiency, MOSCAPs are preferred because of their high capacitance density [9]. However, the MOSCAP structures suffer greatly from parasitics that lead to harmonic distortions. The simulated capacitance-voltage (C-V) curves of the proposed three MOSCAPs in a 0.18 μm CMOS process are given in Fig. 6. It is shown that single-PMOS type in accumulation region is able to provide high density (8.45 fF/μm^2) with moderate bias voltage (0.4-1.4 V) and poor linearity (<4.1 %). Parallel-PMOS type in depletion region combines moderate density (2.35 fF/μm^2) with narrow bias voltage ($\pm$0.2 V) and moderate linearity (<3.5 %). Series-PMOS type in accumulation region has moderate density (2.05 fF/μm^2) with wide bias voltage (0.2-1.4 V) and good linearity (<2.8 %) when V_B is larger than 0.3 V. In contrast, the density of MIM capacitor is just 0.97 fF/μm^2 although it supports a wide bias voltage range (-0.4-1.4 V) and has a good linearity (<0.1 %).

D. Implementation of Switched-Opamp and MB Quantizer

The implementation of a power-efficient SO is crucial to an ultra-low power modulator design. Fig. 7 shows the

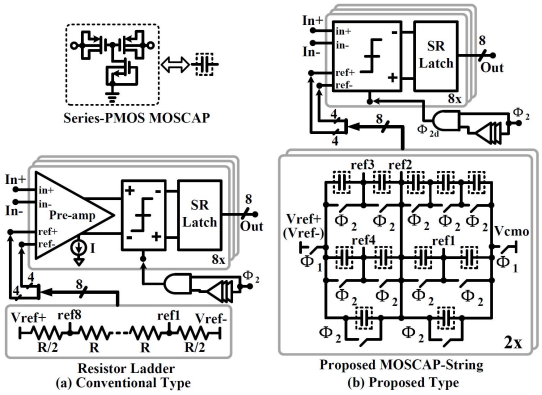


Fig. 8. The circuit schematic of 9-level quantizers. (a) conventional type (b) proposed type.

circuit implementation of a proposed high power-efficiency fully-clocked current-mirror SO structure. The proposed SO is a load-compensated single-stage OTA with a Class-AB output stage and provides higher power efficiency than two-stage one. Besides, a cross-coupling structure is used to ensure enough voltage gain and fast recovery from off-state. Although it introduces a large parasitic capacitor C_p and noise (mainly 1/f noise) without effective suppression, high performance could be achieved by selecting appropriate SOs for each integrator. To efficiently save power, S_1 and S_2 are adopted to turn SO off fully during the sampling phase.

Implementation of an area and power efficient MB quantizer is also very challenging in this design. As described in Fig. 8 (a), one common solution is to use a flash ADC consisting of a resistor ladder and 8 dynamic comparators with pre-amplifiers. This architecture is not preferred because large area and static power are consumed by comparators and resistor ladder. To remove static power and improve circuit area efficiency, Fig. 8 (b) gives the proposed MB quantizer structure consisting of 8 dynamic comparators without pre-amplifiers and only 2 combinations of MOSCAP-strings. Here, MOSCAP-strings are introduced to generate the required voltage reference instead of resistor ladder. Also, appropriate clock signals with the corresponding delayed versions are employed to avoid glitch and guarantee system stability. Based on the simulation results, the proposed quantizer saves 96 % power and 69 % area over the conventional structure; random offsets with a standard deviation of up to 0.4 LSB can be tolerated easily in this structure when achieving a 14-bit resolution. Thus, the proposed quantizer is more suitable for ultra-low power high performance applications.

E. Complete Modulator Circuit

Fig. 9 shows the simplified circuit schematic of the proposed modulator. To avoid harmonic distortions by capacitor non-linearity, MIM capacitor is used as the sampling capacitor in the first integrator that is split up into 8 unity capacitors. The feedback DAC is implemented by connecting the bottom terminal of each unity capacitor to either V_{ref+} or V_{ref-}. Series-PMOS capacitors are adopted in the feed-forward summation to meet the requirement of wide input signal range (full scale) and large output swings. Moreover,

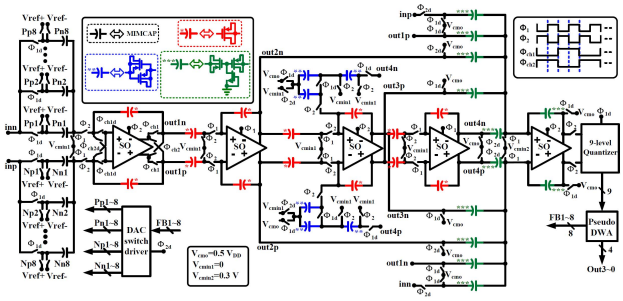
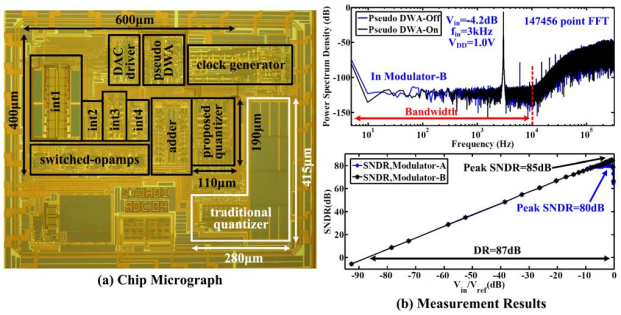


Fig. 9. Circuit implementation of the proposed 4th-order MBSO modulator.



(a) Chip Micrograph (b) Measurement Results

Fig. 10. (a) chip micrograph (b) measurement results.

a novel area and power efficient resonator scheme applicable to SO technique is adopted to realize an accurate coefficient of 1/50 with parallel-PMOS capacitors [13]. As to other integrators, single-PMOS capacitors are employed to reduce chip area effectively. Compared with only MIM capacitor design, 55 % capacitor area is saved in the proposed modulator. CHS technique with another two non-overlapping clocks Φ_{ch1} and Φ_{ch2} is used in the first integrator to suppress the effect of 1/f noise. In order to avoid charge injection, the delayed versions (Φ_{1d}, Φ_{2d}, Φ_{ch1d} and Φ_{ch2d}) of the clocks used in this design are developed. For comparison purposes, both traditional quantizer used in Modulator-A and proposed quantizer used in Modulator-B are designed as shown in Fig. 8 to implement a 9-level quantization. DAC switch driver is used to reduce the number of feedback signals.

IV. Measurement Results

The designed modulator is fabricated in a 0.18μm CMOS. Fig. 10 (a) shows the chip micrograph and Fig. 10 (b) gives the measurement results at 1.0 V supply and 640 kHz clock. The output spectrum of the proposed modulator (Modulator-B) clearly shows that pseudo DWA can effectively suppress harmonic distortions. The measured peak *SNDR* and *DR* are 85dB and 87dB, respectively, while it only dissipates 13 μW and 0.25 mm^2 area with a *FOM* of 44.7 fJ/conv.-step. The bandwidth is 10 kHz. Table II gives the performance comparison with published works. The *FOM* of the designed modulator is lowest even compared with opamp-less based modulators.

V. Conclusion

To simultaneously record LFPs, extra-cellular spikes and artifacts/interferences, an ADC with a resolution of 14-bit or more is demanded. This paper presents the design and implementation of a high-precision area-efficient MBSO based $\Delta\Sigma$ modulator for full-spectrum neural recording. By using fully-clocked power-efficient SO, zero-static power quantizer and high-density MOSCAPs, the designed chip only consumes a 13 μW total power and 0.25 mm^2 area at 1.0 V supply.

TABLE II

Performance Summary and Comparison

Modulator	[8]	[7]	[5]	This Work
Process (nm)	180	180	180	180
Integrator Type	opamp	opamp	Inverter	SO
V_{DD} (V)	1.0	0.9	0.7	1.0
f_s (MHz)	4	5	4	0.64
Bandwidth (kHz)	20	10	20	10
Power (μW)	140	200	36	13
DR (dB)	88	83	85	87
SNDR (dB)	81	80	81	85
FOM (fJ/conv.-step)	381.7	1223.5	98.1	45

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