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Towards On-Chip Integration of Brain Imaging Photodetecors Using Standard CMOS Process*

Ehsan Kamrani, *Member IEEE,* Frederic Lesage, and Mohamad Sawan, *Fellow IEEE*

***Abstract*—The main effects of on-chip integration on the performance and efficiency of silicon avalanche photodiode (SiAPD) and photodetector front-end is addressed in this paper based on the simulation and fabrication experiments. Two different silicon APDs are fabricated separately and also integrated with a transimpedance amplifier (TIA) front-end using standard CMOS technology. SiAPDs are designed in p+/n-well structure with guard rings realized in different shapes. The TIA front-end has been designed using distributed-gain concept combined with resistive-feedback and common-gate topology to reach low-noise and high gain-bandwidth product (GBW) characteristics. The integrated SiAPDs show higher signal-to-noise ratio (SNR), sensitivity and detection efficiency comparing to the separate SiAPDs. The integration does not show a significant effect on the gain and preserves the low power consumption. Using APDs with p-well guard-ring is preferred due to the higher observed efficiency after integration.**

I. Introduction

Chip-level integration provides higher performance with less required system components, less power density and power consumption. Integration offers more reliable and lower cost systems that are easier to manufacture and maintain. It reduces the design complexity by offering lower communication latency and eliminating generalized transactional interfaces that are typically used when modules communicate across chip boundaries. To increase the use of optical sensor based systems for state-of-the-art biomedical applications, integration of the image sensor and the high-speed peripheral circuitry on the same chip using complementary metal-oxide-semiconductor (CMOS) technology is highly desired [1]. Figure 1 shows block diagram of a functional near infra-red spectroscopy (fNIRS) which offers a non-invasive, low-cost and portable optical technique for real-time and long-term brain imaging applications. The most critical building block in this system is the photodetector front-end. Due to the large size of the photodiode and front-end circuitries required for detecting, amplifying and filtering the incident light in this block, it usually suffers from high-noise, high-power consumption and low-spatial resolution. The main components of photodetector front-end are the photodiode and amplifier.

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E. Kamrani and M. Sawan are with Polystim Neurotechnologies Lab., Electrical Engineering Dept., Polytechnique Montreal, QC, Canada. (e-mail: {ehsan.kamrani, mohamad.sawan}@polymtl.ca).

F. Lesage is with Optical and molecular imaging Lab., Elec. Eng. Dept., Polytechnique Montreal, Canada. (e-mail: frederic.lesage@polymtl.ca).

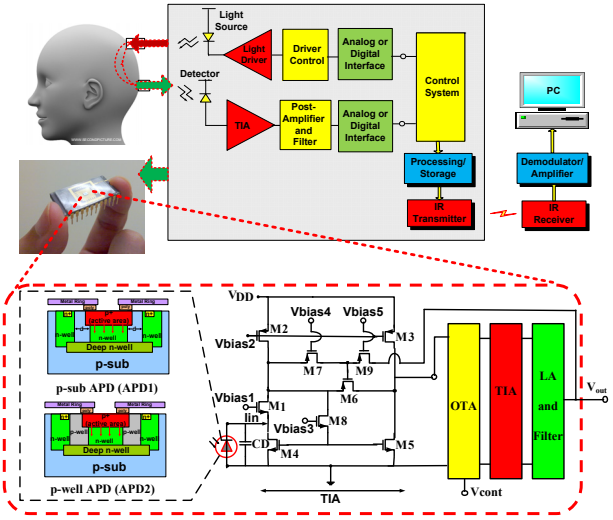

Figure 1. Block diagram of the proposed brain imaging front-end.

The photodiode used in the photodetector requires being highly sensitive, enabling the reliable conversion of the ultra-low amplitude light signal into a detectable electric signal. Silicon avalanche photodiode (SiAPD) is a candidate for low-level light detection (especially in the visible and near-infrared regions) due to its bias dependent internal gain and its ability to amplify the photogenerated signal by avalanche multiplication [1]. SiAPDs have been commercially available for more than 35 years normally with a dedicated process, which is highly expensive and do not allow monolithic integration with other electronic circuitry. To overcome these problems, researchers have investigated the design and fabrication of SiAPDs in a standard CMOS process. The advantages of standard CMOS fabrication process are: the availability of a fully supported, mature and reliable technology at reasonably low cost, and the possibility of developing a complete system on chip with a high degree of complexity [2]-[3]. The mandatory requirement for SiAPD fabrication in standard CMOS process is that a suitable subset of CMOS fabrication process flow should be able to build a planar p-n junction without device breakdown at the photodiode periphery [4]. It is challenging to make SiAPDs in CMOS technology due to lack of special fabrication steps and optimizing the performance of both the CMOS devices and the SiAPD is a non-trivial job. Several research groups have fabricated SiAPDs using standard CMOS technology [5]-[10] and also integration of the APD with TIA front-end [4]-[5]. Although due to their relatively high-power consumption and low sensitivity and SNR characteristics [11]-[12] their

performance is still far from the one obtained with commercial APDs. We have already designed new p+/n-well miniaturized, low-noise and high-gain SiAPDs with high-detection efficiency and low-breakdown voltage in standard 0.35µm CMOS technology [6]-[7], and a low-noise, high-gain and low-power TIA front-end for low-intensity light detection applications [1], [6]. In this paper we have implemented and characterized an integrated circuit includes SiAPDs and TIA front-end, fabricated using standard CMOS process. The effects of on-chip integration and its impact towards implementing on-chip, low-noise and low-power photodetectors for real-time brain imaging are introduced.

II. CMOS Photodetector Design

Here we have designed the p+/n-well SiAPDs [6]-[7] with guard ring in two different square and octagonal shapes implemented using relatively low-doped layers available in standard 0.35µm CMOS technology. Schematic of the cross-section and plan view (not to scale) of the proposed SiAPDs are depicted in Fig. 1. In p-sub ring APD (APD1), the guard-ring is realized by low doped n-ring due to n-wells lateral diffusion. The n-well is splited into two n-tubs separated by a small interval (d≈0.9µm) constituting the guard-ring. We have developed this APD with two different active areas of 100µm×100µm and 400µm×400µm. The p-well ring APD (APD2) is also a p+/n-well APD developed in square and octagonal shape (with active area of 100µm×100µm) with guard ring realized by low doped p-well around p+ active area to preventing premature edge breakdown (Fig. 1). Optimization of the performance of SiAPD is done by device level simulation using Sentaurus TCAD software. The active junction of the photodiode exists between p+ (Na = $5\times10^{19}/cm^3$) and deep n-well (Nd = $1.28\times10^{17}/cm^3$). One of the main difficulties for optimal CMOS APD design and fabrication is the technological constraints imposed by CMOS chip manufactures (e.g. AMS, IBM and TSMC). Manufactures do not give out doping profile information for their technologies. Referring to the applied technology layers doping and depth characteristics, we can point out the weak depths and the high doping values applied in the technology. In some fabricated APDs there was a discrepancy between the simulated and measured parameters, especially regarding to the photon detection efficiency (PDE) and dark current. This could be due to the inadequacy of the applied device simulation tool and inflexibility of the standard CMOS technology regarding to the precise simulation and implementation of the considered characteristics. The output impedance of the SiAPD should be considered for impedance-matching with the integrated front-end amplifier. The output impedance of APD2 under reverse bias is around 0.5Ω and for the APD1 is around 600Ω. The capacitance of the photodetector increases with its area with measured values being 1pF for a 100µm² SiAPD and 32 pF for 400µm² SiAPD. For APD1 and APD2 the breakdown happens at approximately 9V and 6V respectively. In order to find out if the source of the breakdown is avalanche or it is due to the tunnelling we have measured the breakdown variation in different temperatures. The value of temperature coefficient of the breakdown voltage is positive for diodes with avalanche breakdown and negative for diodes with tunneling breakdown [8].

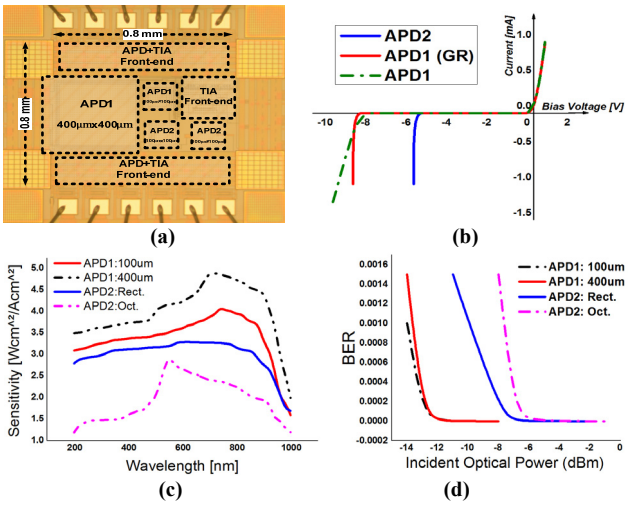

Figure 2. The microphotograph of the fabricated chip (a), the I-V characteristics (b), Sensitivity (c), and bit error rate (d) of the SiAPDs.

The microphotograph of the fabricated chip using standard CMOS technology is shown in Fig. 2. The SiAPDs have been characterized more and evaluated individually. The I-V characteristics and sensitivity of the SiAPDs are depicted in Figures 2(b)-(c). The bit error rate (BER) affecting the photodetector sensitivity and speed, is also characterized in different incident powers (Figure 2 (d)). For the wavelength specific applications also the spectral sensitivity of the detector should be considered. The sensitivity is calculated as the photocurrent per unit area of the photodiode for a given irradiance and it shows the peak sensitivity in near-infrared region for all proposed APDs.

III. CMOS TIA Front-end Design

The proposed TIA front-end, shown in Fig. 1, is formed by four stages. The first stage TIA provides a very low input resistance to handle the large photodiode capacitance (up to 5 pF) and the second TIA is also the same as the first TIA block. Using distributed gain concept in TIA front-end design increase the GBW of the circuit and allows changing the gain of the amplifier without varying the BW. We have used this fact in order to make the intensity of the photoreceptor independent to the BW variation. This new structure offers a low-noise, high-gain and high-BW TIA [1], [9]. Furthermore we have proposed using dynamic threshold voltage metal-oxide-semiconductor field-effect transistor (DTMOS) in this TIA structure in order to enhance the differential input common-mode range (ICMR). The design consists of a current amplifier implemented in a transimpedance configuration. In this circuit (Fig. 1), we have used the combination of three transistors (M6, M7 and M9) to work as a feedback resistor to minimize the output ripple and reduce the drained current. M7 and M9 biased in the linear region. Bandwidth of TIA increases by decreasing the photodiode capacitance (C_D≈1pF). In order to boost the voltage swing and match the output impedance to drive the photoreceiver output, we designed a Limiting Amplifier (LA) [6] and an operational transconductance amplifier (OTA) to be added to the output of the TIA. The OTA used in the proposed front-end amplifier design is a current-mirror OTA, which is modified from the OTA reported in [10]. Performance of this

OTA highly depends on the bias current and the sizing of the transistors. So we have considered these two parameters in order to reach best performance. To increase the maximum output swing, and improve the stability of the circuit, we have also used a filtering block followed by TIA and LA. In the TIA, the transistors M2-M1 form a two-pole shunt negative-feedback loop that reduces the equivalent M2 source resistance. Because one of the main requirements of biosignal amplifiers is to have a wide dynamic range, here in order to achieve wide dynamic range, we have considered a photoreceiver circuit with the ability to tune important parameters. This is preferred to using output signal limiting and input current steering techniques to extend the dynamic range of amplifier. Using the constant applied voltage of V_{cont} $(0V < V_{cont} < 2V)$, the Gain, BW, power-consumption and dynamic range of the output can be changed to achieve a wide output range. We also need low input-noise for high signal quality. Due to the low-frequency behavior of the signals, in-band noise of the readout is dominated by 1/f noise. The proposed TIA shows ultra-low input noise characteristics. This shows the efficiency of the applied topology and using DTMOS accompanying with optimal transistor scalling based on the sensitivity analysis. We used Cadence Virtuoso schematic and layout editors to design and simulate our proposed TIA in 0.35µm CMOS technology. In order to optimize the performance of the amplifier, we analyzed the sensitivity of each circuit component on the output and the best values for optimal sizing were selected. For TIA:$Z_{in,dc} = 500\ k\Omega, V_{in,dc} = 0.5\ V$ and for the total front-end: $Z_{in,dc} = 300\ \Omega$, $V_{in,dc} = 3\ mV$. By varying the V_{cont} in proposed variable-gain front-end, between 0-1.5 V, we reached the very-high and fixed value of 45×10^9 for gain-bandwidth product (GBW). This value is tuneable between 10M and 45G for various applications. We can reach the transimpedance gain in the range of 2-400 MV/A and BW in the range of 1.7-5MHz using this configuration. The maximum power consumption of this circuit is 3.5 mW, making it usable for biomedical wireless and portable applications. In order to validate the robustness of the circuit performance against power supply variation we have examined the TIA front-end characteristics for the supply voltages vary between 1-3.3V. The sensitivity is calculated as:

$$S = (Q/R) \times (qQB + \sigma_T) = (\lambda Q_e) \times (1/1240) \times 100\% \quad (1)$$

where S is sensitivity, Q_e is the quantum efficiency, Q is desired Q factor, R is the photodiode responsivity, q is charge of an electron, B is receiver bandwidth and σ_T is the rms thermal noise current and is given by:

$$\sigma_T^2 = (4k_B T / R_L)\ F_n B \quad (2)$$

where k_B is Boltzmann's constant, T is temperature, R_L is the receiver load resistance and F_n is the receiver noise factor. Due to the specific wavelength design consideration [1], [12] to reach maximum sensitivity to the red/infra-red light, the octagonal APD2 offers a better sensitivity (with the cost of significantly higher noise factor and after-pulsing) comparing to other APDs.

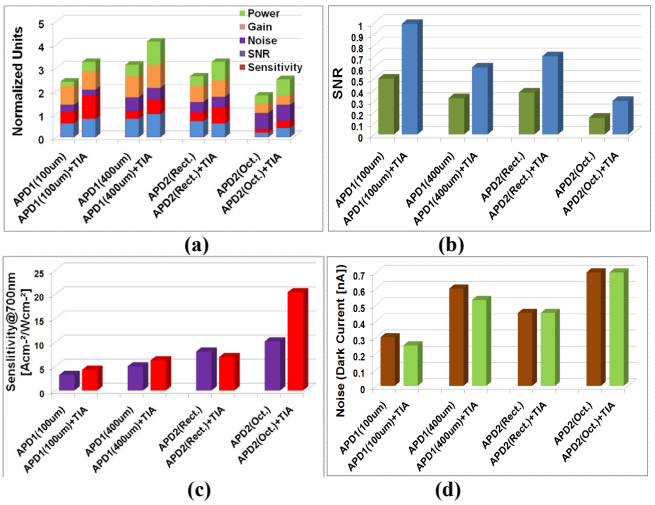

Figure 3. Comparison the impact of integration on different parameters (a), the impact of integration on SNR (b) and sensitivity (c), the dark current noise of the CMOS integrated photoreceiver and separate CMOS-APDs (d).

TABLE I. THE GENERAL CHARACTERISTICS OF THE IMPLEMENTED INTEGRATED SIAPDS + TIA

Circuit / Parameter	TIA+APD1		TIA+APD2		[4]	[5]
	Rectang	Rectang.	Rectang.	Octag.		
CMOS Tech.(µm)	0.35	0.35	0.35	0.35	0.18	0.13
SupplyVoltage(V)	3 V	3 V	3 V	3 V	1.8	1.3
APD Guard-Ring	p-sub	p-sub	p-well	p-well	n-well	p-well
APD Gain (M)	20	100	45	15	-	-
APD Area (µm)	100×100	400×400	100×100	100×100	-	-
Sensitivity (dBm)	-4.3	-2.2	-6	-22	-19	-5.5
Vbr (V)	9	9	6	6	-	-
Power diss. (mW)	5.12	2.31	0.91	1.16	50	21.6
Max TIA Gain	249M	245.01M	248.6M	248M	-	
BW (MHz)	1200	1643	1420	1006	-	-
Data Rate (Gb/s)	5.68	3.31	4.17	2.4	3	4.25
Log(BER)	-13	-13	-12	-11	-11	-12

IV. APD+TIA INTEGRATION

Here the proposed SiAPDs and TIA front-ends have been integrated on the same chip and the measurements results regarding to this integration are shown in Table 1. The final layout of the designed integrated circuit after post-layout simulation and optimization was fabricated by TSMC via CMC Microsystems. This 18-pin IC has the die size of 1.5mm×2mm, and includes 2 different APDs and the proposed amplifier. Comparing to the integrated circuits proposed at [4]-[5], this design offers the highest transimpedance gain (~10k higher) and the lowest power consumption (~10 times lower) and input/output noises (~1k lower) accompanying with a suitable gained performance regarding to the APD-TIA on-chip integration. The impact of integration on different parameters is depicted in Fig.3 (a). The values of each parameter are scaled down to normalized values between 0-1 for better comparison of the variation of different parameter. It shows a more significant effect of integration on power, SNR, and sensitivity respectively. In other words, these results show that the impact of integration is mainly on power and then on the SNR, sensitivity and noise respectively. In order to verify the impact of the applied APD structure and size on these different measured values, this comparison has been also established on different APDs.

Figs.3 (b)-(c) show the SNR and sensitivity of the different separated and integrated APDs. Regardless of a reduction in sensitivity of the rectangular APD2 (which can be due to the BW and thermal noise degradation in this structure introduced by integration), for all other integrated APD structures a significant improvement in sensitivity, SNR, noise and size are gained in integrated circuit with the cost of higher power consumption. No significant change is observed on the multiplication gain and BW.

In Fig. 3 (d) the dark current noise of the CMOS integrated photoreceiver and CMOS-APD only when Vr = 9V and incident optical power = 0 dBm are compared. While the photodetection frequency response (PFR) for the proposed APDs is not high, the integration improves the PFR significantly. As the reverse bias voltage is increased, the photodetection frequency response increases because of increased avalanche gain. Optimization of the CMOS-APD utilizing RF-peaking can enhance photodetection 3-dB bandwidth while maintaining sufficient avalanche gain. The maximum 3-dB bandwidths for the integrated circuit of APD1+TIA and APD2+TIA are around 3.79 GHz and 2.78 GHz respectively at the reverse bias voltage of 10.6V. Integrated circuit specially regarding to the square APD2 has better BW performance than APD1. However integration has no significant effect on the gain of TIA but reduces the input referred current noise as depicted in Figs. 4 (a)-(b). As shown in Figs. 4 (c)-(d), comparing with other works, the proposed integrated circuit shows lower power consumption and noise-level and higher sensitivity with no degradation in data-rate. However work is still in progress in order to improve the power and data-rate characteristics and increase the speed of the photodetector front-end.

V. Conclusion

The main effects of on-chip integration of APD and TIA front-end were addressed in this paper. We have developed two new p+/n-well SiAPDs with p-well and p-sub guard-rings for premature edge breakdown prevention. Proposed rectangular and octagonal SiAPDs have the avalanche gain of 100 and 45 with the breakdown voltage of 9V and 6V and the photon absorption efficiency of 45% and 25% at 800nm respectively. A high gain (up to 250MV/A), tunable BW (1kHz-1GHz), extremely low input and output noise (100fA/√Hz, 1.8μV/√Hz), high stability (phase margin≥40°), and low-power consumption (0.8mW) TIA front-end also implemented using standard 0.35μm CMOS technology. The SiAPDs then have been integrated on-chip with TIA front-end and their characteristics are evaluated. The on-chip integrated APDs with the proposed TIA preserves the high-performance characteristics of both APDs and TIA while offering a more miniaturized photodetector front-end dedicated to low-intensity light detection applications. The integration improves the SNR, sensitivity, fill factor (FF) and PFR with no significant change in power and gain values. Using APDs with larger active areas and applying p-well guard-ring is also preferred due to the higher observed efficiency after integration.

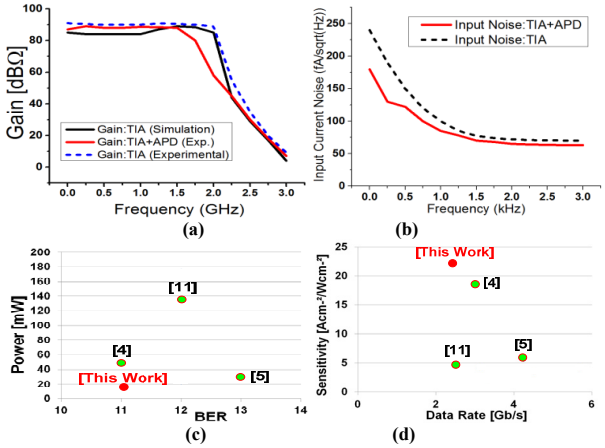

Figure 4. Comparison of gain (a) and input noise (b) characteristics of the integrated and separated TIA front-ends, Comparison of the power-BER (c) and sensitivity-data rate (d) of the proposed front-end with other works.

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