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Low Noise and High CMRR Front-End Amplifier Dedicated to Portable EEG Acquisition System

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Abstract— **This paper concerns the design and implementation of a fully integrated low noise and high CMRR rail-to-rail preamplifier dedicated to EEG acquisition channel. The preamplification technique is based on two complementary CMOS True Logarithmic Amplifier (TLA) stages connected in parallel. The TLA largely amplifies small amplitude of EEG signals, and moderately the large amplitude ones created during epileptic. A chopper stabilization technique is used to filter the 1/*f* noise and the DC offset voltage of the input CMOS transistors and to increase the common-mode rejection ratio (CMRR). Due to the TLA structure, a high CMRR and high power supply rejection ratio are achieved and the signal-to-noise ratio (of the channel is better enhanced). To snugly fit the ADC input window to the EEG signal magnitude a new programming gain approach is implemented. Also, a chopper spike filter is used to cancel the spike voltages generated by the charge injections of modulator/demodulator switches. The proposed preamplifier is implemented in 0.18 µm CMOS technology. Post-layout simulation results exhibit 253 dB @50/60 Hz as CMRR, 500 nVrms @100 Hz as input-referred noise while consuming 55 µA from a 1.8 V supply.**

I. Introduction

The Electroencephalogram system in today's science is used to long term monitoring the electrical activity of the brain which is based on a non-invasive and painless diagnostic test. The Electroencephalography is the measurement of this electrical activity by means of placing several electrodes on the head (scalp) around the brain. The potential difference between certain electrodes is measured and converted into waveform called EEG signal [1-2]. The recorded EEG signals are used to evaluate of brain disorders or epilepsy.

Recently, there is an increasing demand on the miniaturized for low-power and low noise bio-potential acquisition system in order to avoid bulky connectivity and mains-power instruments that reduce patients mobility and create discomfort [3]. Also, this will influence the recording data time, the monitoring continuity and the illness diagnosis.

However EEG signals are not easily obtained because they are extremely weak signals, in the range of 1 to 160 µVpp and they are band limited to a very low frequency range from 0.1 to 100 Hz [3]. Due to these characteristics, the EEG acquisition system susceptible to ambient noise (50/60 Hz common-mode interference signal coupled to human body from the mains), to amplifier flicker noise (1/f) and DC offset, to problem of electrode DC offset generated at the skin–electrode interface and between electrodes.

This can lead to the saturation and decrease the CMRR of the readout front-end that defines the quality of the extracted signal [2,3]. Therefore, in order to extract high-Resolution EEG signal under these circumstances, low-power, low noise and high CMRR & PSRR readout front-end is needed to meet the standards for the digital recording of clinical EEG and to increase battery life [3].

In this paper, we present a low-noise and high CMRR rail-to-rail Chopped Logarithmic Programmable Gain amplifier (CLPGA) dedicated to EEG acquisition channel. Section II presents the block diagram of the proposed EEG acquisition channel. The CLPGA is the subject of section III, post-layout simulation results are in section IV, and conclusions are in section V.

II. Analog Front-End Architecture Overview

General front-end of EEG acquisition systems were realized with extensive passive components to suit biopotential request and as the EEG system needs to support growing of the channel numbers, the integrations of the passive elements in chip via CMOS technology becomes the greatest solution [3]. Figure 1 shows the conventional CMOS Bio-potential acquisition channel that usually consists of electrodes, a protection circuit, an instrumentation amplifier (IA), a high-pass filter, a low-pass variable gain amplifier, a Right Leg Driver circuit (RLD) and an analog-to-digital converter (ADC) [2-4]. Due to the very small voltage EEG signal amplitudes of less than 100 µV, the EEG channel has to provide for post-processing task a stable programmable ac gain from 200 to 10000 V/V [4].

Each channel will take a potential signals from two electrodes. It will send them through low input referred-noise and DC offset, low gain, and high CMRR IA to be differentiated and amplified.

A high-pass filter is used to cut all signals less than 0.1 Hz. A low-pass variable gain amplifier that makes further amplification of the EEG signal to snugly fit an ADC input window and cut-off all frequencies above 100 Hz. After filtering the incoming signal to fit into the EEG band, a high resolution ≥ 20 kSPS ADC digitizes the EEG signal for digital signal processing. Finally, Right Leg Drive circuit is used to cancel the 50/60 Hz common mode interference signal coming from the power supply and fluorescent light. In order to perform very high signal to noise ration of EEG channel and to reduce the input offset voltages due to the effect of electrodes mismatch and CMOS transistor process

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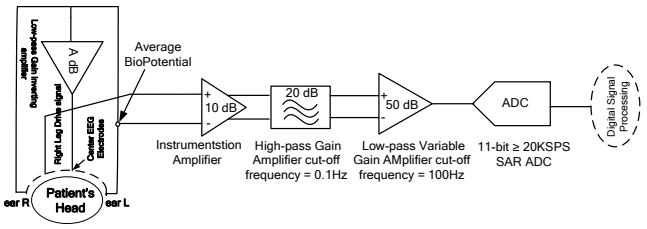


Fig. 1. Block diagram of the conventional EEG acquisition channel

variation, a low input referred noise and very high CMRR and PSRR as well as a low power and small silicon area EEG channel architecture is proposed in this paper.

The proposed architecture is shown in figure 2; it consists of a Chopped Logarithmic Programmable Gain Amplifier as preamplification stage. A high-pass amplifier provides a fixed gain of 50 dB and cut all EEG signal with frequencies lower than 0.1 Hz. A 14-bit 50 kSPS low-pass second order Sigma-Delta modulator that combines the standards low-pass filter and the ADC. It is used to cut-off EEG signal with frequencies higher than 100 Hz and to digitize the preamplified signal. These characteristics can maximize the number of available quantization steps thus reducing the error levels (quantization noise) and increase SNR ≥ 100 dB.

III. Implementation of the Proposed CLPGA

Typically, the preamplifier of the EEG channel is based on a low gain, low noise instrumentation amplifier that consists of three operational amplifiers and several matching resistors to achieve high CMRR. But, there are some major drawbacks in this type of topologies such as high power consumption and too many resistors, which reduce the battery operating time and increase the area cost respectively as well as it represent a source of noise and low precision amplification [5]. Recently, AC-coupled chopped IA based on current feedback circuit and CMOS differential difference amplifier (DDA)-based noninverting IA have been presented [4, 6]. The main drawback are the passive resistors and transconductance amplifier used in the feedback which constrained the mentioned IAs by high noise (which needed large transistor sizes) and have an CMRR that just meets the minimum specification of 80dB. In order to strongly amplify the small EEG signals and to moderate the larger one created during epileptic crises and to cover EEG signals which have a dynamique range of 80 dB [5,6], a rail-to-rail logarithmic programmable gain amplifier (CLPGA) is presented in this paper to replace the standard IA.

It is based on true logarithmic amplifier topology where the phase shift or delay doesn't vary with input signal level [7]. It consists of a cascade of a three rail-to-rail low dual gain stages, each complementary stage (P or N type transistors) has a total gain of 13 dB and consists of 2 parallel blocks: Limiting amplifier & Unity gain amplifier (Figure 3). The outputs of these two amplifiers are tied to an analog node.

Figure 4a) shows the output voltage of one low dual-gain stage which can be written as equ. (1):

$$\text{For } V_{EEG} < V_{iL} \Rightarrow V_{out} = (A+1)*V_{EEG}$$

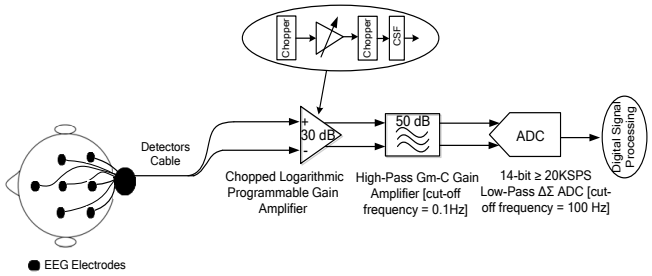


Fig. 2. The proposed EEG acquisition channel

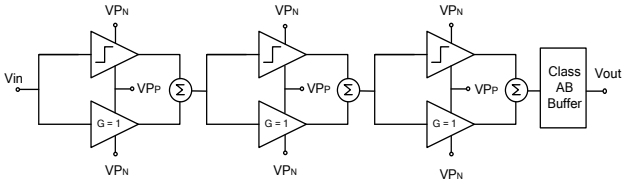
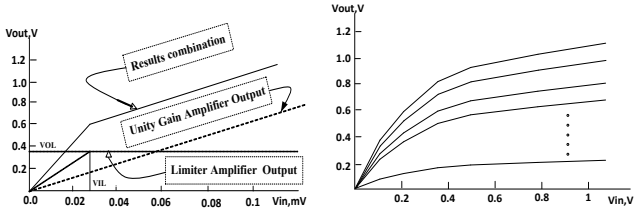


Fig. 3. Block diagram of the rail-to-rail CLPGA



(a) (b)

Fig. 4. Transfer function of: (a) one dual-gain stage, (b) n cascade programmable dual-gain stages

$$\text{For } V_{EEG} \geq V_{iL} \Rightarrow V_{out} = V_{EEG} + V_{oL} \quad (1)$$

where V_{EEG} is the EEG input signal, $V_{iL,oL}$ are the limiting input and output voltages and A is the small signal gain of the limiting amplifier . By cascading n programmable low dual-gain stages, the output waveform exhibits the characteristic that shown in figure 4b. It consists of series of straight lines with breaking points determining the stage amplification limits stage. By cascading low dual gain stage, the amplification of the input noise & offset voltage can be reduced as well as a very high CMRR and high PSRR one can obtain. A Class AB output buffer is used to perform high output swing which results in increasing of SNR of the EEG channel.

To cancel the 1/f flicker noise and DC offset of the input transistors a chopper stabilization technique is used by input signal modulation and demodulation (figure 5) [8].

The Modulator, based on CMOS switches (figure 6a), transposes EEG signal to 1 kHz chopper frequency. The CLPGA is followed by a demodulator used to return back the amplified EEG Signal to its original band and to modulate the noise to the Chopper frequency i.e. out of the EEG band.

In order to cancel the spike voltages due to charge injection in analog switches which is correlated with the amplified EEG Signal, a chopper spike filter is implemented which is triggered by 2 kHz clock signal (figure 6b). A low-

pass filter has 100 Hz cut-off frequency can be used to cancel the noise out of the EEG signal band.

To perform high charge transfer of analog switches and reduce charge injection, dummy transistor technique as well as a bootstrap circuit is designed to double the supply voltage of nonoverloping clock generator used to control the modulator & demodulator's switches (figure 5).

Figure 7 shows the schematic of one rail-to-rail programmable dual low-gain stage.

Due to the variation of the dc voltage between each signal electrode with reference electrode which can be as high as ± 300 mV [6], this CLPGA exhibits rail-to-rail characteristic.

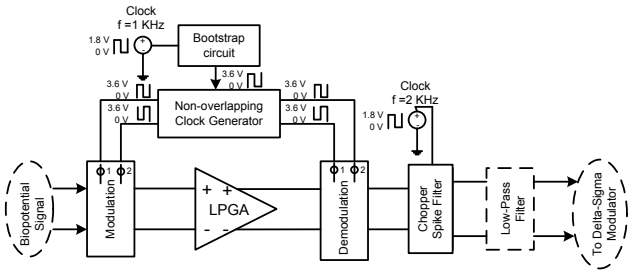


Fig. 5. The Chopped Logarithmic Programmable Gain Amplifier

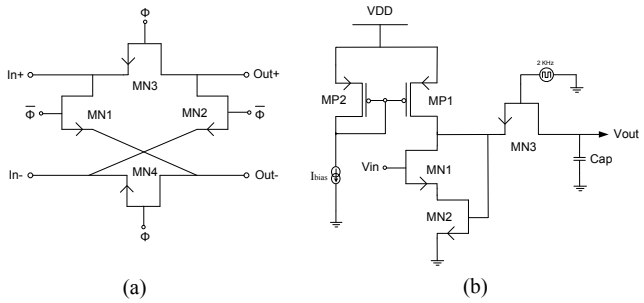


Fig. 6. Transistor level: (a) chopper stabilization technique, (b) chopper spike filter

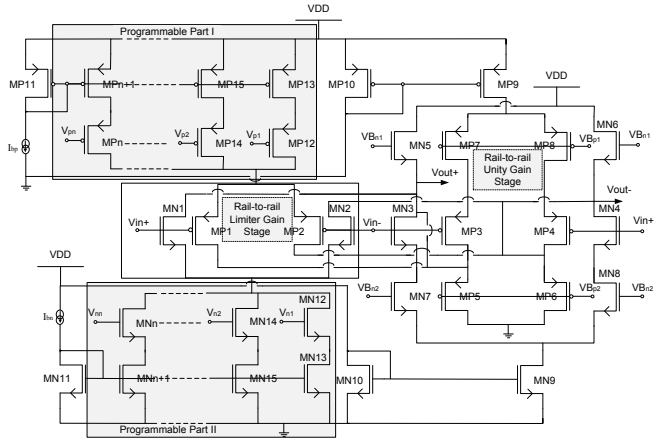


Fig. 7. Transistor level dual low-gain stage

However, to reduce input-referred noise of the CLPGA, large size of MN &MP (N & P type) input pair transistors is chosen. Noting that, the dynamic range and the precision are determined by the number of stages and their corresponding gains. Indeed, the dynamic range of one stage is equal to (A +1) where A is the gain of the limiting stage, and its value is the following: $A = \sqrt{K1/K3}$, where, K1 and K3 are the transconductance constants of MN1/MP1and MN6/MP6 respectively.

To fit EEG signal into 1 V ADC's input window, a programming approach is proposed. It is based on the variation of the tail current transistor width of each N and P input pair limiting stage simultaneously (see Figure 7 Programmable Part I & II).

IV. Results

The proposed CLPGA is implemented using standard in 0.18 µm CMOS process. The total layout area of the CLPGA including the digital part needed to program the CLPGA and the pads is 3mm^2 and the corresponding layout is shown in Figure 8. For total CLPGA, the power consumption is 99 µW which is acceptable for EEG applications.

The post-layout simulation was done with Spectre under Cadence platform. Figure 9 shows the DC transfer function of the CLPGA where for an input DC voltage of 15 mV the simulated output DC voltage is aproximated as 1.36 V_{PP}. The simulation result of figure 9 exhibits the bode transfer of the CLPGA for different gain at 1 dB step and for maximum gain of 40 dB.

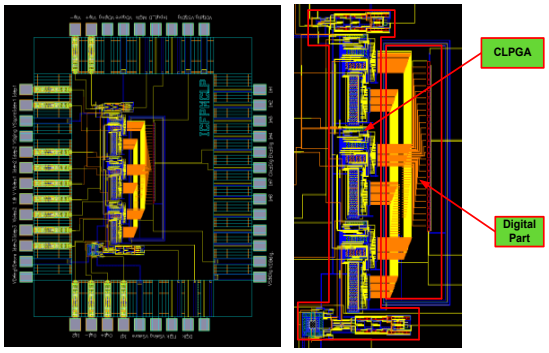


Fig.8. Layout of the proposed CLPGA: (a) Chip, (b) Core

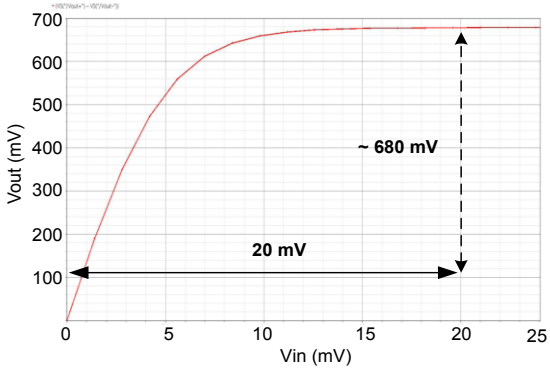


Fig. 9. Simulated Transfer Function of the CLPGA

Table 1. CLPGA main characteristics compared to conventional topologies

Features	*This Work*	*[4]*	*[6]*	*IA (Texas Instruments)*
CMOS Technology	0.18 µm	0.5 µm	0.5 µm	TI bipolar process (BiCom3)
Supply Voltage	1.8 V	± 1.5 V	3 V	1.8 V to 5.5 V
Gain dB @0.1Hz→100Hz	0-40 dB	0-80 dB	3-68 dB	≈ 60 dB
Input common Mode Range (V)	0.6 → 1.2	-1.5 → 1.3	1.05 → 1.7	(V-) + 0.1 ~ (V-) + 0.1
GBW of LPGA	8 MHz	N/A	N/A	350 Hz
* CMRR @50/60Hz	253 dB	117 dB	120 dB	110 dB
* PSRR @50/60Hz	235 dB	65 dB	80 dB	120 dB
Input-Referred Noise from 0.1 to 100Hz	500 nVrms	0.86 µVrms	600 nVrms	354 nVrms
Input Referred Offset	675 nV	≤ 60 µV	N/A	25 µV
THD (%)	0.022425	N/A	0.052	N/A
Power Consumption	99 µW	1.5 mW	60 µW	150 µW

CMRR, PSRR * High value due to very low commun mode gain of the logarithmic dual gain stage

Figure 10 demonstrates the full operation as well as the down output magnitude of the CLPGA controlled by the digital part.

Table 1 shows the main characteristics of the implemented CLPGA compared to the recent conventional and industrial topologies. It can be seen that the proposed CLPGA offers high performance of critical parameters such as very high CMRR& PSRR, low input-referred-noise, low offset voltage, no cross-over distortion since the input stimulus is made close to the biopotential signal, wide operation frequency and reasonable power consumption

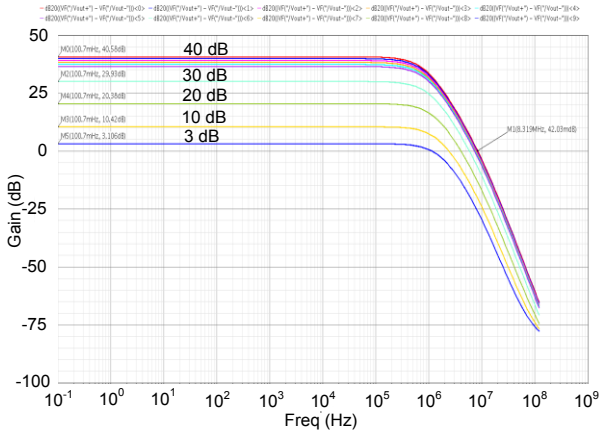


Fig. 10. Frequency response of the CLPGA for different gain

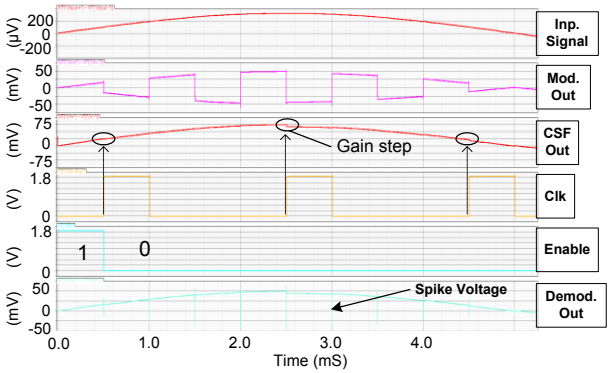


Fig. 11. Simulation results of the CLPGA controlled by digital part for f_{Clk} = 666 kHz and input sine wave of 360 µV.

V. Conclusion

In this paper, the implementation of high CMRR/PSRR, lowinput-referred noise, and small silicon area CLPGA for EEG acquisition systm has been described using the CMOS0.18 µm technology. We proposed a new preamplification technique of EEG channel that uses a chopped logarithmic programmable gain amplifier. The post-layout simulation of this module shows several advantages compared to conventional IA: high CMRR/PSRR, low noise, wide bandwidth, non cross-distortion, high programming precision reasonable consumption, and low power-supply voltage adequate for the future portable EEG devices.

References

[1] M. Ven Bavel et al, "Wearable Battery-free Wireless 2-Channel EEG Systems Powered by Energy Scavengers" Journal of Sensors & Transducers, Vol. 94, No. 7, pp. 103-115, July 2008.

[2] J. Xu et al, "A 160 µW 8-Channel Active Electrode System for EEG Monitoring" IEEE Transactions on Biomedical circuits and systems, Vol. 5, No. 6, Dec. 2011.

[3] Ch. Chieh et al, "Front-end amplifier of low-noise and tunable BW/gain for portable biomedical signal acquisition" IEEE ISCAS, pp. 2717-2720, May 2008.

[4] A. K. Ng and P. K. M. Chan, "A CMOS Analog Front-End IC for Portable EEG/ECG Monitoring Applications" IEEE Trans. Circuits, Syst, I, Regular Papers, Vol. 25, No. 11, pp. 2335-2347, Nov. 2005.

[5] C. H. Hsu et al, "A high performance current-balancing instrumentation amplifier for ECG monitoring system" IEEE ISOCC, pp. 83-86, May 2009.

[6] R. F. Yazicioglu et al, "A 60 µW 60 nV/√Hz Readout Front-End for Portable Biopotential Acquisition Systems" IEEE Trans. Circuits, Syst, I, Regular Papers, Vol. 42, No. 5, pp. 1100-1110, May 2007.

[7] M. Sawan et al, "Integrated Front-End Receiver For A portable Ultrasonic System", Journal of Analog Integrated Circuits and Signal Processing, Vol. 36, Issue 1, pp. 57-67, July 2003.

[8] T. Denison et al, "A 2.2µW 94nV/√Hz, Chopper-Stabilized Instrumentation Amplifier for EEG Detection in Chronic Implants", IEEE International Solid-State Circuits Conference, pp. 162 - 594, Feb. 2007.