35th Annual International Conference of the IEEE EMBS
Osaka, Japan, 3 - 7 July, 2013

Wireless Neural Acquisition System Design*

Qu Ruoyuan, Li Tong, Li Xiao, Xu Minglu, Chen Yueyang , Wang Xinghua

Abstract—**A wireless neural signal acquisition system is presented for freely-running test. It consists of low-noise, high input impedance analog processing, radio frequency (RF) transmitter and receiver. Firstly, the weak neural signal is amplified by a variable gain pre-amplifier and then digitalized by a Sigma-delta ADC. Secondly, the digital data is transmitted and received with couple of RF circuits based on IEEE STD802.15 standard and on-off keying (OOK) modulation. Fabricated in SMIC 0.18μm CMOS process, the IC prototype occupies 2.88mm^2 and works functionally, which can be a wide solution for wireless neural signal processor.**

I. Introduction

The biological brain and neural function research has been more and more popular in modern medical and clinical application: on the one hand, Electrical stimulation by neural microelectrodes has been applied in treatment of intractable diseases such as polio and Parkinson's disease; on the other hand, real neural signals offer reliable data for diagnosis[1,2]. This paper presents a wireless neural signal acquisition system to acquire more accurate, efficient and less delay electronic neural signal. Wireless RF circuits are adopted to transfer neural signal without data SNR decline and high risk of wound infection. Meanwhile, there is an ADC to digitalize the neural signal on chip, which makes the transfer and process more efficiently. This paper is organized as below: circuit design will be introduced in the second part; the chip test result will be analyzed in the third part; the fourth part is the summary of the main work.

II. Circuit Design

A. System Design

The system architecture shown in Fig 1 contains three parts: analog front-end, RF transmitter and receiver. As microelectrode usually has a small output magnitude and high output impedance, the function of analog process is to receive and amplify the signal. OOK modulation is adopted in this design as it has 1.5 times less bandwidth utilization and 50% less power consumption compared with Frequency Shift Key modulation method [3]. Carrier signal is generated by low power VCO instead of phase-locked loop in transmitter, and the off-chip antenna sends out modulated data after being amplified by the power amplifier. Low-noise amplifier located in receiver is used to amplify the data from antenna, and then data is demodulated and buffered to CMOS format for computer analysis.

B. Analog Process

Usually the output of microelectrode is as small as several ten micro volts, and the output impedance is as high as several mega ohms, therefore the key point of amplifier lays on low-noise, high-gain and high input impedance design. The operational amplifier architecture is shown in Fig.2. Gain is decided by the ratio of R2 and R1, and adjustable gain from 1 to 1000 can be achieved as R1 is placed off-chip. Meanwhile, this connection provides higher input impedance than traditional close-loop architecture as input is connected to gate of MOSFET instead of resistor. Flicker noise is a key issue for the two stages common-source amplifier as the neural signals are low frequency data. According to the equivalent input 1/f noise voltage spectrum density shown in the following formula, the common-source MOS with large width and length is used to decrease the flicker noise.

$$v_f^2 = \frac{K_f}{C_{ox}^{\ 2} \cdot W \cdot L \cdot f} \tag{1}$$

In which, v_f represents the flicker noise, and K_f is constant when the electron quasi-Fermi level doesn't change.

After being amplified, Sigma-delta ADC is chosen to covert the analog signal. Sigma-delta ADC adopts over-sampling technique to average white noise in a wide sample bandwidth, therefore after down-sampling filter the noise in signal bandwidth is much lower. This ADC has a second order noise shaping function as well as low power consumption, stability and high precision [4]. Designed ADC is shown in Fig.3, it is a second-order single quantizer and one bit DAC structure. K1 and K2 are non-over lapping clocks that are provided by the on-chip clock-tree.

In the circuit design, discrete-time integrator and comparator are used to consume as low static current as possible. At the same time, as the coefficient is decided by the ratio of two capacitances and layout between capacitances has a better matching, switch-capacitor integrator with common-mode feedback is good for precise coefficient implement. The function of the integrator is shown in the following formula.

$$V_{out} = -\frac{1}{RC_F}\int V_{in}\,dt = -\frac{C_S}{C_F} \bullet f_{CK}\int V_{in}\,dt \tag{2}$$

In which C_S and C_f represent the sample and integration capacitances respectively and f_{CK} is clock frequency.

*Research is supported by the "Strategic Priority Research Program" of the Chinese Academy of Sciences, Grant No. XDA06020101 and the national science foundation for young scientists of China (Grant No.61201040).

Qu Ruoyuan, Li Tong, Li Xiao, Xu Minglu, Wang Xinghua is with School of Information and Electronics, Beijing Institute of Technology, Beijing, 100081 China (e-mail: quruoyuan@hotmail.com).

Chen Yueyang is with School of Information and Electronics, Beijing Institute of Technology, Beijing, 100081 China (corresponding author: +86010-68913074; fax: +86010-68913074; e-mail:chenyuexiang@bit.edu.cn).

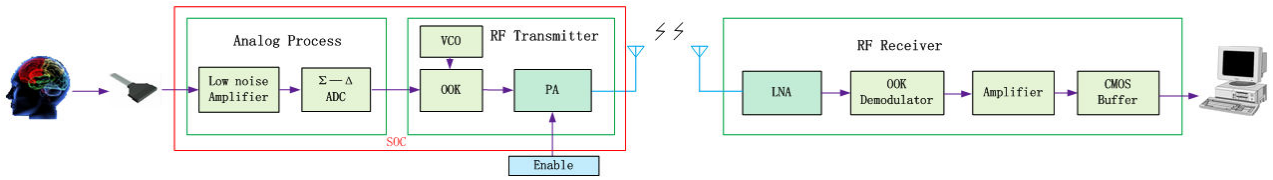

Figure 1. System architecture of the wireless neural signal acquisition system which contains analog module, RF transmitter and RF receiver. Analog module and RF TX are supposed to be integreted in the same chip and low power.

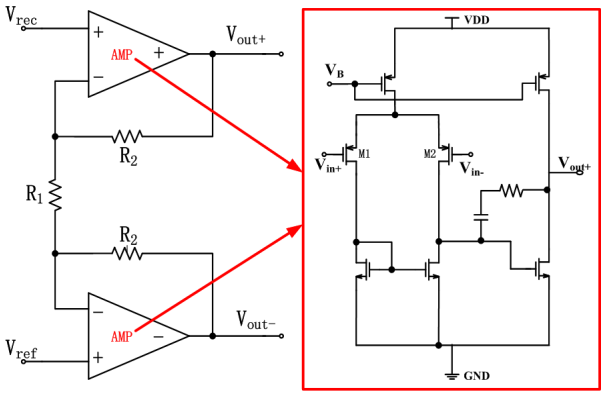

Figure 2. Schematic representation of high input impedience and high gain Op-amp implemented by two diffiential input and single output amplifiers and resistors. R1 is implemented off-chip for a adjustable gain.

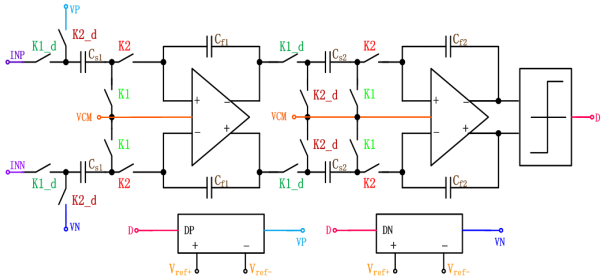

Figure 3. Schematic representation of second order one bit quantizer sigma delta ADC controled by non-overlapping clock K1 and K2.

C. RF Transmitter

The voltage-controlled oscillator is consisted of three parts: LC-type VCO with cross-coupled load, bias circuit that adopts cascode current mirror structure and the CML output buffer circuit. The core schematic is shown in Fig.4. There are two kinds of load capacitances that offer 300MHz tuning range, varactors and 2-bit digital logic to control the different fixed capacitor configurations. Both complementary cross-coupled NMOS and PMOS pairs are used to provide negative resistor in VCO design. Meanwhile, appropriate output common mode voltage can be achieved by adjusting the cross-coupled pair, which provides a good DC operating point to the following circuit and a convenient implementation of variable capacitor controlled voltage [5]. Inductor is implemented by two direct serial symmetric inductors, which achieve larger quality factor and smaller chip area. Fixed capacitance is implemented by high quality factor MIM capacitors, while variable capacitor is implemented by accumulation NMOS capacitor.

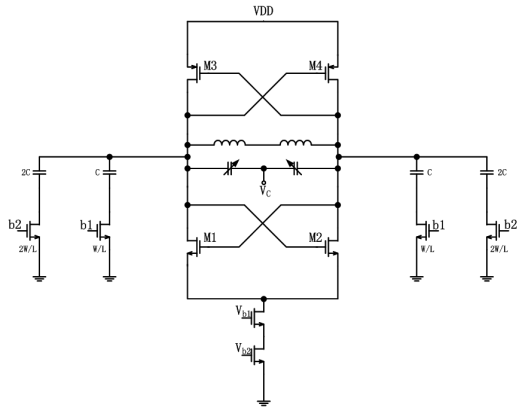

Figure 4. Schematic representation of 2 bit digital logic controlled tunable LC-type VCO with cascode current mirror

The circuit of on-off keying modulator and some important waveforms at circuit key nodes are shown in the Fig.5. NMOS M3, M4 and M6 are served as switches in this modulator structure, which are controlled by transfer data. When data is logic "1" switches are on, the carrier signal can be amplified by the common source MOS and achieved at the output node; while the modulator circuit is completely shut off When data is logic "0", which achieves smaller leak and coupling of clock signal generated at output node. Meanwhile the usage of PMOS switch M5 can shorten the differential outputs rapidly. In order to get smaller open resistance, which means a shorter cut-off time, the size of M5 should be large enough. As shown in the following simulation result, the switch speed from "0" to "1" can be 35ps shorter by use of M5. The value of inductive load is selected according to the following circuit impedance requirement at the working frequency.

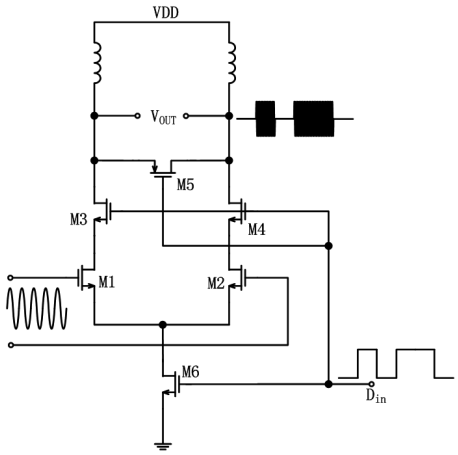

Figure 5. Schematic representation of on-off keying circuit with inductance load.M1/2 works for carriar signal and other MOS works as switches controlled by data to be modulated.

The specifications of the power amplifier are referenced according to Bluetooth standard, in which output power of 1dB compression point is necessarily no less than 4dBm. In order to meet the gain and amplitude requirements of antenna, one stage power amplifier shown in Fig.6 is used to further amplify the signal generated by the output of the modulator. Pseudo-differential transformer load cascode amplifier structure is presented in this design. Except boosting the gain, another advantage of cascode architecture is to protect the circuit from breaking down. That is to say under the same output power, the circuit can provide a larger output range, therefore less current and smaller transistor will be needed. In Fig.7 it is can be seen that the breakdown voltage of cascode structure is higher than the one of common-source.

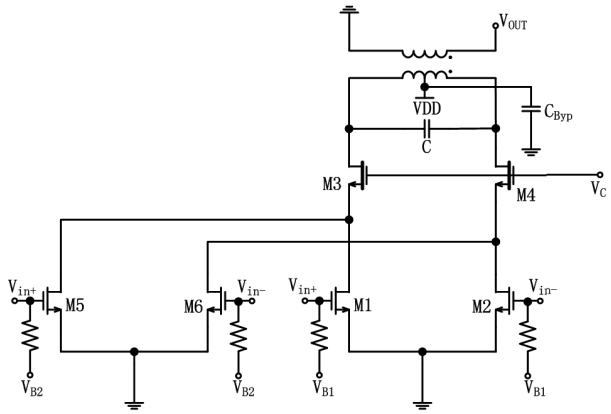

Figure 6. Schematic representation of transformer load cascode power amplifier with two input stages working in class A and B respectively for a better linearity.

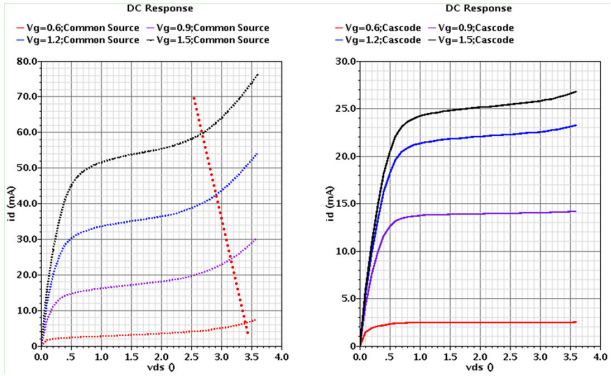

Figure 7. Breakdown voltage simulation of common-source Vs cascode. Dotted red line shows the breakdown voltage of common source structure in left sub window, while on the right it shows the cascode structure won't be breakdown within power supply voltage

D. RF Receiver

The RF receiver is made up of a low noise amplifier and an on-off keying demodulator. Through a buffer stage, the final output is sent to computer. Fig. 8 shows the schematic circuit of LNA. Larger M2 helps to reduce the couple effect between output and input. However, this will lead to a larger parasitic capacitor. This is unacceptable at high frequency, as it would enlarge noise created by M2. Generally, size of M2 is chosen to be the same as that of M1. In this way, drain of M1 can be merged with source of M2 in layout, resulting in a small parasitic capacitor. Inductor connected in series with source of M1 helps to make the real part of input impedance to be positive, which makes LNA a narrow-band amplifier. It could reduce the whole power consumption. At the same time, noise performance is optimized. Usually a small inductor is connected between source terminal of M1 and the ground in series in actual design. It brings in a negative feedback that realizes impedance matching at no additional noise as well as stability of the circuit is improved.

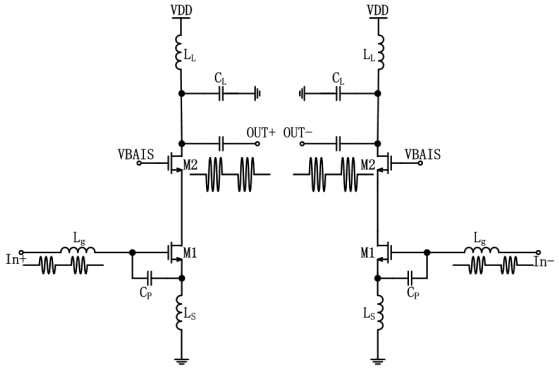

Figure 8. Schematic representation of pseudo-differential inductive degenerated cascode LNA circuit

Fig. 9 represents the schematic circuit diagram of OOK demodulator as well as waveforms at critical nodes. The demodulator mainly consists of three parts. The first part is a common source amplifier that is biased on class AB. R_B and V_B provide DC bias for MOSFETs M1 and M2. The second part is also an amplifier while it converts the single ended input to differential. The last part is an adjusting circuit designed for DC offset. R1 and C1 constitute a filter network, whose corner frequency should be higher than data frequency while lower than double frequency of the carrier. Both R2 and C2 work together to extract DC signal at node V_Q.

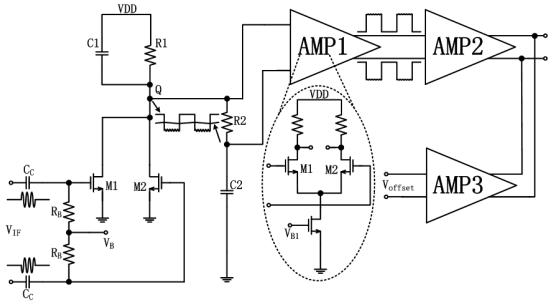

Figure 9. Schematic representation of single end to differential envelope detection with DC offset cancellation

III. Test Results

Fabricated in 0.18um SMIC 1P6M CMOS process, the IC prototype core occupies 2.88mm^2 area with a 1.8V power supply. It is shown in Fig. 10 and each module is labeled.

Test result of the analog front-end is shown in Fig. 11. Amplitude of the sinusoidal input is 2mV with 1 KHz frequency. After amplifying 500 times and sampling by 1.1MHz clock, output SNR of the ADC is 67 dB, which means effective accuracy is 11 bits.

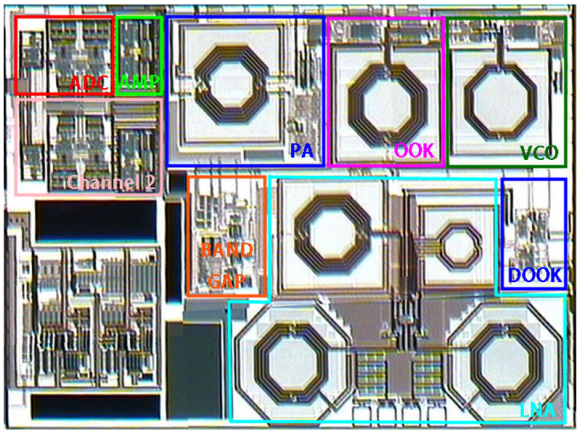

Figure 10. Chip die photograph

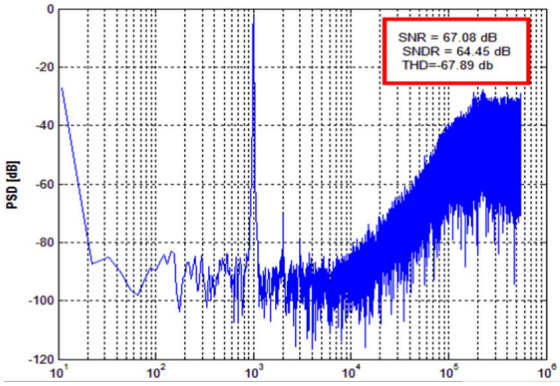

Figure 11. Power spectral density of analog process output when input 1KHz 2mV sine wave and sample frequency is 1.1MHz. It shows a 11bit ENOB for the whole analog process module.

The transmitter is tested with the analog module and the results are shown in Fig. 12. After analog to digital conversion, the actual neural signal is shown as the green line. Then through OOK modulation, the red line represents the signal. The blue waveform shows the signal processed by PA that will be transmitted. Results show the right function which means when logic '1' comes, oscillating signals at 2.45GHz created by VCO is sent, while when logic is '0' the output is 0V.

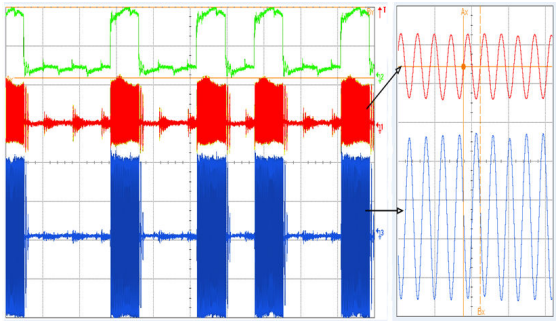

Figure 12. Functional test results of transmitter, logic '1' has a 2.45GHz carrier output, while '0' has a 0V output.

At last, the whole system is tested with a neural signal source (Blackrock microsystems, Ltd) and two prototypes in this design preformed as TX and RX respectively. Received digital data is filtered in Matlab and final test results in time domain are shown in Fig. 13. Received raw data is revealed in the first sub-window. And the following two show the local field potential and spike signal separated from raw data. It indicates that the whole system works functionally and well for the neural acquisition application.

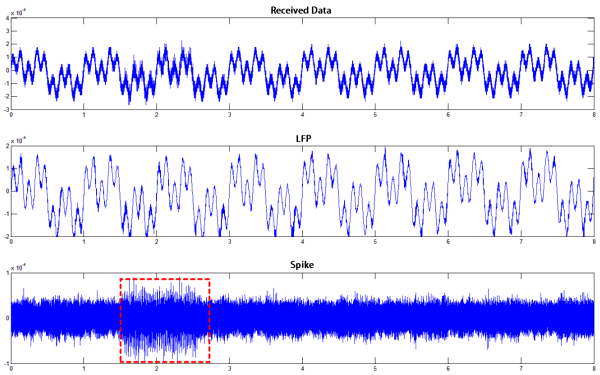

Figure 13. Received data of the whole system test with a neural signal source, LFP shows the low frequecy signals within 10KHz and the Spike sigal is all happed in the red square in 1K-2KHz.

IV. Conclusion

A wireless neural acquisition system is presented in this paper. The analog preamplifier has qualities of high gain, high input impedance and low noise and high precision Sigma-delta ADC is adopted in this system. The wireless transfer/receiver modules are designed based on WIFI and Bluetooth Class2 characteristics. Fabricated in a 0.18μm CMOS process and tested, the transmitter module functionally performs well. SNR of the ADC is 67dB at working frequency. Center frequency of the voltage controlled oscillator is 2.45GHz, meanwhile the modulator and power amplifier work functionally. Therefore, this system can be a widely used solution for neural acquisition applications.

References

[1] M. A. Lebedev and M. A. Nicolelis, "Brain-machine interfaces: Past, present and future," Trends in Neurosciences, vol. 29, no. 9, Sep. 2006, pp.536–546.

[2] H. Yu, K. Najafi, "Circuitry for a wireless microsystem for neural recording microprobes," 2001 Conference Proceedings of the 23rd Annual International Conference of the IEEE Engineering in Medicine and Biology Society, Istanbul, Turkey, 25-28 October 2001: pp.761-764.

[3] R. Muller, S. Gambini, and J. M. Rabaey, "A 0.013 mm, 5 uW, DC-coupled neural signal acquisition IC with 0.5 V supply," in IEEE Solid-State Circuits Conf. Dig. Tech. Papers, 2011, pp. 302–304.

[4] Wang Xinghua, Zhong Shun'an, Chen Yueyang, "Sigma-delta modulator for low power with SC techniques", IET International Radar Conference, 2009, pp.122–125.

[5] Andrea Bevilacqua and Ali M. Niknejad, "An Ultra-wide-band CMOS Low-Noise Amplifier for 3.1–10.6-GHz Wireless Receivers", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 39, NO. 12, DECEMBER 2004, pp.2259-2269.

[6] Z. Xiao, C.-M. Tang, C. M. Dougherty, and R. Bashirullah, "A 20 uW neural recording tag with supply-current-modulated AFE in 0.13 um CMOS," in IEEE Solid-State Circuits Conf. Dig. Tech. Papers, 2010, pp. 122–123.