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A 1V Low Power Second-Order Delta-Sigma Modulator for Biomedical Signal Applicaion

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***Abstract*—This paper presents the design and implementation of a low-power delta-sigma modulator for biomedical application with a standard 90nm CMOS technology. The delta-sigma architecture is implemented as 2nd order feedforward architecture. A low quiescent current operational transconductance amplifier (OTA) is utilized to reduce power consumption. This delta-sigma modulator operated in 1V power supply, and achieved 64.87 dB signal to noise distortion ratio (SNDR) at 10 KHz bandwidth with an oversampling ratio (OSR) of 64. The power consumption is 17.14 μW, and the figure-of-merit (FOM) is 0.60 pJ/conv.**

I. Introduction

The development of the biomedical electronics grows rapidly in recent years, especially portable and wearable low-power equipments for sensing biomedical signals. The bio-potential signals contain much important information, so doctors can judge a man is healthy or not. The frequency range of different bio-potential signal is wide, from DC to 10 KHz, and the amplitude range is from μV scale to mV scale. The frequency and amplitude of common bio-potential signals are summarized in Table I[1].

Most of biomedical electronic systems are made up of the block diagram, shown in Fig.1 [2]. They include:

1) Instrumentation amplifier (IA)

   It amplifies the biomedical signal to fit the ADC input range, removes undesired low-frequency noise such as flicker noise, and reduces the effect of the electrode offset drift, thus relaxes the resolution of the ADC in Fig.1.

2) Anti-aliasing filter (AAF)

   It is used to avoid signal aliasing.

3) Analog-to-digital converter (ADC)

   Because the low-frequency electrode offset is suppressed by the instrumentation amplifier, the resolution requirement of ADC is relaxed to about 10bits[2].

4) Digital signal processor

   It is used for back-end signal processing, such as filtering, smoothing, classification, and so on.

TABLE I. Medical And Physiological Parameters

Bio-Potential Signal Type	*Amplitude*	*Frequency*
Electro-oculogram (EOG)	50 ~ 3500 μV	0 ~ 50 Hz
Electroencephalography (EEG)	5 ~ 300 μV	0 ~ 150 Hz
Electrocardiography (ECG)	0.5 ~ 4 mV	0.01 ~ 250 Hz
Electromyograpgy (EMG)	0.1 ~ 5 mV	0 ~ 10000 Hz

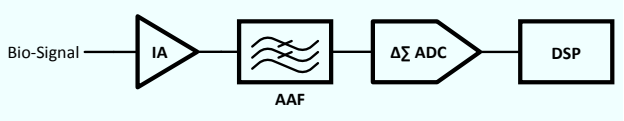

Figure 1. General front-end of biomedical system.

For a Nyquist-rate ADC, the input signal bandwidth is limited by the cut-off frequency of anti-alias filter (AAF). Because the unwanted out-of-band noise is close to the signal frequency, a higher order and sharp roll-off slope of AAF is required. The performance of an analog AAF is very challenging to achieve. For an oversampling ADC, because of oversampling, the sampling frequency is much larger than input signal bandwidth. Hence, the requirement of AAF is relaxed and can use simple passive filter to implement.

In addition, the input signal bandwidth is determined by the decimation filter. The filter is implemented as a digital filter and integrated in digital signal processor. It is easier to implement and more accurate than analog filters, and is easily configurable and re-programmable. Therefore, it is suitable for digitizing different bio-potential signals just to reconfigure the digital low-pass or band-pass filter.

A delta-sigma modulator is suitable for the A/D interface system because of its high signal to noise ratio (SNR) by using oversampling and noise shaping techniques. The oversampling technique can reduce in-band quantization noise, and the noise-shaping technique can shift quantization noise from in-band to out-of-band.

This work implements a 2nd order delta-sigma modulator as feedforward structure, which reduces the integrator's output swing and power consumption. The feedforward delta-sigma architecture and its Simulink® model are discussed in Section II, the circuit implementation is discussed in Section III, the layout and simulation results are discussed in Section IV, and Section V gives the conclusion.

II. The Architecture

Fig. 2 shows the block diagrams of the 2nd order, feedback (Fig. 2(a)) and feedforward (Fig. 2(b)) delta-sigma modulator. A 2nd order modulator is chosen because of its simple structure and robustness against non-idealities caused by the op-amp and coefficient mismatch. Although higher order

modulators may have a better SNR, they may cause the stability issues and increase power consumption.

Due to the input signal will appear in loop filter path, the operational transconductance amplifier (OTA) need to have large output swing in the conventional architecture. However, there is an extra signal path from the input of the modulator to the quantizer in the feedforward architecture. This causes the input signal is completely removed in the loop filter path[3]. This feature makes the OTA not need to have large output swing, so the design requirement of the OTA is relaxed. Thus, the power consumption of the modulator is reduced.

In Fig. 2(b), the coefficients of gain (A1, A2, B) need to adjust to prevent two integrators from output saturation. Simultaneously, it also need to consider non-ideal effects such as sampling jitter noise, thermal noise, and settling noise to optimize the performance[4]. In this paper, the mathematical model is build with Simulink® as shown in Fig. 3, and it is used to get the optimized coefficients.

III. CIRCUIT IMPLEMENTATION

A. *Low Quiescent Current Class-AB Current Mirror OTA*

In Fig. 3, the most critical parts are OTAs. They consume most of the total power. As a result, low power consumption OTA is necessary.

For low power consideration, the OTA architecture should be simple, and avoid cascode structure in low supply voltage application. As a result, current mirror OTA is a suitable choice.

Unfortunately, high gains OTAs are needed to keep performance in switch-capacitor circuit. Conventional current mirror OTA can't provide enough gain, so we use an improved OTA to achieve high gain with one stage current mirror OTA in [5], and modify it to differential version. Its

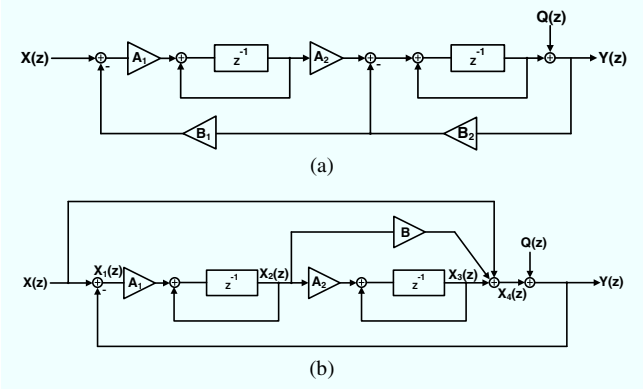

Figure 2. Block diagram of the 2nd order delta-sigma modulator (a) feedback (b) feedforward.

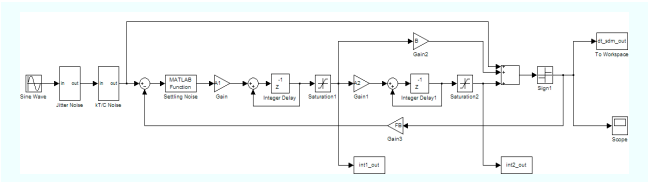

Figure 3. Simulink® model of 2nd order feedforward delta-sigma modulator with non-ideal effects.

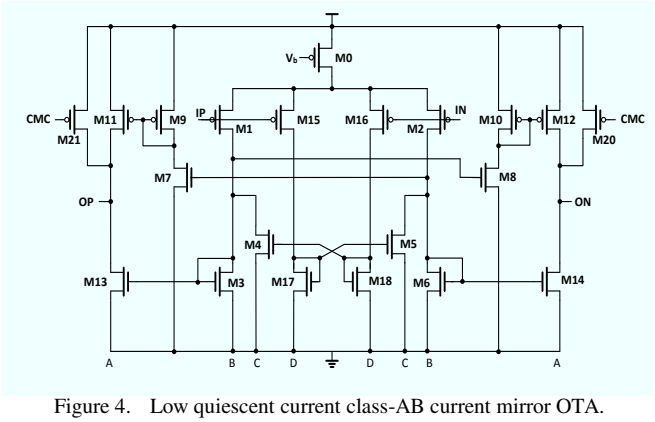

Figure 4. Low quiescent current class-AB current mirror OTA.

method is: reduce the quiescent current of the output stage, and add an extra control circuit to increase the output current during large signal operation. The circuit schematic of OTA is shown in Fig. 4. The M1, M2 are input transistors, and M15~M18 sense the input differential signal and then control two voltage controlled current sources (VCCS) as M4 and M5. In the quiescent condition, a significant portion of the drain current of M2 now flows into the current source M5, as a result reducing the output current.

The letters at the bottom of Fig. 4 represent the W/L ratio of each transistor. For example, the size of M1 is equal to B + C, and the size of M15 is D, and so on.

Therefore, the transconductance (Gm) and output resistance (Rout) of the OTA can be expressed as:

$$G_m = \frac{3}{2}\times g_{m1,2}\times\frac{A}{B}+\frac{3}{2}\times g_{m15,16}\times\frac{C}{D}\times\frac{A}{B} = \frac{3}{2}\times\frac{I_t}{V_{OD}}\times\frac{A}{B}\times\frac{B+2C}{B+C+D} \quad (1)$$

$$R_{out} = (r_{o20,o21}\parallel r_{o11,o12}\parallel r_{o13,o14}) = \frac{B+C+D}{A}\times\frac{4}{(\lambda_{20,21}+\lambda_{11,12}+2\lambda_{13,14})I_t} \quad (2)$$

Following Eq.1 and Eq.2, the gain of the OTA is:

$$A_v = (1+\frac{2C}{B})\times\frac{6}{V_{OD}(\lambda_{20,21}+\lambda_{11,12}+2\lambda_{13,14})} \quad (3)$$

From Eq.3, the gain of OTA is dependence the C/B ratio. In other words, this gain is dominated by the W/L ratio of M4/M3 and M6/M5.

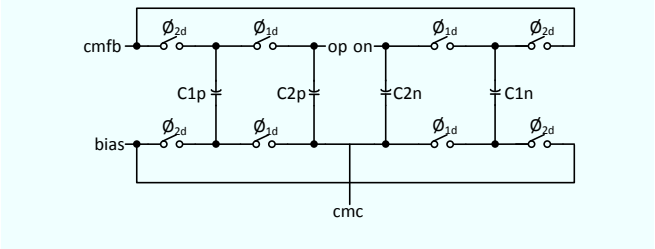

Figure 5. Common-mode feedback circuit.

This OTA is designed in a fully differential configuration, and a common-mode feedback circuit (CMFB) is used to set the common-mode output voltage to $V_{DD}/2$ for maximum output swing. The circuit schematic is shown in Fig. 5.

It operated as follows: when φ_{1d} is in off-state, φ_{2d} is in on -state, C1 stores the constant voltage $|V_{bias} - V_{cmfb}|$. And when φ_{1d} is in on-state, φ_{2d} is in off-state, one plate of C2 senses the output common voltage of OTA, and the other plate of C2 produce $V_{op} - |V_{cmfb} - V_{bias}|$ and $V_{on} - |V_{cmfb} - V_{bias}|$ to node cmc. Then the voltage V_{cmc} is used to control two transistors M20, M21 in Fig. 4.

B. Comparator

Because the effects of the non-idealities of the comparator and the quantization noise are reduced with noise-shaping, the design of 1-bit comparator can be relaxed.

A regenerative latch with clock signal control (Fig. 6) and a SR-latch (Fig. 7) are utilized to form a dynamic comparator. This comparator has some characteristics such as lower power consumption and fast transition.

It operated as follows: when phi is low, the comparator is in reset mode, M4p, M4n, M5p and M5n turn on, pull the comparator output to VDD. When phi is high, the comparator is in comparison mode, all PMOS turn off, and all NMOS turn on. The comparator output experience voltage drops from the power supply. The speed of the voltage drop is determined by the input voltage of the comparator. In order to enhance the comparison processing speed, the positive feedback structure (cross-coupled transistors) is adopted in this paper.

C. Clock Generator

Two clock signals phi1 and phi2 with non-overlapped phases are necessary for the operation of the discrete-time switch-capacitor circuit based delta-sigma modulator. To

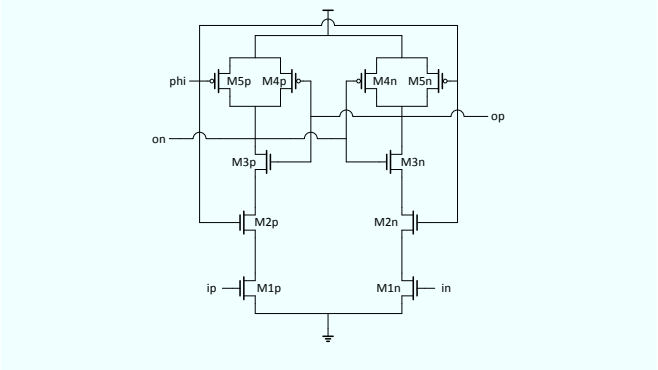

Figure 6. Regenerative latch.

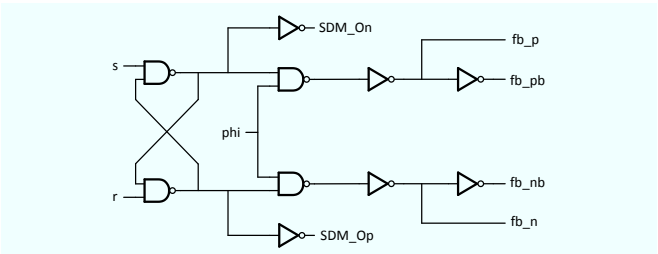

Figure 7. SR latch.

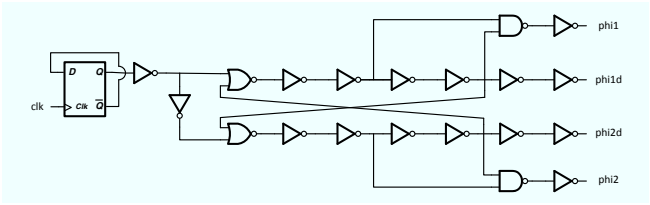

Figure 8. Two phases non-overlapped clock generator.

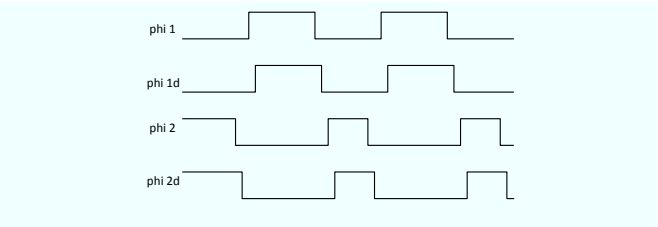

Figure 9. Timing diagram.

reduce the effect of charge injection, another two delay clock signals phi1d and phi2d are utilized, shown in Fig. 8. The timing diagram of clock generator is shown in Fig. 9.

The D flip-flop in Fig. 8 is utilized for eliminating high frequency noise generated by the external signal generator. Thus the external clock signal frequency should be set at two times larger than the sampling frequency.

D. The 2nd Order Feedforward Delta-Sigma Modulator

The modulator circuit is shown in Fig. 10. It contains two integrators and an 1 bit comparator, which are configured in differential mode for reducing even order harmonic distortion.

Although better SNR can be achieved by using multi-bit quantizer, the non-linearity of the feedback DAC may cause signal distortion. This problem can be solved by using dynamic element matching (DEM) to compensate the linearity of feedback DAC, but the system complexity is increased. Therefore, we adopt 1 bit quantizer to certificate the linearity of the feedback DAC to reduce the system complexity. Therefore, the area and power consumption is reduced.

The input common-mode voltage V_{cmi} is set to 0.2V to guarantee the OTA differential input pairs have enough operation room, and the output common-mode voltage V_{cmo} is set to $V_{DD}/2$ for maximum output swing, e.g. , 0.5V. The feedback reference voltages V_{refp} and V_{refn} are set to V_{DD} and ground.

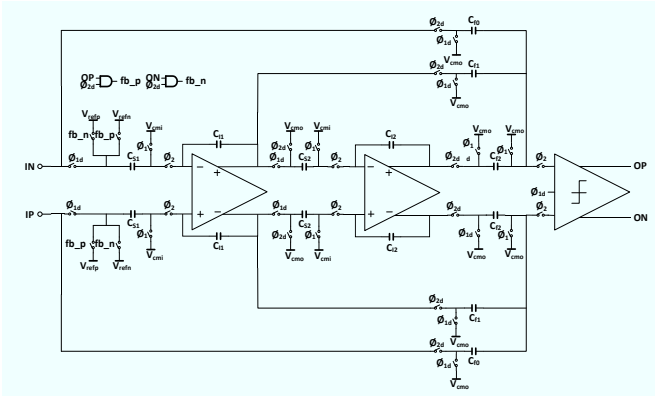

Figure 10. 2nd order feedforward delta-sigma modulator.

IV. Layout And Simulation Results

Fig. 11 shows the chip layout of the modulator. The core area is 0.75mm^2. The analog and digital power supplies are separated to avoid digital signal disturbance. The analog parts are protected by guard rings from the substrate noise, and the whole digital parts are shielded by one guard ring. The transistors in the critical signal path of the OTA are carefully arranged for symmetry layout. This prototype chip has been fabricated in a TSMC 90nm 1P9M CMOS process.

For post-layout simulation, a 2.5 KHz sinusoidal signal with $V_{DD}/2$ input offset voltage is used as modulator input. An oversampling ratio of 64 resulted in a 10 KHz signal bandwidth. Fig. 12 shows the simulated output spectrum (using 8192 bins FFT and analysis with Hann window) of the modulator. The modulator reaches the maximum SNDR of 64.87 dB while power consumption is 17.14 µW. The major parameters of the modulator and comparison are summarized in Table II. And the figure of merit (FOM) is defined as follows to compare different ADCs.

$$FOM = \frac{Power}{2^{\frac{SNDR-1.76}{6.02}} \times 2 \times BW} \quad (4)$$

V. Conclusion

In this paper, a low power 2nd order feedforward delta-sigma modulator for common bio-potential signals is presented. This modulator achieves SNDR of 64.87 dB with 10 KHz bandwidth, and its power consumption is 17.14 µW. It is suitable for different biomedical applications.

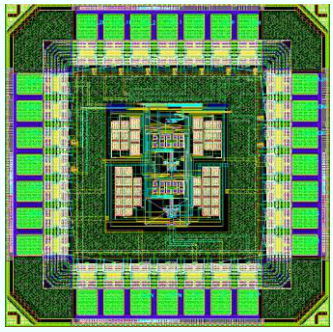

Figure 11. The chip layout.

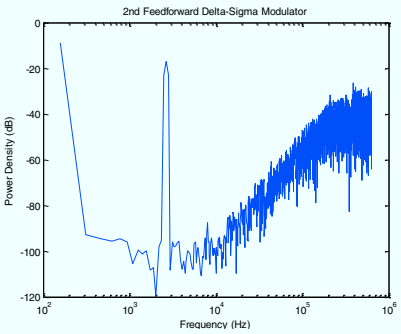

Figure 12. The output spectrum.

TABLE II. Medical And Physiological Parameters

Specification	*TCAS-I 2010 [6]*	*TCAS-I 2006 [7]*	*ISSCC 2006 [8]*	*MWSCAS 2009 [9]*	*This Work*
Supply Voltage (V)	1	0.8	0.9	1	1
OSR	100	64	256	125	64
BW (kHz)	20	5	10	16	10
Sampling Rate (MHz)	4	0.64	5.12	2	1.28
SNR (dB)	87	50	82	63.4	66.91
SNDR (dB)	84	47.5	80.1	58	64.87
ENOB (bit)	13.66	7.60	13.01	9.34	10.48
Power Consumption (µW)	660	180	200	18.1	17.14
FOM (pJ/conv.)	1.27	92.90	1.21	0.87	0.60

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