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A Pipeline VLSI Design of Fast Singular Value Decomposition Processor for Real-time EEG System Based on On-line Recursive Independent Component Analysis

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Abstract—**This paper presents a pipeline VLSI design of fast singular value decomposition (SVD) processor for real-time electroencephalography (EEG) system based on on-line recursive independent component analysis (ORICA). Since SVD is used frequently in computations of the real-time EEG system, a low-latency and high-accuracy SVD processor is essential. During the EEG system process, the proposed SVD processor aims to solve the diagonal, inverse and inverse square root matrices of the target matrices in real time. Generally, SVD requires a huge amount of computation in hardware implementation. Therefore, this work proposes a novel design concept for data flow updating to assist the pipeline VLSI implementation. The SVD processor can greatly improve the feasibility of real-time EEG system applications such as brain computer interfaces (BCIs). The proposed architecture is implemented using TSMC 90 nm CMOS technology. The sample rate of EEG raw data adopts 128 Hz. The core size of the SVD processor is 580x580 um^2, and the speed of operation frequency is 20MHz. It consumes 0.774mW of power during the 8-channel EEG system per execution time.**

I. Introduction

EEG signals are very week, and may be easily contaminated by artifacts. The independent component analysis (ICA) [1] can clearly separate the clean EEG signal and artifacts. In order to improve the feasibility and convenience of EEG system applications such as BCIs [2], a real-time ICA pre-processing is required. The proposed EEG system is based on the ORICA algorithm [3]. Because this type of ICA has a very fast convergence rate to reach receivable accuracy results, this algorithm is extremely suitable for real-time EEG applications. It produces a result from each independent component at each sample time, so we don't waste additional registers to buffer a segment of EEG raw data. Therefore, the features of this type of ICA not only give a fewer output delay time but also narrow down the hardware area. The ORICA algorithm can improve reaction time of independent component algorithm and make the combination of BCI and ICA more feasible.

The proposed SVD processor is utilized to calculate diagonal, inverse and inverse square root matrices of the target matrices during the whole system process. This processor is based on the coordinate rotation digital computer (CORDIC) algorithm [4]. This work proposes a novel SVD architecture which speeds up the calculated latency. There are two methods to lower the clock cycle numbers of SVD computations: 1) Reduce the iteration numbers directly of the computations. But unless it considerably revises the architecture of CORDIC, this method will cause the sharp decrease in the accuracy of results. 2) Alter the sequence of the updated data process. This method uses additional hardware resources to avoid structural hazard, and utilizes VLSI design skills to achieve pipeline design. However, this paper adopts the second method to achieve a low-latency and high-accuracy SVD processor.

The remainder of the paper is organized as follows. Section II demonstrates the processor in the EEG system. In section III the architecture of the SVD processor is presented. Section IV describes the details of the pipeline design consideration of the SVD processor. The simulation results are provided in Section V and finally a conclusion is given in Section VI.

II. The SVD Processor in The EEG System

This section describes the proposed SVD processor used in the EEG system based on ORICA. Fig. 1 shows the flow chart of the EEG system. First of all, the purpose of the Whitening unit is to remove the correlation of each EEG raw data, and the whitening transformation is a linear operation. Vector Z, as shown in (1) and (2), will be uncorrelated as their variances equal to unity after being whitened. And then, vector Z is sent to ORICA Training unit to estimate an unmixing weight W and the independent component Y as shown in (3) to (5). Initially, W is first set to an identity matrix ensuring full rank. Then, the following calculation is applied to update W until Δ W is close to zero.

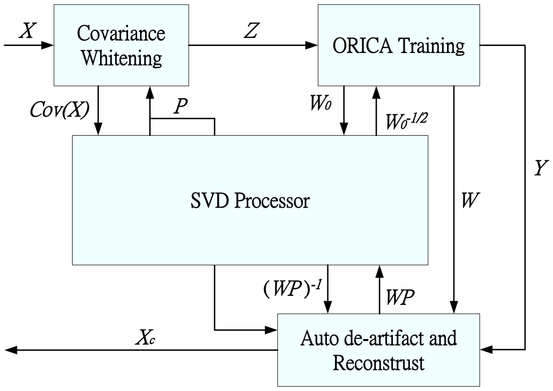

Figure 1. The data flow diagram of an EEG system.

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$$Cov(X) = E[X, X^T] \quad (1)$$

$$Z = Cov(X)^{-1/2} \times X \quad (2)$$

$$Y = W \times Z \quad (3)$$

$$\Delta W = \frac{\lambda}{1-\lambda}\left[W - \frac{y \times f^T \times W}{1 + \lambda(f^T \times y - 1)}\right] \quad (4)$$

$$W = (W + \Delta W)^{-1/2} \times (W + \Delta W) \quad (5)$$

$$X_c = (W \times P)^{-1} \times Y_c \quad (6)$$

Finally, Y is delivered to Auto de-artifact and Inverse ICA unit for artifact rejection and EEG signals reconstruction. After rejection, Y is updated as Y_c. Then, the inverse ICA is performed to obtain eye blink artifact free EEG signal, X_c as shown (6).

The following paragraph describes the algorithm adopted in this SVD processor [5]. The Jacobi SVD (JSVD) algorithm has been proven to have very good performance in dealing with pseudo inverse, matrix approximation and other similar ill-posed problems. In linear algebra, any rectangular matrices A_{mxn} can be decomposed into three special matrices as shown in (7) by JSVD algorithm. U_{mxm} and V^T_{nxn} are both unitary matrices, and Σ_{mxn} is a rectangular diagonal matrix with singular values of matrix A on the diagonal.

$$A_{m\times n} = U_{m\times m} \Sigma_{m\times n} V^T_{n\times n} \quad (7)$$

And using the property of the unitary matrix, equation (7) can be written in the following form:

$$A = U \Sigma V^T \Rightarrow U^T A V = \Sigma \quad (8)$$

A practical JSVD algorithm called the Kogbetlianz method performs two orthogonal side plane rotations to generate matrix U_{mxm} and V^T_{nxn} [6]. And as the iteration increases, A_{i+1} becomes more diagonal than A_i. The rotation equation is shown in (9). J^l_i and J^r_i are Jacobi rotation matrices and the matrix A_n will be transformed into the diagonal matrix A_0 after n iterations.

$$A_n = (J^l_n)^T (J^l_{n-1})^T \ldots (J^l_0)^T A_0 J^r_0 \ldots J^r_{n-1} J^r_n \quad (9)$$

JSVD, based on CORDIC implementation, can be decomposed into 2-by-2 SVD problems, as shown in (10). To solve each 2-by-2 SVD problem, the two-side rotation matrices composed of θ and ϕ are applied to transform the matrix A into a diagonal matrix.

$$\begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix}^T A \begin{bmatrix} \cos\phi & \sin\phi \\ -\sin\phi & \cos\phi \end{bmatrix} = \begin{bmatrix} \sigma_1 & 0 \\ 0 & \sigma_2 \end{bmatrix} \quad (10)$$

III. The Proposed SVD Processor Architecture And Implementation

The state diagram of the SVD processor flow control unit is shown in Fig. 2. In the beginning, the processor remains in the IDLE state. Once the data is received, the processor turns into State 1. In State 1, matrix L and matrix R will be set to unity matrix in the different single-port SRAMs. After that, the processor turns into Angle_Fetch state. In this state, the SVD processor will catch four corresponding elements in matrix D. Then θ_n and ϕ_n are estimated in State 3. After the calculation of angles is completed, the signal START turns into "1". In State 4, the processor will catch row vectors of matrix L and D, and catch column vectors of matrix R and D. These vectors will be updated by vector CORDIC operation and store these data to the same location of the different SRAMs in State 6.

However, this work uses eight vector CORDIC engines in State 5 for reducing the calculation latency to estimate new vectors in matrix L, R, and D. If the iteration number, Itt_num, of the vector CORDIC engine is less than Total_ITER, this work is set to 5, the data flow will turn into State 4 periodically. However, the situation wherein the number of Iteration equals the total number of iteration results in State 5. This situation means that the processor finished the singular value decomposition of the target matrix. Finally, the processor calculates the inverse or inverse square root of the diagonal elements of matrix D in State 7. It then turns into State 0 while waiting for the next data.

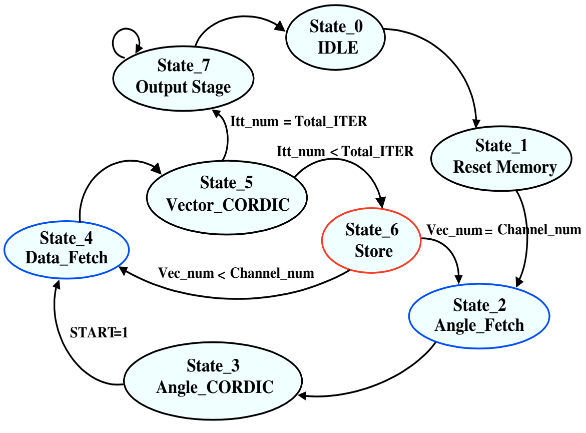


Figure 2. State diagram of the SVD processor flow control unit.

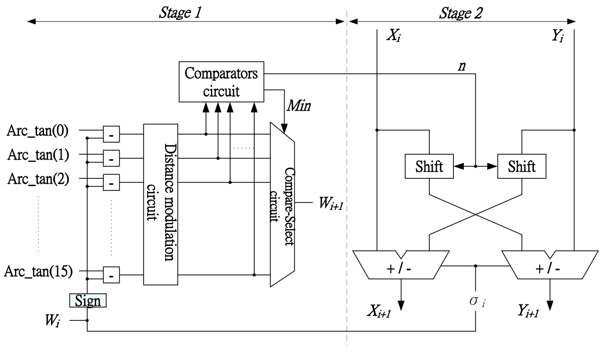


Figure 3. The architecture of the vector CORDIC engine circuit

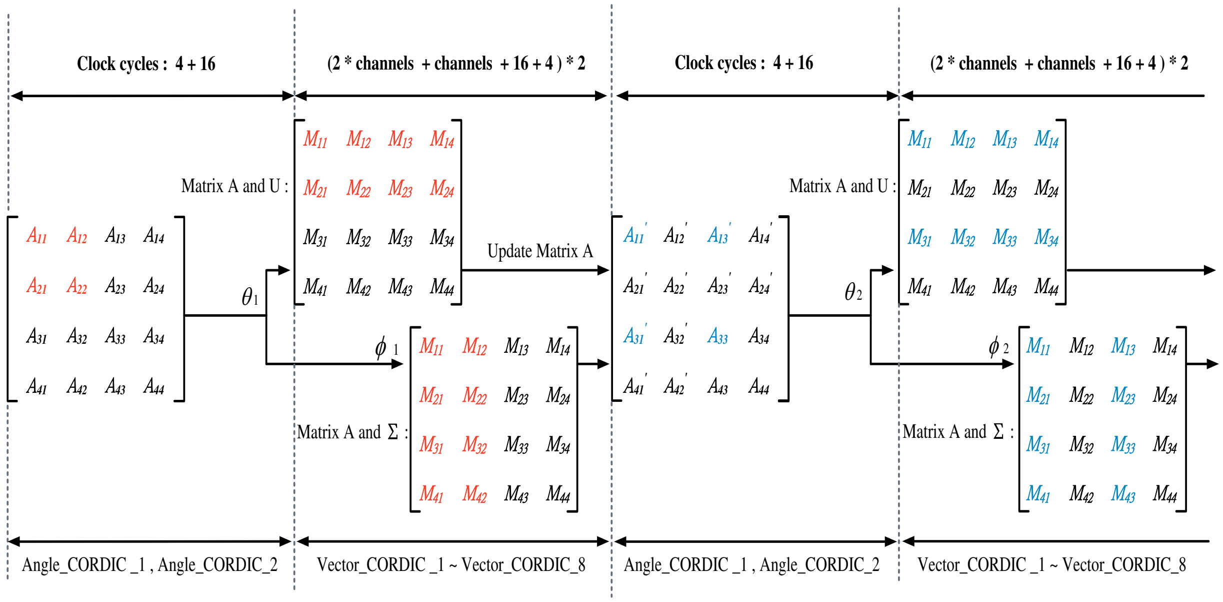

Clock cycles : 4 + 16
(2 * channels + channels + 16 + 4) * 2
Clock cycles : 4 + 16
(2 * channels + channels + 16 + 4) * 2
Matrix A and U :
Update Matrix A
Matrix A and U :
θ_1
ϕ_1
θ_2
ϕ_2
Matrix A and Σ :
Matrix A and Σ :
A_{11} A_{12} A_{13} A_{14}
A_{21} A_{22} A_{23} A_{24}
A_{31} A_{32} A_{33} A_{34}
A_{41} A_{42} A_{43} A_{44}
M_{11} M_{12} M_{13} M_{14}
M_{21} M_{22} M_{23} M_{24}
M_{31} M_{32} M_{33} M_{34}
M_{41} M_{42} M_{43} M_{44}
A_{11}' A_{12}' A_{13}' A_{14}'
A_{21}' A_{22}' A_{23}' A_{24}'
A_{31}' A_{32}' A_{33} A_{34}
A_{41}' A_{42}' A_{43} A_{44}
Angle_CORDIC _1 , Angle_CORDIC_2
Vector_CORDIC _1 ~ Vector_CORDIC_8
Angle_CORDIC _1 , Angle_CORDIC_2
Vector_CORDIC _1 ~ Vector_CORDIC_8

Figure 3. The data flow of the SVD processor

The architecture of the vector CORDIC engine circuit is shown in Fig. 3. The pipeline VLSI design used in this work is implemented in stage 1. The novel circuit is in front of the traditional circuit, stage 2 [4]. Stage 1 contains a distance modulation circuit, sixteen adders, and a comparator circuit to execute CORDIC iteration. And distance modulation circuit consists of sixteen multipliers to finish distance scaling of updated vectors. Although this additional circuit causes the hardware area to increase, the advantage is that the engine can finish comparing operations of about sixteen arc-tangent values in a clock period. Therefore, this way can not only decrease the total latency of SVD operation, but also increase the accuracy of the EEG system results.

IV. Pipeline Design of The SVD Processor

Fig. 3 is the data flow during the SVD process. First, Angle_CORDIC_1 and Angle_CORDIC_2 fetch the red elements, A_{11}, A_{12}, A_{21}, A_{22}, in matrix A, and these Angle_CORDICs calculates θ_1 and ϕ_1 respectively at the same time. Similarly, the Angle_CORDICs will fetch the blue elements, A_{11}' , A_{13}', A_{31}', A_{33}, in the updated matrix A to calculate θ_2 and ϕ_2 while on its second operation. After the angles estimation, Vector_CORDICs catch θ_1 and the red elements , M_{11}, M_{12}, M_{13}, M_{14}, M_{21}, M_{22}, M_{23}, M_{24}, in matrices A and U to execute iterative operation. The SVD utilizes eight Vector_CORDICs to update matrices A and U simultaneously. After the data updating, the latest data will be stored back in the same location of the original ones. In the same way, Vector_CORDICs finish renewing matrices A and Σ.

$$T_A = C_2^{channels} \times (4 + 16) \tag{11}$$

$$T_B = [(2 + 1) \times channels + (4 + 16)] \times 2 \times T_A \tag{12}$$

However, Angle_CORDIC and Vector_CORDIC spend total clock cycles as shown in (11) and (12). It's obvious that Vector_CORDIC operation almost wastes latency in the whole SVD operation.

V. Simulation Results

The pipeline SVD processor is used to solve the diagonal, inverse and inverse square root matrices of the target matrices. The simulation shows that the mean square errors are under 1%. And the execution time improved by the pipeline architecture of the proposed SVD processor is sufficient for the real-time and high accuracy requirements. Moreover, the performance assessment of the EEG system is based on the correlation coefficient, which is defined as the relationship between the EEG source and the ICA results.

Fig.5 shows the variation of mean error with the iteration number increasing. This work compares the result of the SVD processor with eig(A), where eig is MATLAB command for calculating the singular value decomposition of the target matrix. This work adopts five times the iteration number, Itt_num, based on the simulation results. This setting is the most suitable trade-off between operation latency and accuracy requirements of the SVD processor. It is evident that the proposed SVD processor gives better performance as compared with Reference [7].

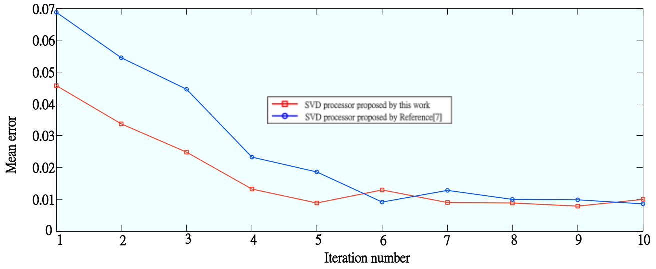
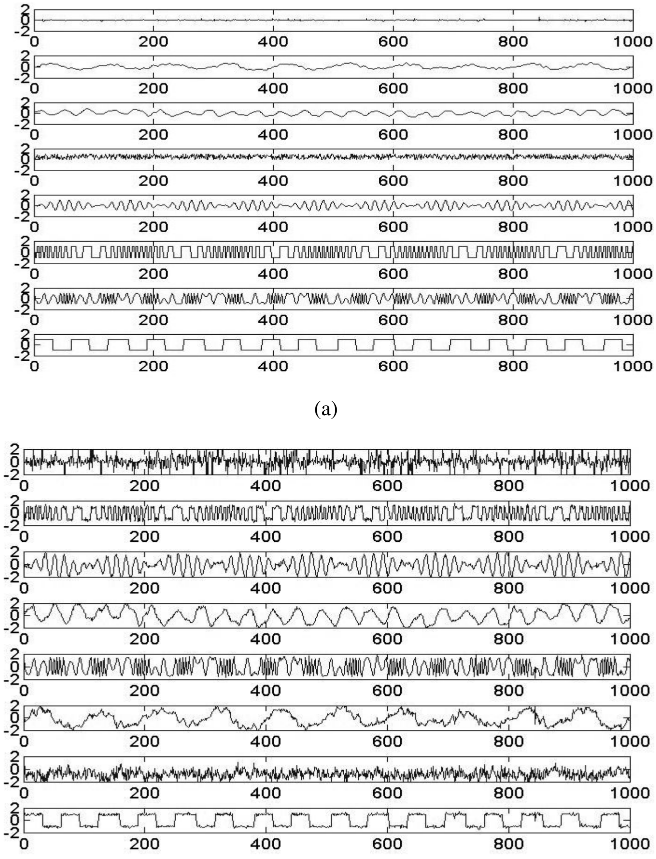


Figure 5. The correlation of the SVD processor



(a)

(b)

Figure 6. (a) Original EEG signal, (b) Simulation result of proposed EEG system

Fig. 6 shows the simulation results of the eight-channel EEG system. The original EEG signal is shown in Fig. 6(a), and the treated signal by this work is shown in Fig. 6(b). This work generates a randomly mixing matrix M = rand(*ch*;*ch*), where rand is MATLAB command for generating uniformly distributed random numbers. It is used to obtain mixtures matrix, *Mix*(*n*). And this matrix is the input data of the multi-channel EEG system based on the SVD processor. It is evident that the channel eight of both Fig. 6(a) and Fig. 6(a) gives faster convergence speed and obviously steadier state source separation.

It is particularly important that the correlation is very high, and this result vigorously proves that the proposed SVD processor is very efficient and feasible in this system. Finally, the core size of the SVD engine based on TSMC 90nm CMOS process library is 580x580 um^2, and the speed of operation frequency is 20MHz. It consumes 0.774mW of power during the eight-channel EEG system per execution time. The chip layout is shown in Fig. 7.

VI. Conclusion

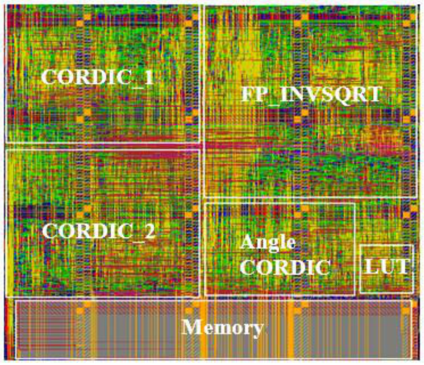


Figure 7. SVD processor chip layout.

In this paper, a low-latency and high-accuracy SVD processor is presented. It has also been shown that the proposed parallel architecture can improve 54.8% latency consumption in CORDIC operation. And the proposed SVD processor can actually benefit the EEG system to reach real-time computation and achieve a high accuracy with low mean errors and favorable correlation coefficient. Furthermore, the SVD processor gives faster convergence speed and better steady state during the EEG system process. Therefore, this work can greatly improve feasibility and convenience of the real-time EEG applications such as BCIs.

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