35th Annual International Conference of the IEEE EMBS
Osaka, Japan, 3 - 7 July, 2013

Towards a smart Holter system with high performance analogue front-end and enhanced digital processing

Leilei Du, Yan Yan, Wenxian Wu, Qiujun Mei, Yu Luo, Yang Li, Lei Wang*

Abstract— **Multiple-lead dynamic ECG recorders (Holter) play an important role in the earlier detection of various cardiovascular diseases. In this paper, we present the first several steps towards a 12-lead Holter system with high-performance AFE (Analogue Front-End) and enhanced digital processing. The system incorporates an analogue front-end chip (ADS1298 from TI), which has not yet been widely used in most commercial Holter products. A highly-efficient data management module was designated to handle the data exchange between the ADS1298 and the microprocessor (STM32L151 from ST electronics). Furthermore, the system employs a Field Programmable Gate Array (Spartan-3E from Xilinx) module, on which a dedicated real-time 227-step FIR filter was executed to improve the overall filtering performance, since the ADS1298 has no high-pass filtering capability and only allows limited low-pass filtering. The Spartan-3E FPGA is also capable of offering further on-board computational ability for a smarter Holter. The results indicate that all functional blocks work as intended. In the future, we will conduct clinical trials and compare our system with other state-of-the-arts.**

Index terms*— *high-performance, AFE, FPGA, enhanced digital processing

I. Introduction

Cardiac diseases seriously threaten human health. The World Health Organization (WHO) reported that in 2008 approximately 17.3 million people died from cardiovascular diseases such as heart disease and stroke (which makes almost 30% of all deaths globally). The WHO also estimated that by 2030, almost 23.6 million people would die from cardiovascular diseases [1]. Dynamic electrocardiogram (ECG) recorder is an important diagnostic tool to investigate cardiovascular dysfunctions. However, the amplitude of recorded ECG signals is in the range between 0.05mV and 5mV. Furthermore, it always contains power-line interferences, electrode pops or contact noise, patient-electrode motion artifacts, electromyography noise and baseline wandering [2].

There were several semiconductor manufacturers (Freescale and ADI) that offered turn-key electronic solutions for dynamic ECG recorder (Holter): ADI introduced a demo board named as ADAS1000SDZ [3], Freescale developed the MED-EKG demo board [4]. Though the performance of these demo boards is excellent, they won't be applied to clinical medicine. In this paper, an improved Holter solution has been reported. Firstly, a high-resolution A/D converter (ADS1298) is used to simply preconditioning circuit. Secondly, an FPGA is adopted to process the raw ECG signal on-board, since it is necessary to incorporate a processing module that offers further on-board processing ability in addition to the ADS1298. Moreover, the algorithms implemented in the FPGA could also be easily realized by a customized IC later.

Leilei Du is a postgraduate in the Shenzhen Key Laboratory for Low-cost Healthcare, Shenzhen, PR China (phone: +86-136-7029-6473; e-mail: ll.du@siat.ac.cn).

Lei Wang is with the Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, as a professor in Biomedical Engineering. (phone: +86-158-1851-8450; e-mail: wang.lei@siat.ac.cn).

II. System Design

As depicted in Figure 1(a), the proposed Holter system consists of an AFE with an ADS1298 and a preprocessing circuit, a microprocessor and a Spartan-3E FPGA [5]-[8]. The hardware implementation of the Holter system is shown in Figure 1(b).

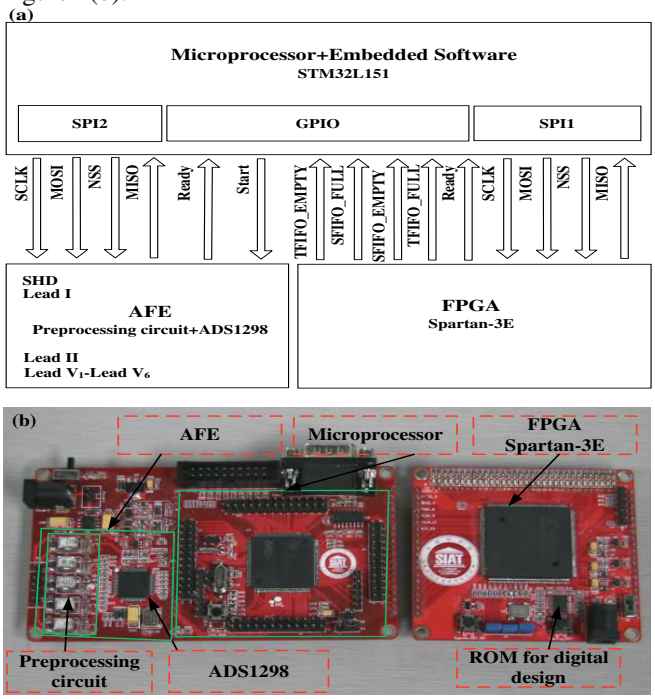


Figure 1. (a) Block diagram of the Holter system (b) Hardware implementation of the Holter system

A. AFE

In the AFE, the preprocessing circuit was designed to remove high-frequency electrosurgery interferences and to protect the proposed Holter system from overvoltage damage. As depicted in Figure 2, the circuit consists of a two-order passive RC low-pass filter with cutoff frequency of 62 kHz (-3dB) and a gas discharge tube as defibrillator and a pair of diodes which clamps the ECG signal within the input dynamic range of ADS1298.

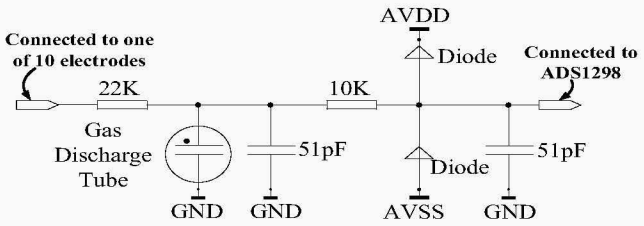


Figure 2. A single input stage of the preprocessing circuit

ADS1298 plays an important role in the AFE and even in the entire Holter system. It is a high-performance, high-resolution Δ - Σ ADC which integrates several low-pass filters and several programmable gain amplifiers [9]. When FSR (Full Scale Range) is 2.4V and the resolution is 24-bit, the LSB (Least Significant Bit) weight of digitized data could be calculated according to the following formula (1):

$$LSB = \frac{FSR}{2^{resolution-1}-1} = \frac{2.4V}{2^{23}-1} = 0.268\mu V \qquad (1)$$

Generally, the amplitude of the ECG signal is in the range between 0.05mV and 5mV. Therefore, a non-amplifying AFE module is realizable in theory and its performance is superior to that of monitoring system made of 16-bit SAR ADC and peripheral components such as Op-Amps, resistors and capacitors in power consumption, size, noise suppression, reliability and cost.

In this Holter system, ECG signal is firstly captured by ten electrodes. Then the ECG signal preconditioned by the preprocessing circuit mentioned above is transferred to the ADS1298. Once the A/D (Analog to Digital) conversion is successfully done by the ADS1298, the microprocessor receives 216-bit digitized raw ECG data from ADS1298. It is composed of 24 status bits and digitized data from bipolar limb leads (I, II) and unipolar precordial leads (V_1-V_6). In a standard 12-lead system, signals from the leads mentioned above could be measured directly from 10 electrodes which are placed on the arms, legs and forebreast. In addition, according to the relationship shown in Figure 3, the signals from bipolar limb lead (III) and unipolar augmented limb leads (aVR, aVL, aVF) could be calculated using the signals from lead I and lead II.

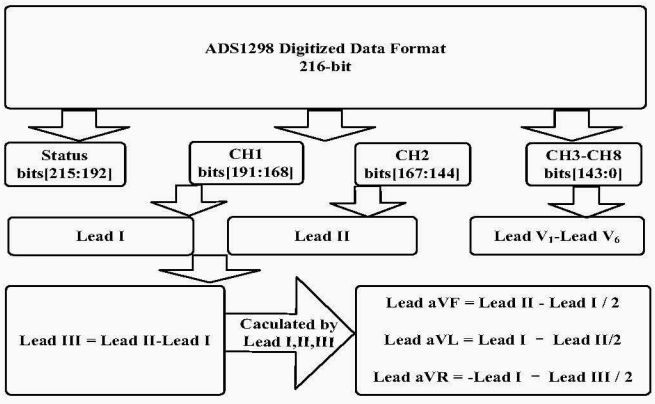


Figure 3. Calculation method of 12 leads derived from 10 electrodes placement

B. Microprocessor+ Embedded software

For our design we chose the STM32L151 microcontroller based on the 32-bit Cortex-M3 CPU. It offers five low-power modes such as low-power operating mode, sleep mode, low-power sleep mode, stop mode and standby mode. Designer is free to choose the mode that provides the best compromise among power consumption, start-up time and available wakeup sources. If AFE module is in idle state, the microprocessor is actually in standby mode to ensure minimum power consumption. Certainly, the microprocessor could be switched to operating mode by external reset signal when the AFE module needs to acquire ECG data normally.

As the core microprocessor in the entire system, STM32L151 should be capable of executing the following functions: FPGA control, ADS1298 initialization and ADS1298 conversion control. First of all, the microprocessor should be able to manipulate the data exchange from or to FPGA. Secondly, ADS1298 internally incorporates 26 registers. It is essential for the system these internal registers to be properly configured by the microprocessor. Thirdly, the A/D conversion by ADS1298 should be controllable. That is to say, the microprocessor should control ADS1298 to start and stop its conversion.

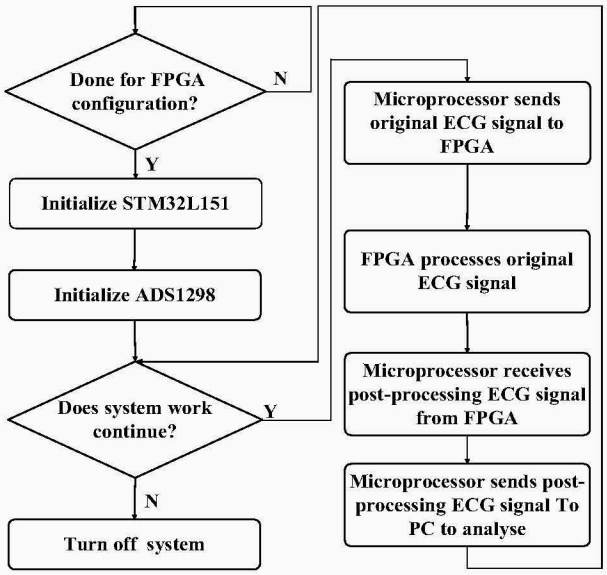


Figure 4. Flow chart of embedded software of the Holter system

Flow chart of embedded software of the proposed Holter system is presented in Figure 4. As depicted in Figure 1(b), the FPGA board is adopted to process digitized raw ECG signals. It is widely known that FPGA is a RAM-based device. Therefore, FPGA should load the digital design from ROM once powered up. So at the beginning of the flow chart, the processor should wait until the configuration of the FPGA is successfully done.

As depicted in Figure 1(a), on-chip peripherals such as SPI1 (Serial Peripheral Interface), SPI2 and GPIO (General Purpose Input and Output) are used to control the ADS1298 and the FPGA. Furthermore, ADS1298 is adopted to digitize the raw ECG signal. It is necessary to initialize the ADS1298

and the microprocessor properly before acquiring and processing the ECG signal.

In order to improve the system processing efficiency, full-duplex SPI communication was employed to transfer the raw ECG data and post-processed ECG data between the microprocessor and the FPGA. Since there are multiple leads, the microprocessor should be able to distinguish the lead to which ECG data belongs in order to guarantee functional correctness of the Holter system. So an extra byte named "Lead" is introduced to resolve this problem.

C. FPGA

As depicted in Figure 5, the FPGA is comprised of SPI, Compose, Decompose, Control Logic, Source FIFO, Target FIFO and Algorithm Block. SPI is a communication interface of FPGA which is connected to the microprocessor. It is used to receive the raw ECG signal and to send the post-processed ECG signal. The unit "Control Logic" is able to control the units "Source FIFO" and "Target FIFO" according to signals such as CDATAOK and DDATAOK. The both signals indicate that the data conversion in the "Compose" and "Decompose" units has been done successfully. The "Algorithm Block" is employed to process raw ECG signals. The operation of units "Compose", "Decompose", "Source FIFO" and "Target FIFO" will be explained in the next paragraph.

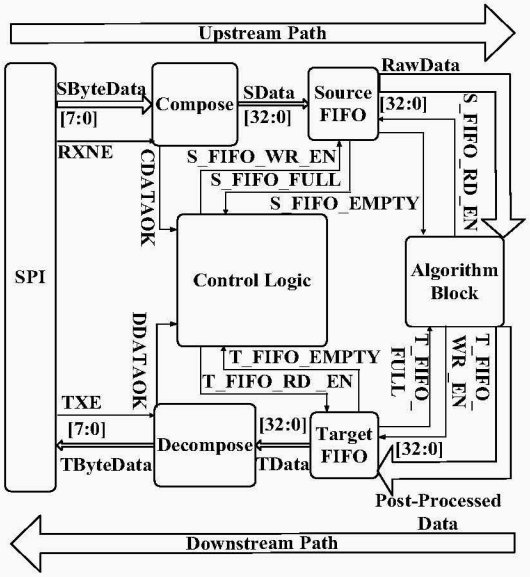


Figure 5. Block diagram of the FPGA

In the FPGA module, the primary issue is matching which involves two aspects. One aspect of matching is data throughput. For convenience, the upstream and downstream paths are denoted in Figure 5. If upstream rate becomes larger than downstream rate, the "Algorithm Block" will abandon some part of the raw ECG signal. So Source FIFO is just used to store raw ECG signal temporarily. Similarly, Target FIFO is used to store the post-processed ECG signal temporarily. As long as the capacity of Source FIFO and Target FIFO is selected properly, matching between upstream rate and downstream rate could be achieved well. The other aspect of matching is the length of the data word. As described above, the width of digitized data of one ECG lead is 32-bit. However, SPI in the microprocessor only supports 16-bit and 8-bit data transmission. Therefore, Compose has the task to reconstruct a 32-bit raw data word of one ECG lead from the corresponding incoming four bytes and the block "Decompose" breaks the post-processed 32-word data of one ECG lead into four corresponding bytes which are transmitted through the SPI.

In order to assess the processing efficiency among different algorithms, the raw ECG signal is as important as post-processed ECG signal. So we designed four modes illustrated in Figure 6 that are: idle mode, raw mode, process mode and fault mode. In raw mode, the Algorithm Block shown in Figure 5 is bypassed to obtain raw ECG waveform. The Process mode is essential for efficiency assessment among different algorithms. In this Holter system, the Algorithm Block adopts a 227-order serial FIR structure with symmetrical coefficients to process raw ECG signal. Fault mode is used to send an alarm if a certain exception occurs when FPGA is processing raw ECG signal. If a certain processing exception occurs, the 32 light-emitting diodes at top of FPGA board shown in Figure 1(b) will be turned on in a combination that corresponds to the exception. All combinations were predefined at the stage of system design.

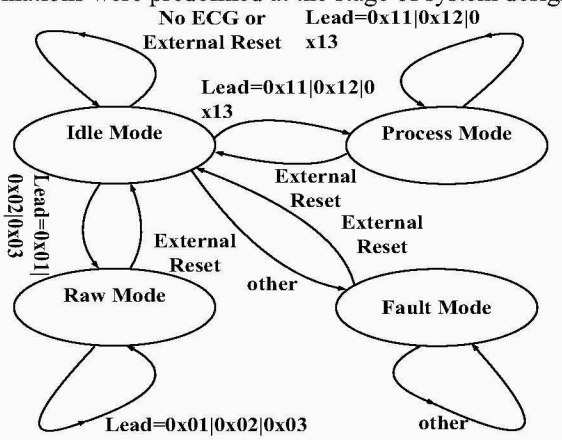


Figure 6. State Machine of the FPGA

III. RESULT

In order to check the functional correctness and the performance of this Holter system, we made two comparative trials and the details are described in the next two paragraphs.

In the functional comparative trial, firstly, we used the board with ADS1298 and the microprocessor to gain raw ECG signal shown in Figure 7(a). However, according to the spectrum shown in Figure 8(a), raw ECG waveform is strongly affected by power-line noise and baseline wandering. Therefore, we designed a 227-order band-pass FIR filter with a pass-band from 0.05Hz to 45Hz and acquired the post-processed ECG signal showed in Figure 7(b). Similarly, we obtained the spectrum of post-processing ECG signal

shown in Figure 8(b). Now we could believe that power-line noise and baseline wandering were removed from the raw ECG signal.

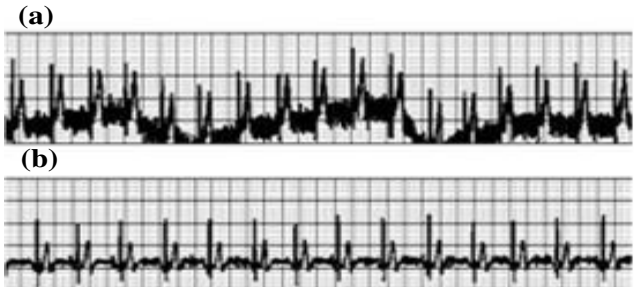


Figure 7. (a) Raw ECG signal (b) Post-processed ECG signal

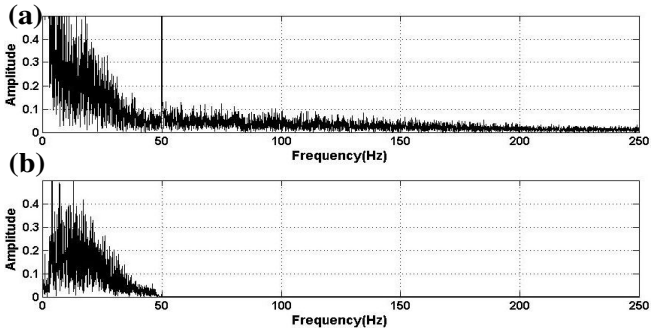
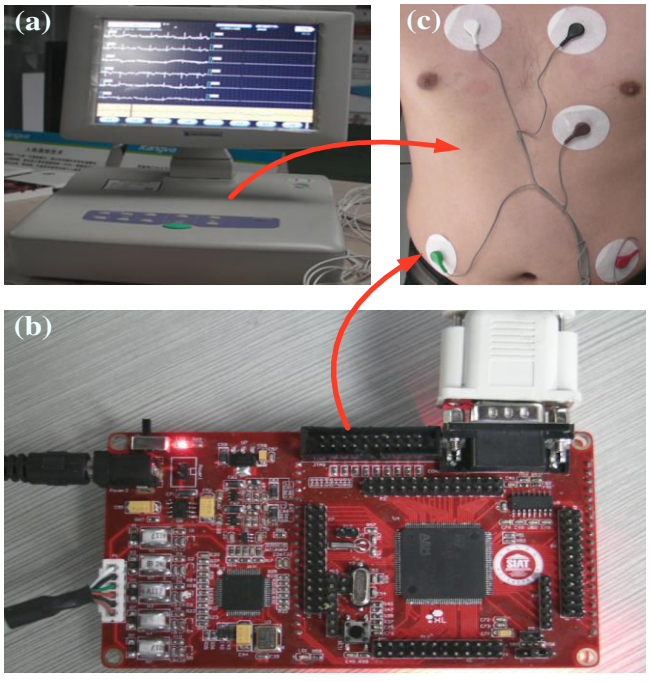


Figure 8. (a) Raw ECG signal spectrum (b) Post-processed ECG signal spectrum

In the comparative trial of performance, the Holter system and an electrocardiograph (1550P) captured ECG signals from the same volunteer. The details for this comparative trial are shown in Figure 9(a), Figure 9(b) and Figure 9(c). According to Figure 9(d) and Figure 9(e), there is a slight gap of ECG waveforms between this Holter system and 1550P.



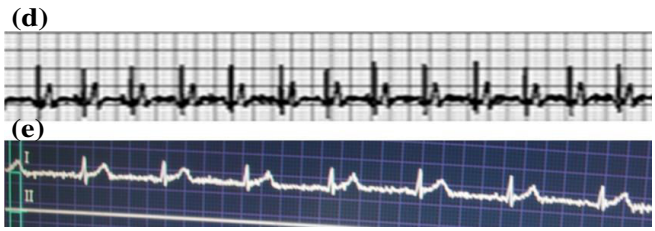


Figure 9. (a) ECG acquisition by 1550P (Nihon Kohden) (b) ECG acquisition by the proposed Holter system (c) Placement of ECG electrodes on our volunteer (d) ECG signal from the proposed system (e) ECG signal from 1550P (Nihon Kohden)

IV. Conclusion

In this paper, a smart Holter system with high performance analogue front-end and enhanced digital processing is presented. Using a high-performance AFE(Analog Front End) together with the latest 32-bit Cortex-M3 microcontroller, we are capable of making high-precision and high reliable ECG acquisition. FPGA is a digital coprocessor which is able to process ECG signals flexibly. Although at this stage the system displays ECG signals only, we intend to implement more FPGA-based diagnostic algorithms of clinical value in our future works.

Acknowledgment

This study was financed partially by the Projects of National Natural Science Foundation of China (Grant Nos. 60932001, 51105369 and 61072031), the National 863 Program of China (Grant No. 2010CB732606), the Projects of Shenzhen science and technology program (JC201005280467A) and the 'Low-cost Healthcare' Programs of Chinese Academy of Sciences.

References

[1] World Health Organization, "Prevention of cardiovascular disease: Guideline for assessment and management of cardiovascular risk", http://www.who.int/cardiovascular_diseases/guidelines/Prevention_of Cardiovascular_Disease/en/index, 2007.

[2] Naregalkar Akshay, Naga Ananda Vamsee Jonnabhotla, "ECG Noise Removal and QRS Complex Detection Using UWT," International Conference on Electronics and Information Engineering, Vol. 2, pp. 438 - 442, 2010.

[3] ADAS1000 ECG Front-End Evaluation Board for Demonstration and Development, Analog Devices, Inc., UG - 426 August, 2012.

[4] Freescale Solutions for Electrocardiograph and Heart Rate Monitor Applications, Freescale™ Semiconductor, AN4323 June, 2011.

[5] Anucha Punapung, Suradej Tretriluxana, "A Design of Configurable ECG Recorder Module," Biomedical Engineering International Conference, 2011, pp. 67 – 70.

[6] Hu Liang, Zhang Yanfang, "Non-Amplifying ECG Signal Acquisition System Based on Σ-Δ A/D," Electronic Measurement & Instruments, 2012, Vol. 3, pp. 105 – 108.

[7] Rakesh Chand, Pawan Tripathi, "FPGA Implementation of Fast FIR Low Pass Filter for EMG Removal from ECG Signal," Power, Control and Embedded Systems, 2010, pp. 1–5.

[8] Li Nianqiang, Wang Yongbing, "A Preferable Method on Digital Filter in ECG Signal's Processing Based on FPGA," Intelligent Information Technology and Security Informatics, 2010, pp. 184–187.

[9] Low-Power, 8-Channel, 24-Bit Analog Front-End for Biopotential Measurements, Texas Instruments, Inc., SBAS459H May, 2011.