35th Annual International Conference of the IEEE EMBS
Osaka, Japan, 3 - 7 July, 2013

Design of a High Voltage Stimulator Chip for a Stroke Rehabilitation System

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***Abstract*—This paper describes the design of an 8-channel high voltage stimulator chip for rehabilitation of stroke patients through surface stimulation, which requires high stimulation currents and high compliance voltage. The chip gets stimulation control data through its Serial Peripheral Interface (SPI), and can accordingly generate biphasic stimulation currents with different amplitudes, duration, frequencies and polarities independently for each channel. The current driver is implemented with thick oxide devices with a supply voltage up to 90V. The chip is designed in a 0.35μm X-FAB high voltage process.**

I. Introduction

Nowadays, with the improvement of living standard and the accelerated pace of life, the morbidity rate of stroke has kept rising year over year, causing death and disability only second to the cardiovascular diseases [1]. Stroke is caused by blood vehicle rupture or blockage in the brain, which results in damage to cerebral neurons and leads to paresis of motor functions in most survivors. There are 2 million people suffering from stroke every year in China, and the number is growing [2]. Only 70% of the patients can survive from the stroke, and most of them are left with hemiplegia, aphasia and disability. Functional Electrical Stimulation (FES) is a widely used technology for stroke rehabilitation, which has been applied to restoring lost motor functions in spinal cord jury patients by directly activating the peripheral nerves that innervate muscles with small electrical currents [3]. FES has been applied to clinical studies on reducing motor impairment and restoring the mobility [4-6]. However, most of the existing FES systems are designed for specific applications. We aim to develop an FES system that can be more flexible with different applications and wearable for home use.

The stimulator is one of the most important modules in FES system. With the improvement of the technologies, miniaturization and portability of the devices have become an important possibility in the studies. Integrated circuits, with the potential to reduce the power consumption and the size, are considered as one of the best solutions to achieve this goal. For the above consideration, the design of a configurable chip with small size, high voltage or current output and low power consumption is necessary. In 2007, Najafi *et al.* developed a chip called "Interestim-2B", which was a wireless implantable System-on-a-Chip (SoC) with 64 channels for nerve stimulation [7]. In 2011, Xiao Liu *et al.* developed an integrated stimulator with DC-isolation and fine current control for implanted nerve tripoles, which is used to restore some bodily function that has been lost due to damage to the central nervous system [8]. In 2012, a neural stimulator frontend with high-voltage compliance and programmable pulse shape for epiretinal implants has been developed [9].

In this paper, a high voltage stimulation chip is designed for a stroke rehabilitation system. The chip is to be applied in the networked FES system for a stroke rehabilitation device under development featuring high voltage stimulation. In Section II, the architecture of the networked FES system is discussed first. Next, the architecture and the circuit implementation of the high voltage chip are presented in Section III. Finally, simulation results of the chip are shown in section IV.

II. System Introduction

We have developed an FES system for stroke rehabilitation and its structure is shown in Fig. 1.

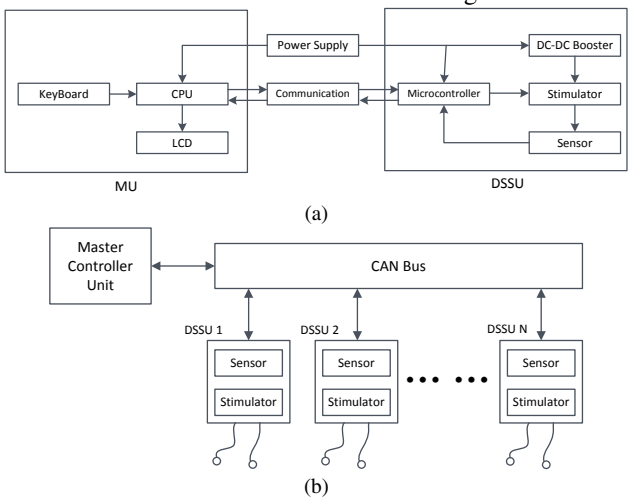


Figure 1. (a) Architecture of the network FES system. (b) The core of MU and DSSU.

The whole system can be divided into three parts: (I) the Master Unit (MU) that supervises the operation of the whole system and decides control methods of stimulation; (II) the distributed stimulation and sensor unit (DSSU), which performs stimulation to the neuromuscular system and detection of physiological signals; and (III) the communication subsystem, controls communication between MU and DSSU through a wired bus module [10]. Stimulation data is sent by MU through a serial bus to DSSUs which output electrical current pulses according to the received data. The DSSU includes a single channel stimulator which

generates stimulus current with different amplitude, duration and frequency fully controlled by the MU.

This system has two characteristics which make it flexible and practical in clinical applications. On one hand, since each DSSU is designed as a node of the network in the system, the number of the stimulation channels can be increased conveniently according to the application. On the other hand, sensor components can be incorporated in the DSSUs to allow monitoring physiological variables.

To further improve the portability and flexibility of the system, we designed a high voltage stimulator chip used in the DSSU. The chip's main function is to output stimulation currents as the stimulator in DSSU.

III. Design of the Stimulator Chip

A. Architecture of the Chip

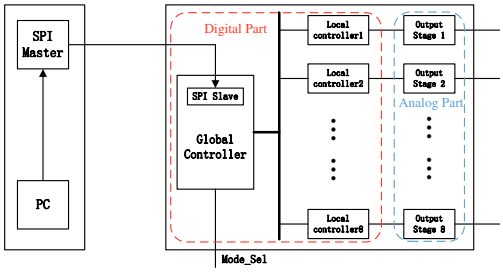


Figure 2. Architecture of the stimulator chip.

Fig. 2 shows the block diagram of the 8-channel high voltage stimulator chip with interfaces. The chip mainly consists of a digital control module which receives and processes the data from the SPI master through its SPI, and an analog output module which outputs the stimulation currents.

A parallel bus topology is adopted in the digital part. The global controller of the digital module is the core of the chip, which can identify the stimulation data packets with a header checker. The stimulation data packet contains the information of amplitudes and timing of the stimulation waves of the eight channels'. The global controller receives the data packets though a standard SPI. The CRC (Cyclic Redundancy Check) is also adopted in the global controller to check whether the data packet is transferred correctly or not. If the CRC is verified, the data will be divided into eight parts and delivered to each channel in a serial fashion. The local controller is a decoder, which decodes the data received from the global controller accordingly controls the analog output stage. The strength of the stimulation current can be configured to different levels according to the amplitude information in the packet in order to accommodate with different stimulus intensities. The chip has two output modes, i. e. the standard output mode and the fast refreshing mode. And the output mode can also be changed through a pin signal *Mode_Sel* as shown in Fig. 2.

The analog output stage generates bipolar square wave pulses which should cause less tissue damage[10] according to the amplitude and timing information received from each local controller, as shown in Fig. 3. The circuit consists of a 6-bit DAC to set the current level, and a current driver implemented by current mirror structure. Thick oxide devices are selected in the circuit with a supply voltage as high as 90V to generate currents at milliampere levels. A bit-controlled discharge channel is designed to help achieve charge-balanced biphasic stimulation to reduce the risk of tissue damage by long term stimulation. The output impedance of the driver needs to be in the 100MΩ range to keep the stimulus current constant within 1% of the desired value under the electrode-tissue impedance variations.

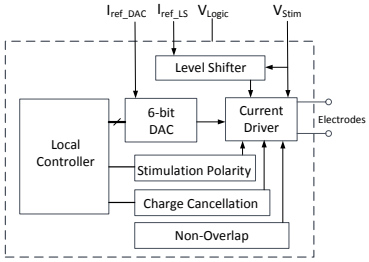


Figure 3. The structure of the current output stage of one channel.

This chip has eight output channels, so eight muscles can be stimulated by one chip simultaneously. The chip can also be easily expanded into 64 channels or more because of the two-stage architecture of the parallel bus topology adopted in the digital controller. And in this chip, a standard SPI is used, so the chip can be controlled by different MCUs. Assume that the current of the stimulation on skin, the resistance of which is 1k-2k ohms, is 50 mA, the voltage source should be 100V. So the high-voltage stimulator is needed

B. Circuit Implementation

This chip is designed in a 0.35μm X-FAB high-voltage process. The function of the digital part is designed using Verilog and synthesized with low voltage libraries provided by the foundry, resulting in smaller area, and the analog part is designed with mostly with high-voltage devices which can withstand a power supply voltage range of up to 90V. Finally these two parts are incorporated together as a mixed-signal chip.

1) Digital Part

The stimulation data is sent to the chip in the standard SPI format. The SPI of the stimulator chip works in a slave mode and that of the MU works in master mode. During operation, a signal called *spi_data* in the global controller indicates the data in the shift register of spi slave, while the signal *si_cnt* is a 4-bit counter counting from 0 to 15. When one bit data is transferred to SPI slave, *si_cnt* increases by 1. So the value of *si_cnt* shows how many bits of a frame data have been delivered to SPI slave. Once the signal *si_cnt* reaches 15, one frame of data in the shift register is saved in the global controller. When a stimulation packet is delivered to the global controller completely, the global controller will decode the whole packet for each channel according to the format shown in Table I or II, and send them into every local controller successively through the parallel bus.

The chip has two output modes: standard output mode and fast refreshing mode. The stimulation waveform is a sequence of bipolar square waves (Fig. 4). The bipolar square waveform is defined by 6 parameters: A1, A2, T1, T2, T3 and T4. In order to keep charge balance, A1×T2=A2×T4 should be

followed. The packet of standard output mode is designed in the form of TABLE I and TABLE II.

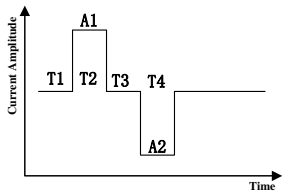


Figure 4. Bipolar square waves.

TABLE I Stimulation Data Packet in Standard Output Mode

	Head	8 Channel Data	CRC
Bits	16	464（58×8）	16

TABLE II One Channel Message in Standard Output Mode

	A1	A2	T1	T2	T3	T4	Charge Cancelation	Polarity
Bits	6	6	8	14	8	14	1	1

One full stimulation data packet, with 496 bits of data, should be sent to the chip for all eight channels to output stimulus waveforms. Each channel has 58 bits of data, including one control bit of charge cancellation. When set, it controls the analog output module circuits to keep the circuit from charge accumulation at the electrodes. And the polarity of the stimulation waves is decided by the bit of 'polarity' as shown in Table II. When it is set to "1", the stimulus current will be anodic-leading and cathodic-leading otherwise.

The stimulation data packet of 496 bits might be too long for some applications. For example, it takes at least 496us to deliver the whole packet with 1 MHz SPI clock. With other overhead in the communication subsystem, this may to be too slow if multiple chips are used. We have also designed a working mode stimulation data can be refreshed much faster. The control strategy is shown in Table III. In fast refreshing mode, each of the eight channels can be chosen to output currents or not, controlled by the bits shown as 'Switch'. However, in order to shorten the length of the data packet, the data packet of fast refreshing mode only contains one set of amplitude and timing information for all eight channels. Thus all channels output the same currents when switched on.

TABLE III Data Packet of Fast Refreshing Mode

	Head	Switch	A1	A2	T1	T2	T3	T4	CRC
Bits	16	8	6	6	8	14	8	14	16

Compared to the standard output mode, the data packet of fast refreshing mode is much smaller, which contains only 96 bits. It takes only 96 us to send the packet into chip with 1 MHz SPI clock.

What's more, the fast refreshing mode can also be used in the application which needs output current larger than the maximum amplitude of one channel in standard output mode. Since the eight channels share the same amplitude and timing information, they can be connected together to output a larger current.

2) Analog Part

As shown in Fig. 3, the local controller decodes the data sent from the global controller in the format shown in TABLE IV, and controls the analog circuitry accordingly. The 6-bit DAC converts the digital data received from the local controller into a current with magnitude controlled by the 6 bits data, and the current is further amplified and output by the current driver as explained below.

TABLE IV Data Format of Local Controller Output

	Amplitude	Charge Cancelation	Polarity
Bits	6	1	1

Each current driver outputs stimulus currents through an electrode pair, as shown in Fig. 5. The driver is implemented with high-voltage devices with a supply voltage up to 90V to obtain strong driving capability. The driver consists of a p-type current source and an n-type current sink to realize biphasic current waveform, which are designed in cascode current mirror structure to inhibit the effect of channel length modulation and achieve high output impedance to shield the impedance drift at output nodes. As shown in Fig. 6, M1-M5 are current mirror FETs, and M6-M10 are cascode FETs which adopt high-voltage devices and bear most of the supply voltage to avoid breakdown of the circuit. Through proper sizing of the devices, the current from the DAC (I_{DAC} as shown in Fig. 5) is amplified by 20 times to drive the electrode pair.

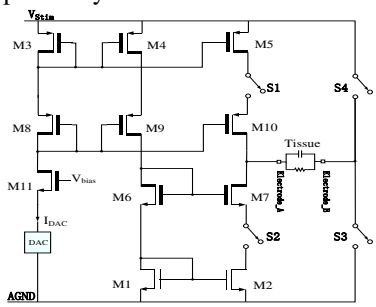


Figure 5. Structure of the biphasic high-voltage current driver.

Bipolar stimulation is achieved with the H-bridge switches as shown in Fig. 5, S1-S4. The polarity of the output currents is controlled by changing the connection of the switches. When S1 and S3 are turned on while S2 and S4 are off, the driver outputs anodic current. When S2 and S4 are turned on while S1 and S3 are off, cathodic current flows through the tissue. The charge cancellation function is also implemented by controlling the switches. When S2 and S3 are turned on while S1 and S4 are off, a discharge path is generated to release residual charge accumulated on electrodes during stimulation stage to achieve charge balance. The switches are also realized by high-voltage devices and controlled by digital block.

IV. Chip Verification

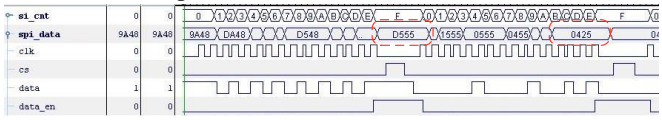
The design has been verified in both digital part and analog part through circuit simulation.

A. Digital Part Verification

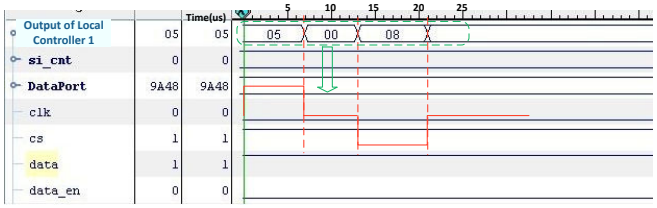
The Verilog code of the digital controller is downloaded into the FPGA board (XC2VP30). The MCU (STM32F103ZET6) sends the control data to FPGA to verify the function of the digital controller. The results are shown in Fig. 6.

As shown in Fig. 6(a), whenever *si_cnt* reaches 15, the data shown by *spi_data* is as the same as the data sent from external device, verifying that the SPI data are delivered correctly and the spi slave works properly.

The simulation results of the local controller are shown in Fig. 6(b). The output of the local controller is 8 bits, which contains 6bits (MSB) of amplitude information and 2 bits (LSB) of control information, i. e. charge cancellation and stimulation polarity. In the simulation, the MU sends a control data packet to the FPGA and the output should be a biphasic square current wave with T2=7μs, T3=6μs, T4=8μs, A1=1 (minimum scale value of the current driver) and A2=2. It can be observed by the wave in the Fig. 6(b) that the amplitude and timing information have been correctly decoded from the stimulation data packet.



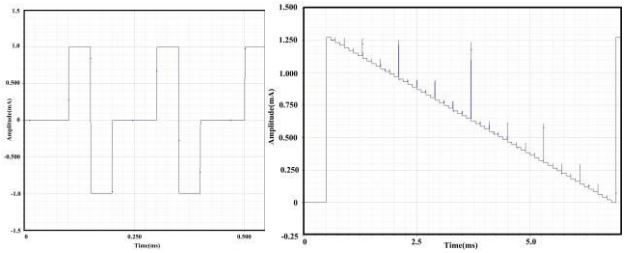
(a)



(b)

Figure 6. (a) Simulation result of SPI slave. (b) Simulation result of digital output.

B. Current Driver Verification



(a) (b)

Figure 7. (a) Current driver outputs current with amplitude of 0-1.26mA when the output of DAC varies from 0-63mA. (b) Current driver outputs biphasic current with amplitude of ±1mA.

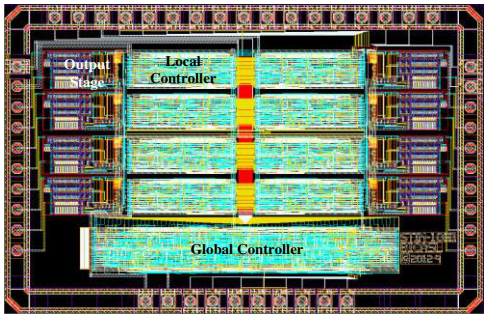


Figure 8 Layout of the chip in a 0.35μm X-FAB process.

The simulation results of the analog part are shown in Fig. 7 (a) and Fig. 7 (b). When a reference current of 1μA and a digital code of 50 are fed to the DAC, the DAC outputs 50μA current and the driver could output ±1mA biphasic current. When the digital code changes from 0 to 63, the output of DAC changes from 0-63μA, the driver outputs current with amplitude of 0-1.26mA, as shown in Fig. 7(b).The glitches in Fig. 7(b) are caused by the dynamic switching of the MOSFETs in the binary-coded DAC when the digital code changes This is not a problem in real functioning since the digital code will not change when the driver is outputting currents. The layout of the chip is shown in Fig. 8. With all the eight channels, the chip occupies approximately 12 mm^2 silicon area and is fabricated by XFAB.

V. CONCLUSION

In this paper, an 8-channel high voltage stimulator chip for a stroke rehabilitation system is introduced. The application, the specification, architecture and circuit implementation of the chip have been presented. According to the simulation results, the digital part successfully receives and decodes the stimulation parameters sent from the external controller, and the analog part could generate biphasic stimulus current of milliampere level for each channel with a supply voltage as high as 90V.

VI. ACKNOWLEDGEMENT

This work was supported partially by the Ministry of Science and Technology, China (Grant No. 2011ZX02505-002), partially by Shanghai Municipal Science and Technology Commission (Grant No. 10DZ1500600) and partially by 985 project (phase 2) of SJTU.

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