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A Programmable Analog Subthreshold Biomimetic Model for Bi-directional Communication with the Brain

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***Abstract*— In this paper, we present a hardware implementation of a second order Laguerre Expansion of Volterra Kernel (LEV) model with four basis functions. The model is versatile enough to be applied at different abstraction levels (synapse, neuron, or network of neurons) and is implemented with analog building blocks in a modular manner. These analog blocks, realized using low power subthreshold CMOS transistors, can serve as a basis for large-scale hardware systems that emulate multi-input multi-output (MIMO) spike transformations in populations of neurons. The normalized mean square error between the signals produced by the circuit LEV implementation and the ideal LEV model is 8.15%. The total power consumption of the analog circuitry is less than 33nW.**

I. Introduction and Background

Scientists have often looked to biology for ideas on how to solve a multitude of problems, which the biological world managed to tackle through years of evolution. The brain's impressive capabilities to perform complex functions, such as memory, learning, and cognition, serve as an inspiration, while also presenting a major challenge for the engineering community, since conventional computing methods have not yet allowed us to achieve such functions. One promising hypothesis on how to capture the brain's energy efficiency, robustness to noise and errors, and modularity/flexibility is building artificial systems in a biomimetic or neuromorphic way.

To construct a biomimetic system, we have to determine the essential characteristics that allow the brain to perform specific tasks. Since it is still unknown how the collective activity of populations of neurons and synapses results in higher-level brain functions, choosing the right mechanisms to include and finding the proper level of abstraction is difficult. Hence, the biomimetic model has to be flexible and modular so that it can be adjusted to account for new findings, without requiring long redesign times.

One essential feature of brain computing that is very different from traditional computing is that larger networks are made up of small modules (neurons with synapses), which are of similar composition, but are not precisely the same. Large networks in the brain with parallel inputs and outputs are made up of many of these slightly different cells, with adjustable features that are activity-dependent (potentiation, depression, etc.). These mechanisms provide for correction in the presence of error or noise, which allows the individual components to be imprecise but adjustable. Therefore, the biomimetic model can use adaptive low-power imprecise modules instead of precise but power-hungry components and satisfy the criteria of compactness, modularity (for easy scaling and modification), low power and adaptation (programmability).

The Laguerre Expansion of Volterra Kernel (LEV) model can closely approximate most biological and physiological systems. It can be applied at different levels of abstraction (synapse [1], neuron [2] or network of neurons level [3]) and, as demonstrated in this paper, it can be implemented in hardware relatively easily in a modular and programmable manner.

In this work, the main goal is to design a hardware model that is implantable in the brain (for example, for hippocampus prostheses [3]). While software models are very flexible, they are neither low-power nor portable and, therefore, do not readily lend themselves to implantable applications. Hardware systems implemented on FPGA-like platforms face the same problems, because they still demand a large area and power.

The advantages of an integrated solution are its compactness (maximum density per function as compared to FPGAs and software-based solutions) and power efficiency. The main disadvantage is that integrated circuits fulfill a specific task and once fabricated they cannot be modified. Furthermore, the design time can be long. To mitigate these problems, we include programmability, which provides more flexibility at the cost of more area. Here we present a programmable biomimetic LEV hardware model whose components are optimized for low power, and a digital subsystem that provides calibration and programmability for the analog building blocks.

II. LEV Model for Biomimetic Systems

The Laguerre Expansion of Volterra kernel model can be used to approximate a nonlinear time-invariant system with finite memory. One example of this is illustrated in [2], where the LEV model, in combination with a thresholding component, is used to capture the input–output properties of single hippocampal CA1 pyramidal neurons based on synaptically driven intracellular activity. In [3], the LEV is part of a model that captures the multiple-input multiple-output transformation of spatio-temporal patterns of the activity in the hippocampus.

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The time domain representation of a second order LEV model is described by:

$$y(t) = c_0 + \sum_{n=1}^{L} c_1(n) v_n(t) + \sum_{n_1=1}^{L} \sum_{n_2=1}^{n_1} c_2(n_1, n_2) v_{n_1}(t) v_{n_2}(t) \quad (1a)$$

where: $$v_n(t) = \int_0^{\infty} l_n(\tau) x(t-\tau) d\tau \quad (1b)$$

is the convolution of the n[th] order Laguerre function with the input $x(t)$. The coefficients c_k control the amplitudes of the Laguerre basis function and allow us to modify the model for different applications. These are found during model estimation by training the system with a sufficiently long input and output training dataset [3]. The Laguerre basis functions $l_n(t)$ can be scaled in time, depending on the time-constants of the system to be modeled, by adjusting a single parameter p.

To optimize this model for hardware implementation, it is important to minimize complexity while maintaining precision in estimation and prediction. For this application, a second order LEV model with four basis functions was found optimal [1].

III. Hardware Implementation of LEV Model

In this section we show how the LEV model can be efficiently implemented in hardware using first order filters (H_{LP}, H_{AP}), multipliers, and gain cells (weighting block) as shown in Figure 1. Because of its modularity, the implementation can easily be extended to a higher order or large-scale system. The model parameters (filter time constants and coefficients of the weighting block) are programmable, and adaptive processing techniques can be applied to train them. All analog components are implemented using transistors in the subthreshold regions with bias currents in the orders of tens to hundreds of pico Amperes.

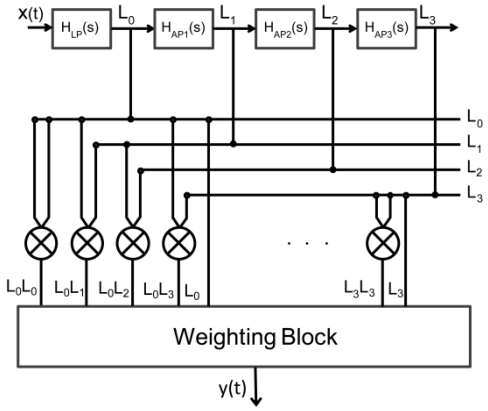

Figure 1: LEV System Overview

A. Basis Function Generation

The Laguerre basis functions $l_n(t)$ are implemented as the impulse response of a chain of continuous time analog filters with Laplace-domain transfer function:

$$H(s) = H_{LP}(s) H_{AP}^n(s) \quad (2a)$$

$$H_{LP}(s) = \frac{1}{p+s} \quad (2b)$$

$$H_{AP}(s) = \frac{p-s}{(p+s)} \quad (2c)$$

where the subscripts *LP* and *AP* denote the low-pass and all-pass nature of the sections in the frequency domain. The time scaling parameter p is determined as part of the model training.

Passive and active filter design techniques can be used to implement these sections. Since the time constants of physiological systems are large, in a passive realization, the RC constants will also be large and considerable silicon area will be needed for the resistors or capacitors. OpAmp-RC solutions suffer from the same problem. An OTA-C realization, however, produces the desired time constants via reasonably sized capacitors and very small transconductance values, which can easily be adjusted by changing the OTA bias currents.

For a model approximating a physiological signal in real-time, very small currents, preferably in the pico Ampere range, are required, calling for a subthreshold implementation. The inherently lower current levels in subthreshold translate into low power consumption of the circuit, which is critical in biomedical implant applications due to risks of overheating and/or tissue burn. It has been demonstrated that even a slight increase in the temperature of an implant can change the behavior of its surrounding cells. One example is the effect of temperature on NMDA receptors' desensitization and glutamate binding. The temperature-dependent changes of the receptor can alter the amplitude and time course of NMDA receptor mediated postsynaptic currents, which in turn influences synaptic plasticity [4].

The implementation of $H_{LP}(s)$ is shown in Figure 2 (dashed box), with transfer function:

$$H_{LP}(s) = \frac{\frac{gm_1}{C_1}}{s + \frac{gm_2}{C_1}} \quad (3a)$$

The all-pass section is implemented using the low-pass (LP) module along with additional circuitry (Figure 2).

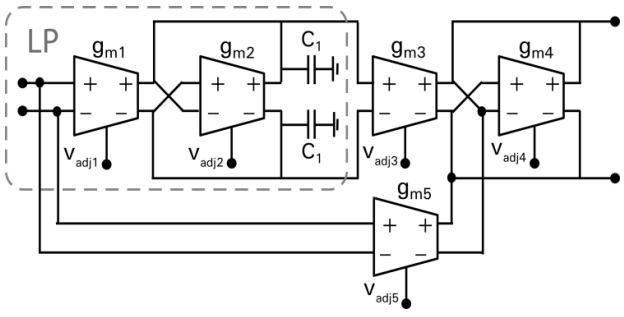

Figure 2: Controllable All-Pass Filter Implementation

The transfer function for the all-pass section is:

$$H_{AP}(s) = \frac{(\frac{gm_1 gm_3}{gm_5 C_1} - \frac{gm_2}{C_1}) - s}{s + \frac{gm_2}{C_1}} \qquad (3b)$$

The bias currents of the OTAs in the low-pass and all-pass filters can be adjusted by varying the voltage v_{adjn}.

B. Second Order LEV Component Generation

To generate the second order components of the LEV model, Gilbert cells are used for cross-multiplication. One Laguerre polynomial filter output l_{x1} is applied differentially to the gates of $M_{1a,b}$ and the other filter output l_{x2} to the gates of $M_{2a,b}$ and $M_{3a,b}$, as shown in Figure 3. The differential implementation provides robustness against noise and DC bias variations at the price of the added complexity of common-mode feedback circuitry.

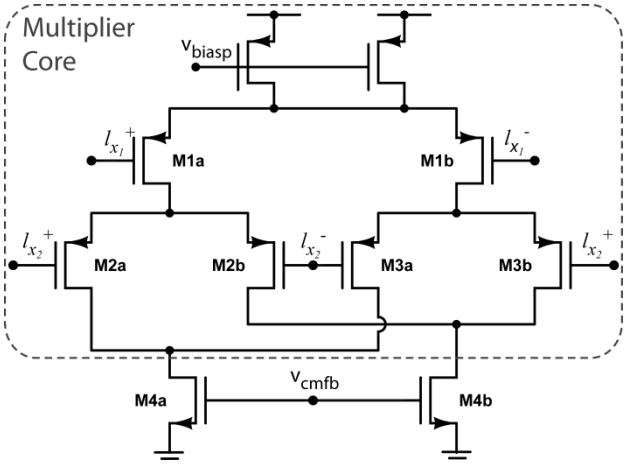

Figure 3: Gilbert cell multiplier to generate 2nd order LEV terms

C. Weighting Block Generation

Modularity and scalability play an important role in the implementation of the LEV system, because they provide flexibility and quick re-design. Therefore, to implement the weighting block, a structure similar to the Gilbert cell is used. Each coefficient c_k is multiplied by its corresponding LEV signal using the multiplier core of Figure 3.

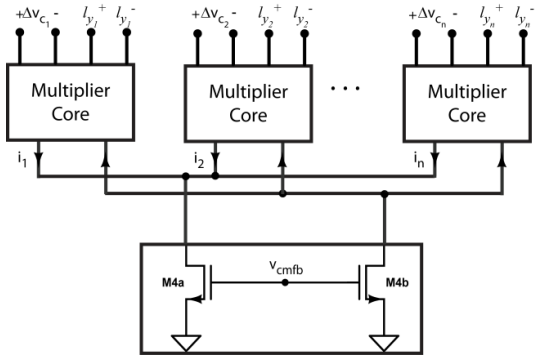

Figure 4: Weighting Block Implementation

In Figure 4 the differential dc voltage Δv_{ck} corresponds to c_k. The current outputs of the multiplier core blocks are then added together to produce the final output voltage, as the weighted sum of the Laguerre polynomials and the higher order terms. The output NMOS devices are biased at the gate by v_{cmfb}, generated by a common-mode feedback circuit (not shown).

IV. Programmability and Flexibility

A. Effects of Mismatch in Subthreshold

It can be shown that the relative mismatch of the drain currents of two identically sized transistors with the same gate voltage (such as in a current mirror), is:

$$\frac{\Delta I_D}{I_D} = -\frac{g_m}{I_D}\Delta V_T + \frac{\Delta\beta}{\beta} \qquad (4)$$

Where β denotes the current factor, g_m is the transconductance, and V_T is the threshold voltage of the transistor. Since g_m/I_D is maximized in the subthreshold region, the current mismatch is more significant in this region compared to strong-inversion [5].

The MOS drain current expression for a transistor in weak inversion with the source used as the reference is described by:

$$I_D = I_0 \frac{W}{L}\exp\left(\frac{v_{gs} - V_T}{nU_T}\right) \qquad (5)$$

where U_T is the thermal voltage and n is the slope factor which is approximately 1.33 (for the 0.13µm technology used in this work) [6]. I_D varies exponentially with V_T, which is a random variable with a normal distribution. The standard deviation of this distribution becomes larger as the CMOS process shrinks. Therefore, I_D becomes subject to significant statistical variations in sub-micron technologies. It is therefore not uncommon to have nominally identical transistors with currents that are apart by more than an order of magnitude due to the variability of V_T.

Conversely, it can be shown, using (5) that a transistor's drain current changes by a factor of 10 for approximately every 80mV change in gate voltage. Therefore we adjust the gate voltage to compensate for the often significant current mismatch in subthreshold region using a digital calibration subsystem. It can be calculated that to keep the current mismatch below 5%, the gate voltage must be programmable with a resolution of better than 1.76mV.

B. Digital Calibration for LEV Implementation

Figure 5 shows the digital subsystem used to adjust the gate voltage of each analog current source independently. It also provides the right voltage level to set the time constant p and the weighting coefficients of the LEV model. By providing these adjustable output voltages random variations in the chip can be calibrated.

A ladder of 127 resistors (R1) generates 128 voltage levels between v_high and v_low. A 7-bit analog tree mux selects the desired voltage. This voltage is then directly applied to the gate of the transistor under calibration, or the

v_{adj} input of a transconductance cell to set the correct time constant p, or to the input of a weighting multiplier core to set c_k.

For every adjustable voltage a tree mux and its associated 7-bit register will be needed. In our prototype this number is limited to around 120 independent voltages and therefore the dashed box in Figure 5 is replicated 128 times. A decoder activates one of the 128 mux/register cells via a 7-bit Gate Select word. The calibration process is a closed loop system that starts by setting a voltage at the nominal value and measuring the variable to be calibrated (e.g. the transistor current). The voltage is then changed in the right direction until the target variable is adjusted to the correct value.

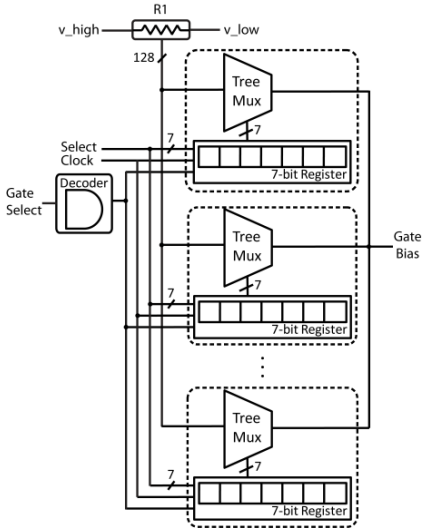

Figure 5: Digital Calibration System

To accomplish a 1.76mV resolution in the voltage using a 7-bit resistive ladder, the difference between V_high and V_low should be 225mV. This range can change a given current by a factor of 500, which is more than sufficient for calibration of transistors, based on the foundry's mismatch data. Therefore the calibration range can be reduced to obtain better step resolution, if needed.

This scalable scheme allows a multitude of methods to be utilized for more extensive calibration. For example, the bulk voltage of the PMOS devices can be changed in the same manner to compensate the threshold voltage variations.

V. Results

To evaluate the performance of the hardware LEV model, the LEV coefficients and time constants are determined using Matlab simulations. The system is trained using post-synaptic potential recorded at the soma of a hippocampal neuron in response to a 2Hz Poisson random interval train (Fig.6a). The output of the hardware LEV model simulated using Cadence Analog Design Environment is shown in Fig. 6b. As a comparison, the output of the ideal LEV model simulated in Matlab is shown in Fig. 6c. The normalized mean square error between the ideal and the subthreshold hardware implementation is 8.15%. The power consumption of each component of the system is shown in Table 1. The total power consumption of the system is 32.3nW.

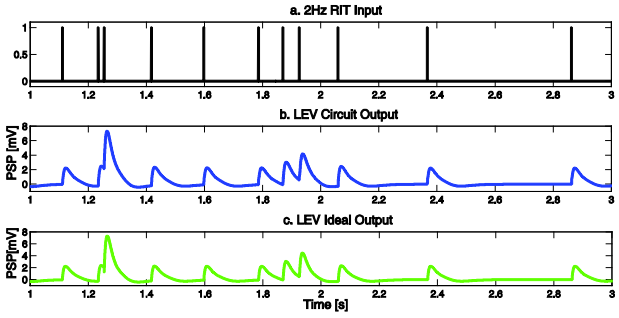

Figure 6: a) Poisson random input stimulus, b) output of the hardware LEV model (coefficients c_k and parameter p determined using Matlab training simulations, c) output of the ideal (Matlab) approximation

The digital subsystem is only on during calibration and, therefore, does not contribute to the overall power consumption of the system. The total chip area is 1mm x 1mm in 0.13µm Cypress technology, where the analog part occupies an area of 0.3mm x 0.3mm.

Hardware Component	Power Consumption [nW]
OTA	.062
Low-Pass Filter	.062
All-Pass Filter	.248
Gilbert Multiplier	.682
Gilbert CMFB	.620
Weighting Block	9.461
Weighting Block CMFB	8.768
LEV System	32.3

Table 1: Power consumption of subthreshold analog LEV circuitry

VI. Conclusion

We have implemented a 2nd order LEV model in subthreshold CMOS analog hardware. The hardware model is programmable and can be calibrated using a digital subsystem. This system serves as a foundation for large-scale LEV systems.

Acknowledgment

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