35th Annual International Conference of the IEEE EMBS
Osaka, Japan, 3 - 7 July, 2013

Neural Recording Front-End IC Using Action Potential Detection and Analog Buffer with Digital Delay for Data Compression

Lei Liu, Lei Yao, Xiaodan Zou, Wang Ling Goh, *Senior Member, IEEE*, and Minkyu Je, *Senior Member, IEEE*

***Abstract*— This paper presents a neural recording analog front-end IC intended for simultaneous neural recording with action potential (AP) detection for data compression in wireless multichannel neural implants. The proposed neural recording front-end IC detects the neural spikes and sends only the preserved AP information for wireless transmission in order to reduce the overall power consumption of the neural implant. The IC consists of a low-noise neural amplifier, an AP detection circuit and an analog buffer with digital delay. The neural amplifier makes use of a current-reuse technique to maximize the transconductance efficiency for attaining a good noise efficiency factor. The AP detection circuit uses an adaptive threshold voltage to generate an enable signal for the subsequent functional blocks. The analog buffer with digital delay is employed using a finite impulse response (FIR) filter which preserves the AP waveform before the enable signal as well as provides low-pass filtering. The neural recording front-end IC has been designed using standard CMOS 0.18-μm technology occupying a core area of 220 μm by 820 μm.**

I. Introduction

In neuroscience research and clinical neuroprosthesis, simultaneous activities of a large population of neurons have to be recorded, transmitted and processed for neural pattern classification and recognition [1], [2]. Conventionally, a complete set of recorded raw data is preserved for data analysis [3]. However, for the recently emerging implantable wireless neural recording microsystem such as in Fig. 1, the compression of this large volume of data becomes of great necessity to reduce the effective transmission data rate so as to lower the power consumption of the entire recording implant [4], which is the key to minimize the required power and size of the data transmitting coils, thereby alleviating the excessive heat dissipation caused by the implanted electronics.

In the neural recording system, the neural activity is recorded as action potentials (APs) which is a pulsatile signal with a peak-to-peak amplitude ranging from 50 to 500 μV and a power spectrum that lies between 300 Hz and 5 kHz. Neural activities are decoded from these recorded APs using different decoding methods such as the firing rate decoding, temporal decoding and population decoding [5]. Since AP represents the complete neural information, by detecting the APs and transmitting only APs, not only the signal integrity is preserved, the data volume required for neural information decoding [6] is also reduced.

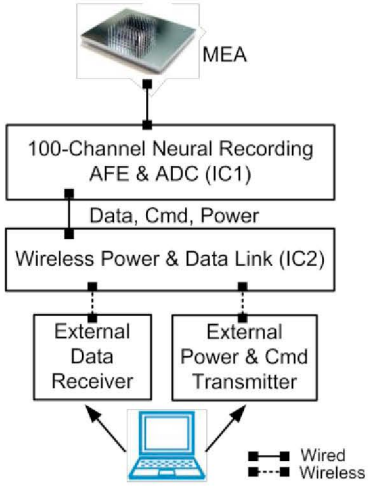


Figure 1. Typical system architecture of the fully implantable wireless neural recording microsystem.

In [7], only the occurrence of APs is detected, resulting in a data rate of 330 kbps from 100 recording channels. However, recording of a complete AP waveform is essential to better understand brain functionality and to predict the intended movements. In [8] and [9], the neural AP detection is conducted in digital domain and it outputs only the detected APs for transmission, achieving more than 90% data compression. It has relatively accurate control in AP waveform preservation since it performs AP detection after data quantization. However, the system requires large on-chip memory and computation resources to store and process the quantized data from all the channels, and consumes a significant amount of power among the analog-to-digital converters (ADCs) that are constantly on. In [6], the AP is detected in the analog domain before quantization and an analog delay of 600 μs is inserted in the front-end chain to preserve the AP waveform before crossing threshold voltages. No memory is required and the ADCs can be switched off using this AP detection strategy. However, the time delay implemented using the analog filter can be significantly affected by process variation and mismatch, which makes the preservation of complete AP waveform not guaranteed, especially when the recording is performed from a large

This work was supported by the Science and Engineering Research Council of A*STAR (Agency for Science, Technology and Research), Singapore, under SERC grant number: 1021710162.

L. Liu, L. Yao, and M. Je are with the Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), Singapore (jemk@ime.a-star.edu.sg). L. Liu is also with the Nanyang Technological University, Singapore (e-mail: liul0021@ntu.edu.sg). M. Je is also with the National University of Singapore, Singapore.

X. Zou was with the Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), Singapore. X. Zou is now with Qualcomm CDMA Technologies Asia-Pacific Pte. Ltd.

W. L. Goh is with the Nanyang Technological University, Singapore.

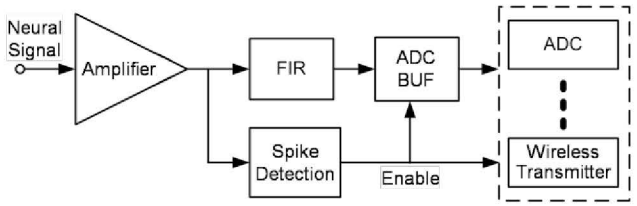


Figure 2. Block diagram of neural recording front-end.

number of channels simultaneously. Therefore, an AP detection method providing precise preservation of AP waveform without requiring large memory and computation resources or power penalty is highly demanded.

In this work, we present a neural recording front-end IC with AP detection using a discrete-time finite impulse response (FIR) filter as a delay buffer to perform data compression while ensuring preservation of the AP waveform. The AP detection is carried out in analog domain before data quantization so that the ADCs and their driving buffers can be powered down during the non-AP period. The time delay for preservation of the complete AP waveform is implemented using the FIR filter in discrete-time domain where the time delay is defined by the clock period that is accurate and robust to process variation and mismatch.

II. System Architecture

Fig. 2 depicts the block diagram of the proposed neural recording front-end IC which comprises three main building blocks: (1) a low-noise neural amplifier for amplifying the neural signal acquired through the multi-electrode array (MEA) by 100 times; (2) an AP detection circuit that detects the AP and generates triggering signal to enable its subsequent functional blocks such as buffers, ADCs, multiplexers, and circuits in the RF transmitter; and (3) an analog buffer with digital delay implemented using an FIR filter to preserve the complete AP waveform.

III. Circuit Implementation

A. Low-Noise Neural Amplifier

One of the most critical components in the design of the neural recording front-end IC is the low-noise neural amplifier as it contributes the most to the overall input-referred noise performance of the front-end IC. The schematic diagram of the low-noise neural amplifier used in this work is shown in Fig. 3. A capacitive feedback topology is chosen to effectively block the large input DC offset caused by the tissue-electrode interface while using pseudo-resistors to stabilize the DC bias at the input nodes. The gain of the amplifier is determined by the ratio of C_1/C_2, where $C_1 = 20$ pF and $C_2 = 200$ fF. The value of the pseudo-resistor R_{DC} together with C_2 determines the high-pass cutoff frequency of the neural amplifier. It is set to be 300 Hz so that the AP waveform can be recorded without being affected by the LFP signal. The low-pass cutoff frequency is defined by the bandwidth of the operational transconductance amplifier (OTA), which is designed to be 5 kHz so that the out-of-band noise can be filtered out. A fully differential current-reuse OTA [10] is used to achieve an optimal power-noise trade-off and hence a very low value of noise efficiency factor (NEF). The current-reuse technique is employed at the input stage of the OTA to improve the transconductance efficiency so as to achieve low power and low noise at the same time.

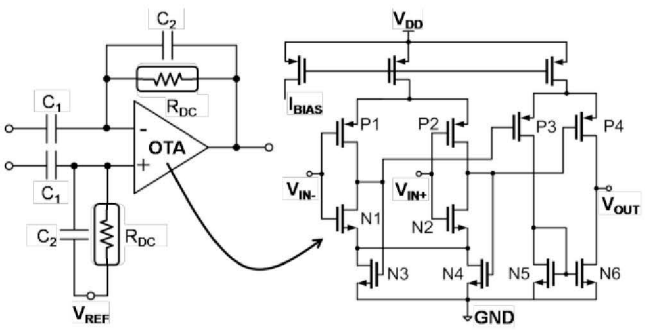


Figure 3. Circuit schematic of the low-noise neural amplifier.

B. Adaptive AP Detection Circuit

Fig. 4(a) shows the block diagram of the AP detection circuit. In order to avoid any influence of the offset generated by the neural amplifier on the AP detection, the neural amplifier is AC-coupled to the AP detection circuit. A pseudo-resistor is used with a capacitor of 500 fF to implement a high-pass cutoff frequency of 100 Hz, resulting in full coverage of the entire AP signal bandwidth. The AC-coupled signal is further processed by two comparators—one for upper threshold detection and the other for lower threshold detection. The outputs from the two comparators are fed to an OR gate to generate a combined output as an enable signal. The enable signal is used to control

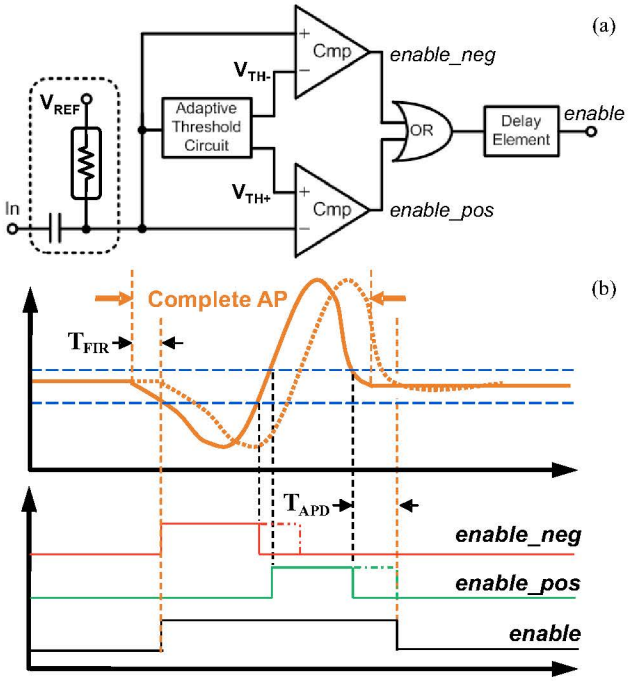


Figure 4. (a) Block diagram and (b) operation waveforms of the spike detection circuit.

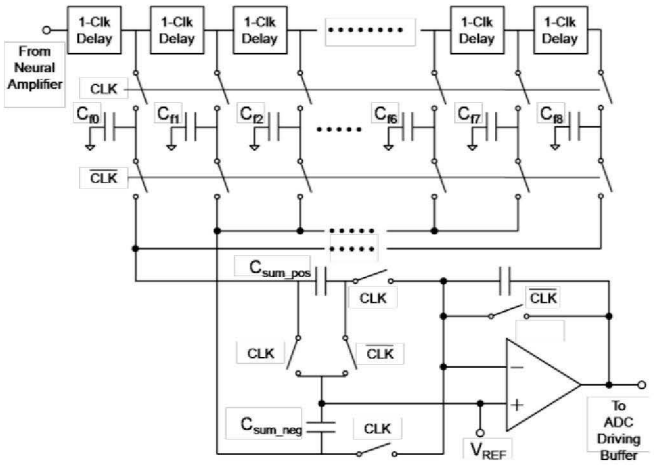
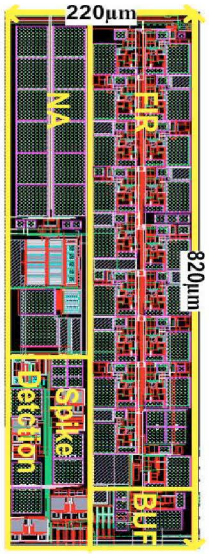


Figure 5. Block diagram of the FIR filter.



System	
Technology	0.18μm CMOS
Area	220μm × 820μm
Low-Noise Neural Amplifier	
Gain	40 dB
Bandwidth	5kHz
Input noise	5 μV/√Hz
Power @ 1V	1μW
AP Detection Circuit	
Threshold Voltage	Automatic adaptive
Power @ 1V	0.6μW
FIR filter	
Sampling Frequency	20kHz
Bandwidth	5.7kHz
Power @ 1V	5μW

Figure 6. Layout and simulated performance summary of the designed neural recording front-end IC.

the subsequent quantization and wireless transmission circuit blocks. The threshold voltages, V_{TH+} and V_{TH-}, for the two comparators are produced by an adaptive threshold generation circuit which automatically sets the thresholds based on the noise level of the amplified neural signal. Typical operation waveforms of the AP detection circuit are shown in Fig. 4(b). The output of the OR gate covers only a part of the complete AP waveform where the signal value exceeds either one of the threshold voltages. To preserve the complete AP waveform, a delay time of T_{APD} = 400 μs is applied to the falling edges of both *enable_pos* and *enable_neg* using eight D flip-flops (DFFs) connected in series and the AP waveform before the onset of *enable* is stored using an analog buffer with a digital delay of T_{FIR} = 300 μs. T_{APD} and T_{FIR} are both empirically determined by observing the real neural waveforms recorded from rat brains [10], [11]. As a result, the entire information of the AP waveform is well preserved for further storage, transmission, and processing.

C. Analog Buffer with Digital Delay

The analog buffer is implemented using an FIR filter shown in Fig. 5. The main role of the FIR filter in the system is to provide a well-defined linear delay to the neural signal so that the complete AP waveform can be passed to the subsequent blocks when the enable signal is triggered. The extra advantage of using the FIR filter as a delay buffer is that the out-of-band noise can be further suppressed by the sharp filtering characteristics. By estimating the time delay required for recording the initial part of the AP waveform from the neural signal recorded *in vivo*, an 8-tap FIR filter is implemented.

Two conventional switched-capacitor buffers are connected in series to form a one-clock delay cell. Different filter coefficients are realized using switched capacitors with different weights, which comprise a different number of multiple unit capacitors connected in parallel. The multiplication of the signal with the filter coefficient is accomplished via charge redistribution among the switched capacitors. First, the amplified neural signal is sequentially sampled on weighted capacitors (C_{f0}, C_{f1}, ···, C_{f8}) by a set of switches. Next, the charges stored on the weighted capacitors are added together by another set of switches. To realize both positive and negative coefficient values, the switched capacitors are grouped into one array of positive coefficients and the other array of negative coefficients. The arrays of positive and negative coefficients are subtracted by the following summing switched-capacitor amplifier. All the switches used in the design are implemented using transmission gates. The charge injection and clock feedthrough errors in the FIR filter are minimized using small-size transistors with two dummy components at both sides of the switch.

IV. Simulation Results

The neural recording analog front-end IC was designed in a standard 0.18-μm CMOS technology. It occupies a core area of 220 μm by 820 μm and does not require any off-chip component. The IC layout is shown in Fig. 6 together with a summary of its simulated performances. The neural amplifier operates with a 1-V supply, from which it draws 1 μA providing 40-dB gain with a low-pass cutoff frequency of 5 kHz. The FIR filter consumes 5.6 μA and has a bandwidth of 5.7 kHz. The AP detection circuit consumes another 0.6 μA from the 1-V supply. Although the AP detection and delay circuit consumes extra power compared to the conventional neural recording front–end design, the power saved in data storage, transmission and processing functions due to the reduced data volume should be much more significant [4], [11].

To verify the functionality of the proposed neural recording front-end IC, simulations were performed using the actual neural signals pre-recorded from anesthetized rats [10], [11] as the input of the designed IC. Fig. 7 shows the simulated outputs of the FIR filter and the spike detection circuit versus the pre-recorded neural signal input. Fig. 8 shows the zoom-in

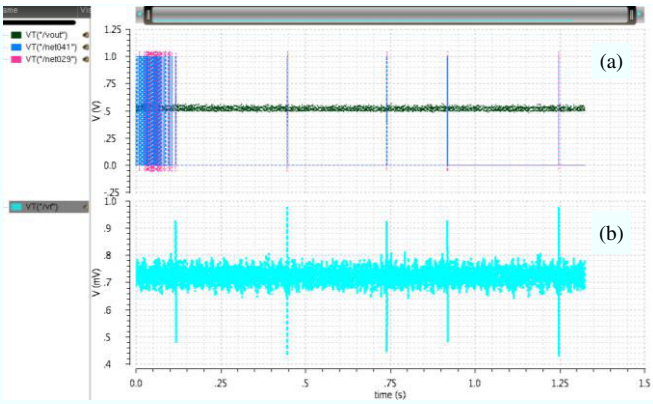


Figure 7. (a) Simulated outputs of the FIR filter and the spike detection circuit with (b) the pre-recorded neural signal from anesthetized rats (1.38-s long trace) as the input to the front-end IC.

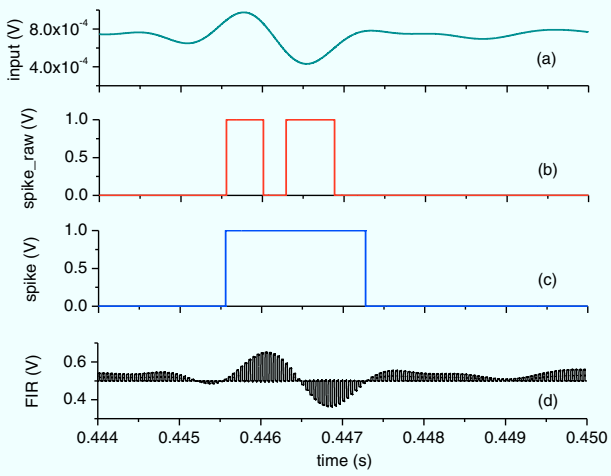


Figure 8. Zoomed-in simulation results with the pre-recorded neural signal from rats (6-ms short trace) as the input: (a) input neural signal, (b) spike detection output before the delay element, (c) spike detection output after the delay element, (d) FIR filter output.

view of the simulation results. Fig. 8(a) is the input neural signal and Fig. 8(b) is the spike detection output before the delay element. The two pulses in Fig. 8(b) are resulted from the positive and negative phases of the neural spike, respectively. Fig. 8(c) shows the enlarged spike recording window on the FIR output (Fig. 8(d)) to preserve the complete AP waveform information. Table I provides a comparison between the different data compression techniques used for implantable wireless neural recording microsystems.

V. Conclusion

A neural recording analog front-end IC with lossless data compression based on spike detection and adaptive waveform windowing has been demonstrated for fully implantable multichannel wireless neural recording systems. Wireless transmission of the recorded neural signal waveform is enabled only during the presence of neural spikes, and hence the data rate can be effectively reduced by more than 10 times [4] compared to the conventional wireless neural recording system. Furthermore, the complete neural AP information is securely preserved with adaptive AP recording windows. The functionality of the proposed recording front-end IC design has been verified with intensive simulation using actual neural signal waveforms pre-recorded *in vivo*.

Table I. Comparison of Data Compression Techniques.

	Domain	Waveform preservation	Recording time per spike	Scalability
[4]	Digital	Partial	1 ms	Yes
[6]	Analog	Partial	2 ms	Restricted
[8]	Digital	Partial	2 ms	Yes
[9]	Digital	Poor	-	Yes
This work	Analog	Complete	Adaptvie	Yes

References

[1] J. Wessberg, C. Stambaugh, J. Kralik, P. Beck, M. Laubach, J. Chapin, J. Kim, S. Biggs, M. Srinivasan, and M. Nicolelis, "Real-Time Prediction of Hand Trajectory by Ensembles of Cortical Neurons in Primates," *Nature*, vol. 408, pp. 361–365, Nov. 2000.

[2] R. H. Olsson, D. L. Buhl, A. M. Sirota, G. Buzsaki, and K. D. Wise, "Brain-Machine Interfaces: Past, Present and Future," *Trends in Neurosciences*, vol. 29, pp. 536–546, 2006.

[3] M. Chae, W. Liu, Z. Yang, T. Chen, J. Kim, M. Sivaprakasam, and M. Yuce, "A 128-Channel 6mW Wireless Neural Recording IC with On-the-Fly Spike Sorting and UWB Transmitter," in *IEEE International Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*., Feb. 2008, pp. 146–147.

[4] A. Bonfanti, M. Ceravolo, G. Zambra, R. Gusmeroli, T. Borghi, A. S. Spinelli, and A. L. Lacaita, "A Multi-Channel Low-Power IC for Neural Spike Recording with Data Compression and Narrowband 400-MHz MC-FSK Wireless Transmission," in *Proc. IEEE European Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2010, pp. 330–333.

[5] J. Gautrais and S. Thorpe, "Rate Coding versus Temporal Order Coding: a Theoretical Approach," *Biosystems*, vol. 48, no. 1–3, pp. 57–65, Nov. 1998.

[6] B. Gosselin and M. Sawan, "An Ultra Low-Power CMOS Automatic Action Potential Detector," *IEEE Trans. Neural Systems and Rehabilitation Engineering*, vol. 17, no. 4, pp. 346–353, Aug. 2009.

[7] R. R. Harrison, "A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural Recording System," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 123–133, Jan. 2007.

[8] B. Gosselin, A. E. Ayoub, J. F. Roy, M. Sawan, F. Lepore, A. Chaudhuri, and D. Guitton, "A Mixed-Signal Multichip Neural Recording Interface with Bandwidth Reduction," *IEEE Trans. Biomedical Circuits and Systems,* vol. 3, no. 3, pp. 129–141, Jun. 2009.

[9] R. H. Olsson III and K. D. Wise, "A Three-Dimensional Neural Recording Microsystem with Implantable Data Compression Circuitry," *IEEE J. Solid-State Circuits,* vol. 40, no. 12, pp. 2796–2804, Dec. 2005.

[10] L. Liu, X. Zou, W. L. Goh, R. Ramamoorthy, G. Dawe, and M. Je, "800 nW 43 nV/√Hz Neural Recording Amplifier with Enhanced Noise Efficiency Factor," *Electronics Lett.*, vol. 48, no. 9, pp. 479–480, Apr. 2012.

[11] K. Cheng, X. Zou, J. H. Cheong, R.-F. Xue, Z. Chen, L. Yao, H.-K. Cha, S. J. Cheng, P. Li, L. Liu, L. Andia, C. K. Ho, M.-Y. Cheng, Z. Duan, R. Rajkumar, Y. Zheng, W. L. Goh, Y. Guo, G. Dawe, W.-T. Park, and M. Je, "100-Channel Wireless Neural Recording System with 54-Mb/s Data Link and 40%-Efficiency Power Link," in *IEEE Asian Solid State Circuits Conf. (A-SSCC) Dig. Tech. Papers*, Nov. 2012, pp. 185–188.

[12] R. R. Harrison, "A Low-Power Integrated Circuit for Adaptive Detection of Action Potentials in Noisy Signals," in *Proc. Ann. Int. Conf. IEEE Engineering in Medicine and Biology Society (EMBC)*, Sep. 2003, pp. 3325–3328.