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Performance of a High-Speed Transcutaneous Link with Error Correction Coding

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Abstract— **Several low-power communication strategies have been studied for interfacing with cortical implants via mutual inductance links. In this paper, we consider performance optimization strategies for a mutual-inductance link based on the Pulse Harmonic Modulation method. We consider two enhancements that may allow for increased throughput in the PHM system. First, a low-power error-correcting code is used to improve the system's robustness against noise, timing jitter and other non-ideal factors. Second, the system is adapted for multi-level modulation as a means of increasing the data rate. Our results characterize each systems' bit error rate as a function of pulse jitter, power interference and comparator offset.**

I. Introduction

Near-Field inductive links have been extensively studied for short range data and power transmission [1], [2]. In most designs, power and data are delivered to an implanted device through a single mutual inductance channel. The channel itself is formed by near-field magnetic coupling between a coil located inside the head, and a second coaxial coil located outside the body. In most cases, the data channel is formed by modulating the implant's power signal. In order to maximize power transfer, most designs require a resonant frequency on the order of 1 to 10MHz, which limits the achievable data rates in the system.

In order to improve the throughput of cortical interfaces, researchers recently began to examine multi-band inductive links (MILs) which utilize separate channels for power and data transfer [3]–[5]. Inanlou et al. recently described an MIL communication solution known as Pulse Harmonic Modulation (PHM), in which data is communicated by exciting harmonic resonance in the data channel [6]. In the PHM system, a binary '1' is communicating by emitting a brief *initiation pulse*, which stimulates a resonant response from the inductive link. After a delay time t_d, a *suppression pulse* is emitted to terminate the resonant response via destructive interference.

Pulse based communication – which include PHM – are emerging as an attractive low-power data transfer solution for biomedical implants, since they can be more power efficient than carrier based systems [6], [7]. Currently, two pulse based systems are mainly being investigated: Impulse Radio Ultra Wide-Band (UWB) and PHM. UWB has been shown to achieve fast speeds suitable for high data rates neuroprostheses [8], [9]. However, a drawback of this system is that it employs a low Q data link, resulting in high vulnerability to interferences and coil separation distances [6], [9]. On the other hand, PHM systems can be employed with high Q links, which may allow for simpler receiver design, with correspondingly lower power consumption.

In this article, we consider techniques to increase the data rate and robustness of PHM-based MIL systems. Specifically, we consider the impact of cross-link interference between the data and power channels, pulse-time jitter in the transmitting device, and miscalibration of the threshold detector in the receiving device. These effects are considered for the original PHM system described by Inanlou [6], and for a new multi-level PHM configuration. Performance is measured by evaluating bit error rate (BER) curves over a range of system parameters. We furthermore evaluate the performance with and without the inclusion of a low-power error-correcting code (ECC) decoder that was recently described by Winstead and Rodrigues [10].

The remainder of this paper is organized as follows. Sec. II describes the construction of simulation models and system design parameters. Sec. III presents the results of our performance simulations, including cross-link interference, threshold miscalibration and multi-level operation. Finally, Sec. IV offers a discussion of the results and conclusions.

II. Experimental Design

A PHM-based MIL system was modeled using the Verilog-AMS behavioral verification language. Fig. 1 depicts the system architecture, which includes a multi-band coil interface based on the "Figure-8" model described by Jow and Ghovanloo [3], [4], a PHM modulation strategy described by Inanlou [6], and a low-complexity ECC decoder similar to a design described by Winstead [10]. The decoder uses the Gallager-A algorithm [11] for a (3,6) low-density parity check (LDPC) code of length $N = 64$. The selected code has rate $1/2$, meaning it inserts one parity-check bit for every data bit. This reduces the effective data rate by a factor of two, but improves the system's robustness as examined in Sec. III.

Fig. 2 shows a detailed model of the PHM receiver model, which includes a low-noise amplifier (LNA), a rectifier and low-pass filter (LPF), and a threshold detector. The MIL's physical parameters are shown in Table I. To maximize power transfer, the power signal was designed to have a low frequency ($f_p = 125$kHz) and high amplitude ($V_p = 100V$). The power link parameters R1, L1, L2 and k_{12} were selected

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from the power efficient link design presented in [3], and the capacitances C1 and C2 were chosen to make the power link LC tanks to resonate at 125kHz. The data link parameters R3, L3, R4, and L4 were selected from the PHM system presented in [6], and the coupling coefficients that affect the data link k_{14}, $k_{12}k_{24}$, and k_{34} were obtained from the Figure-8 MIL described by Jow [4].

The Figure-8 MIL was modeled based on the following equations:

$$\begin{aligned} V_1(t) &= L_1\frac{dI_1}{dt} + M_{12}\frac{dI_2}{dt} \\ V_2(t) &= L_2\frac{dI_2}{dt} + M_{12}\frac{dI_1}{dt} \\ V_3(t) &= L_3\frac{dI_3}{dt} + M_{34}\frac{dI_4}{dt} \\ V_4(t) &= L_4\frac{dI_4}{dt} + M_{14}\frac{dI_1}{dt} + M_{24}\frac{dI_2}{dt} + M_{34}\frac{dI_3}{dt} \end{aligned} \quad (1)$$

where L_a is the inductance of coil a, and M_{ab} is the mutual inductance between coil a and coil b. These equations were implemented in Verilog-A using standard methods as described by Kundert [12], [13]. The resistors' thermal noise contributions were also modeled in Verilog-A by including a noise voltage source in series to each resistor.

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The pulse pattern generator (PPG) and receiver model of the bi-level PHM system presented in this article are based on the designs presented in [6]. In order to model the four-level PHM system, the bi-level PPG and the bi-level receiver comparator were modified. The four-level PPG was modeled to transmit 4 different initiation pulse (IP) amplitudes depending on the two-bits data transmitted, as shown in Table II. In the receiving device, the four-level

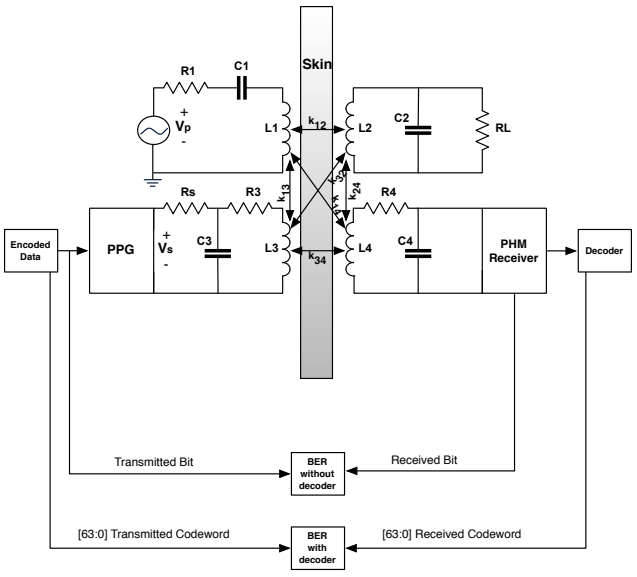

Fig. 1. Bi-level Figure-8 MIL based PHM system including a length-64 Gallager-A error correcting decoder.

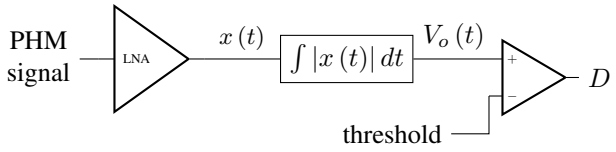

Fig. 2. PHM receiver architecture. The PHM signal is sampled from the data receiver coil L4, processed by an energy detector consisting of low-noise amplifier (LNA), rectifier and low-pass filter (indicated by the integrator), and a threshold detector. In the four-level PHM case (not shown), the threshold detector discriminates among three threshold levels.

TABLE I
PARAMETERS OF THE SYSTEM ARCHITECTURE USED TO VALIDATE THE FIGURE-8 MIL

f_p	125kHz	RL	50Ω	R4	1300mΩ
R1	50Ω	Rs	50Ω	C4	82.7pF
C1	27.48nF	C3	225pF	k_{12}	0.16688
L1	59μH	R3	412mΩ	k_{14}	0.00012
L2	6.55μF	L3	105nF	$k_{12}k_{24}$	0.0004
C2	247.50nF	L4	281nF	k_{34}	0.011

symbol detector was modeled as a simple threshold detector with three thresholds.

TABLE II
FOUR-LEVEL PPG SYMBOLS, INITIATION PULSE AMPLITUDES (V_i), PULSE DELAY TIMES (t_d) AND SYMBOL THRESHOLD FOR THE RECEIVED SAMPLES (V_o).

Data Transmitted	V_i	t_d	V_o thresholds
00	0	N/A	$V_o < 350$mV
01	2	109.9ns	$350\text{mV} < V_o < 1\text{V}$
10	4	108.26ns	$1\text{V} < V_o < 1.6\text{V}$
11	6	107.8ns	$V_o > 1.6\text{V}$

In [6], it is suggested that as long as the normalized amplitude of the suppression pulse (SP) is $0.8V_i$, a t_d of 106ns would be optimal for eliminating inter-symbol interference (ISI). However, while designing the four-level system, it was observed that the optimal t_d varies with respect to IP amplitude, even if the SP amplitude remains fixed at a normalized amplitude. Therefore, the four-level PPG was designed to adapt t_d to different values for each symbol. The t_d values for each symbol are indicated in Table II, and the normalized SP amplitude was fixed to $0.8V_i$.

The need for an adaptable t_d is demonstrated by the simulation results in Fig. 3, which show the signal that appears across the receiver data coil L4. When t_d is fixed to each of the optimal values of Table II, and also when t_d is varied according to Table II. From this figure, it can be observed that even though a certain t_d may be optimal when used with a specific IP amplitude, it can still generate high ISI when used with a different IP amplitude.

III. RESULTS

A. Bi-Level PHM Power Interference Characterization

In order to characterize the effects of inter-link interference in the MIL system, the BER was evaluated while varying the coupling coefficient k_{14} between the transmitting power

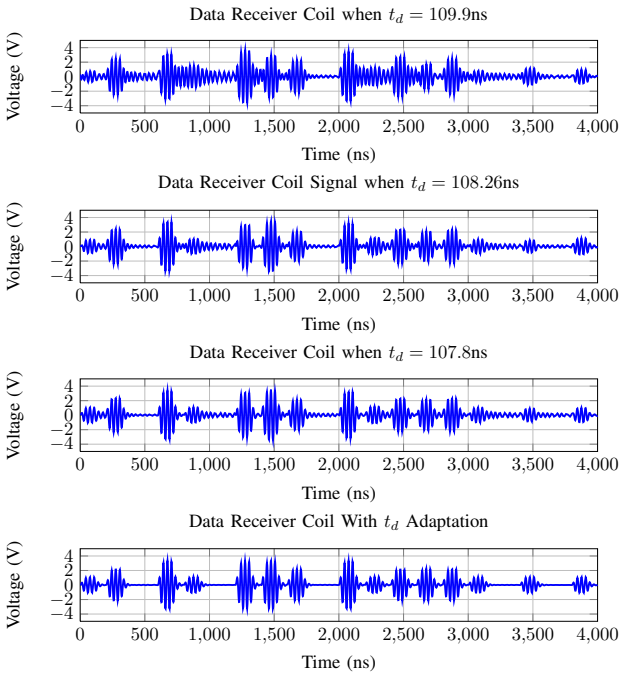

Fig. 3. Four-Level PHM system performance with t_d adaptation.

coil and the receiving data coil. This parameter is known to vary if the coils are not perfectly aligned [4]. In order to characterize the power interference of the bi-level PHM system, the PPG clock jitter, the power signal amplitude, and the receiver's RMS noise voltage were held constant at 0.3ns, 100V, and 2.34mV, respectively. The results of these simulations are shown in Fig. 4, which shows BER performance with and without the included ECC decoder. From Figure 4, it can be observed that as k_{14} increases, the BER of the system also increases. Also, ECC is observed to significantly improve the robustness of MILs against power interference. In fact, without using ECC, the system exhibits an "error floor," defined as a minimum BER that cannot be improved regardless of k_{14}. By using the low-complexity ECC, the error floor is either eliminated or reduced to an unobservably low value.

B. Comparator threshold adaptation

From Figure 5, it can be observed that as k_{14} increases, the modulation of the LPF output signal by the power carrier strengthens. This interference asymmetrically increases the probability of a $0 \rightarrow 1$ error in the receiver. This effect may be partly compensated by adapting the symbol detection threshold in the receiver.

Figure 6 shows the effect of varying the comparator threshold voltage on the BER of the system, when $k_{14} = 2.7 \times 10^{-3}$ and when $k_{14} = 3 \times 10^{-3}$. From this figure it can be noticed that the optimal comparator threshold increases as k_{14} increases. Therefore, suggesting that a comparator that would adapt its threshold to changes in k_{14}, would enhance decoder performance, and robustness against factors that could increase MILs power interference, such as coil misalignments.

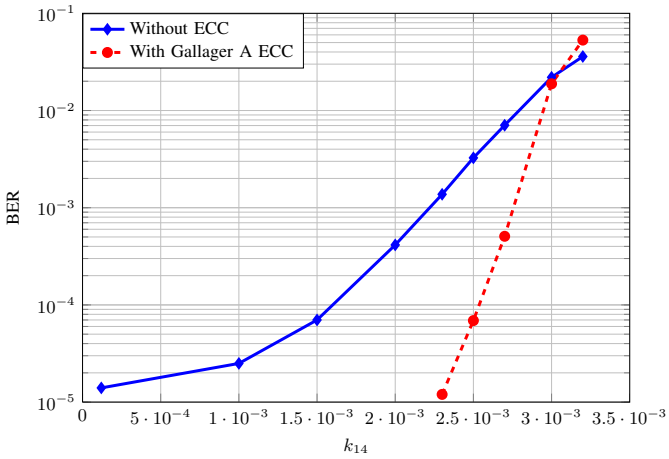

Fig. 4. BER of the bi-Level PHM system under cross-link interference from the power channel.

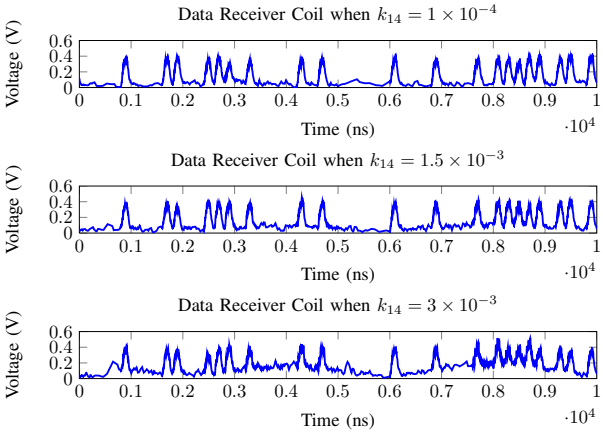

Fig. 5. Power channel interference waveforms appearing on the low-pass filter output V_o.

C. Effects of clock jitter in the bi-level and four-level PHM systems

The PHM system relies on precise timing between initiation and suppression pulses. If the suppression pulse arrives slightly early or late, then the link's resonant response will not be fully terminated, resulting in inter-symbol interference that degrades communication performance. The delay between initiating and suppressing pulses, t_d, is controlled by a digital clock. All digital clock generators are subject to a small random timing error known as *jitter*. As the RMS jitter increases, t_d becomes increasingly unstable, leading to higher ISI.

In order to characterize the effects of jitter in the PHM system's performance, the BER was evaluated for the bi-level and four-level PHM systems while varying the PPG's RMS jitter time. During these simulations, the receiver's RMS noise, the inter-channel coupling k_{14}, and the power signal amplitude were held constant at 2.34mV, 1.2×10^{-4}, and 100V, respectively.

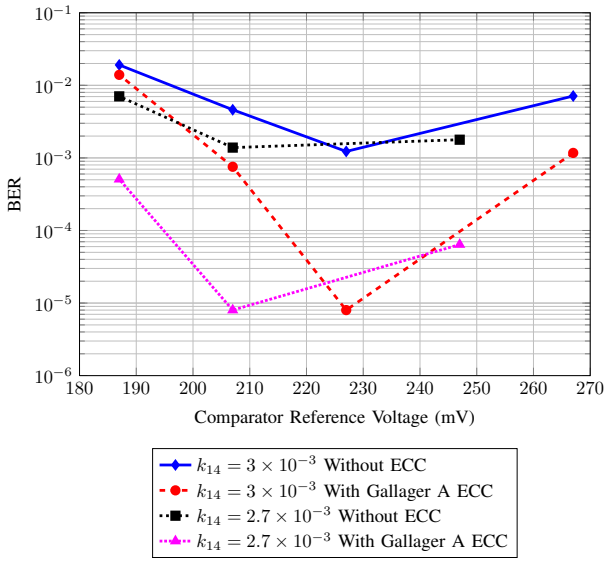

Fig. 6. BER in the presence of power interference while varying the symbol detector threshold.

Fig. 7 shows the effect of increasing the RMS jitter in the BER of the bi-level and the four-level systems. As it can be noticed, the four-level system is more sensitive to clock jitter than the bi-level system. This characteristic was expected, since the four-level system presented transmits IP's that are higher in amplitudes than the transmitted by the bi-level system, which in turn can cause ISI that are larger in magnitude.

It is expected that as PHM levels of transmission increase, the sensitivity to clock jitter also increases, since increasing levels leads to either increasing IP amplitudes which can lead to larger ISI, or, reducing the difference between comparator threshold voltages, which increases the probability of error.

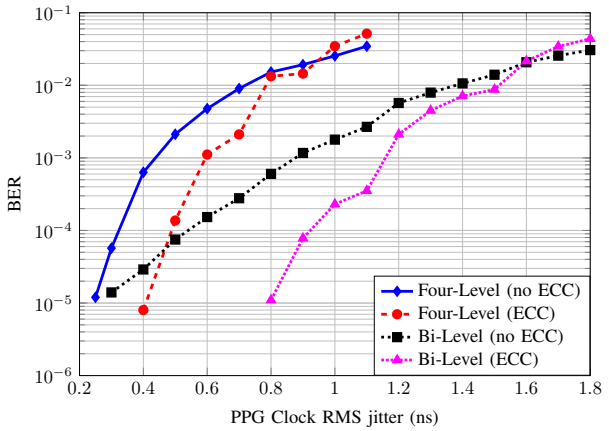

Fig. 7. PPG clock jitter characterization.

IV. Conclusion

The results described in Sec. III demonstrate that the PHM system is sensitive to variation in k_{14}, which can be interpreted as a sensitivity to coil misalignment. This sensitivity is significantly improved by the use of ECC, however the ECC reduces the data rate due to the overhead of parity-check bits. By utilizing a four-level modulation, the system's data rate is again improved. Based on the results of Fig. 7, we may conclude that the four-level system with ECC is more robust than the original uncoded bi-level system when the RMS jitter is below 500ps. It was also shown, however, that realizing the four-level system requires adaptive pulse timing which could complicate both the transmitter and receiver designs.

From the power interference characterizations, it was concluded that as the coupling coefficient k_{14} increases, the effects of power interference can be partially compensated by adapting the symbol detector's threshold voltage. Therefore, it is assumed that a comparator that could adapt its reference voltage to changes in k_{14} would improve the robustness of ECC-based PHM systems against factors that can increase power interference, such as coil misalignments.

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