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A CMOS Enhanced Solid-State Nanopore Based Single Molecule Detection Platform

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Abstract— **Solid-state nanopores have emerged as a single molecule label-free electronic detection platform. Existing transimpedance stages used to measure ionic current nanopores suffer from dynamic range limitations resulting from steady-state baseline currents. We propose a digitally-assisted baseline cancellation CMOS platform that circumvents this issue. Since baseline cancellation is a form of auto-zeroing, the 1/f noise of the system is also reduced. Our proposed design can tolerate a steady state baseline current of 10μA and has a usable bandwidth of 750kHz. Quantitative DNA translocation experiments on 5kbp DNA was performed using a 5nm silicon nitride pore using both the CMOS platform and a commercial system. Comparison of event-count histograms show that the CMOS platform clearly outperforms the commercial system, allowing for unambiguous interpretation of the data.**

I. INTRODUCTION

Label-free single-molecule analysis has transformative potential in personalized medicine, molecular biology and drug-discovery. Inspired by biology, nanopores have recently emerged as a viable single-molecule electronic detection platform [1], [2]. A nanopore is an extremely tiny hole, a few nanometers in diameter, in an insulating membrane that separates two ionic reservoirs. An applied voltage across the nanopore results in an ionic current flow through the nanopore. The principle of single-molecule detection using the nanopore is based on detecting the blockage of this ionic current by the target.

One of the primary reasons for such a vigorous effort in the field of nanopore sensors is their promise of realizing fast, cheap, reliable and label-free sensors, especially for DNA sequencing. Existing methods of DNA sequencing require several thousands of dollars and many weeks to complete. In contrast, nanopores are significantly cheaper and can shorten sequencing time to a few days. Nevertheless, many challenges exist. One of the primary challenges identified is the integration of the nanopore platform and electronics[1]. An efficient integrated platform will reduce the parasitic capacitance, lower the noise and increase the bandwidth, resulting in enhanced sensitivity. Furthermore, coupling the nanoscale sensor with the sensing electronics enables closed-loop feedback, increasing the dynamic range of the sensor. Additionally, due to the batch-fabrication nature of CMOS processes, massively-parallel sensors with integrated electronics can be built. This crucial step is necessary if on-chip sequencing or biosensing is to become a reality. We have pioneered the fabrication of nanopores in a CMOS compatible platform that affords nanometer precision control of pore diameter and array density[3], see Fig. 1. The greatest challenge in fabricating nanopores in a CMOS compatible process is the low thermal budget (450°C), since deposition of high quality oxides, which is typically used in conventional nanopore fabrication, requires a high thermal budget[1]. To circumvent this problem, we used the pristine oxide that is found in a $0.5\mu m$ dual-poly CMOS process and necessitates the use of the same technology for the associated electronics.

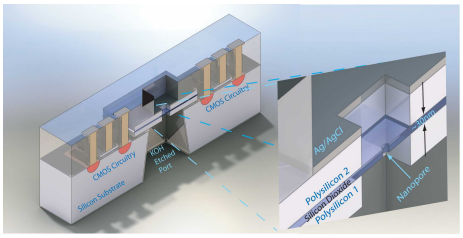

Fig. 1. Schematic illustrating the idea of CMOS integrated nanopore sensor. Shown is a nanopore within a CMOS chip with its associated electronics for control. Nanopore membranes are fabricated by post-CMOS micromachining utilizing the N^+ polysilicon/SiO_2/N^+ polysilicon capacitor structure available in the aforementioned process. Nanopores are then created in the CMOS process by drilling in a transmission electron microscope and shrinking by atomic layer deposition[3].

In this work, we describe for the first time the associated on-chip electronics that are needed for DNA translocation sensing in the $0.5\mu m$ dual-poly CMOS process. An essential requirement for on-chip electronics is wide dynamic range, see Section II-A. In the following sections we describe our solution to this problem that uses single-bit processing to enable adaptation. In Section II, we describe the architecture and the details of our wide dynamic range CMOS potentiostat. Following this in Section III we describe the results of a 5kbp DNA translocation through an off-chip Silicon Nitride 5nm pore. Section IV concludes the paper and discusses future work.

II. WIDE DYNAMIC RANGE CMOS POTENTIOSTAT

A. Measurement of Nanopore Current

The main component of any nanopore current measurement is the potentiostat. A potentiostat enables the application of a fixed potential across the membrane while simultaneously measuring the current going through the nanopore. The most common topology, the op-amp based

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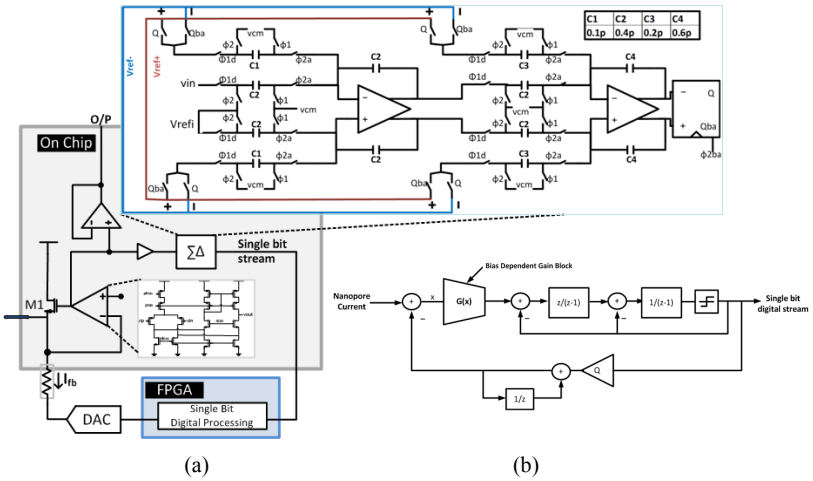

(a) (b)

Fig. 2. (a) Block diagram of the wide dynamic range CMOS potentiostat utilizing adaptive baseline cancellation. The input signal is logarithmically compressed and converted to a single-bit stream using a 2^{nd}order Σ-Δ. The single-bit stream is then subsequently processed by a one-bit digital filter implemented in an FPGA that extracts the baseline. The baseline is then fed-back to the front-end utilizing a DAC and a resistor. (b) Linearized block diagram of the wide dynamic-range CMOS potentiostat.

I-V converter or transimpedance amplifier (TIA), applies a voltage via the virtual ground (i.e via feedback) while forcing current to flow through the impedance in the feedback loop of the amplifier. For noise and bandwidth considerations, a capacitor is often used in the feedback loop of the amplifier. The resulting integration operation is subsequently removed using a differentiator. Alternatively, by utilizing integrated circuit techniques, low-noise and wide bandwidth topologies employing large on-chip resistors have also been demonstrated[4], [5].

Though conceptually simple, the implementation of such a topology is fraught with problems. First, there is a steady baseline current flow across the nanopore in the absence of any molecule translocating through it. Nanopore resistances in 1M salt (KCl) solutions range from $100M\Omega$ for small diameter pores (≈4nm) down to few $M\Omega$. These resistances translate to a baseline currents of 1nA to 10's of nA for a 100mV bias, which is typical for such measurements. The presence of this baseline current saturates integrator based TIAs and limits the dynamic range in resistive feedback topologies ($\leq$10-25nA). Circumventing this issue requires either a periodic reset or active analog baseline cancellation[4]. However, analog baseline cancellation loops enter nonlinear operation in the presence of sudden baseline jumps resulting in prohibitively long cancellation times (≈100 secs). Additionally, electrical sensing of larger molecules, such as proteins, requires using larger nanopores which further exacerbates the problem due to large baseline currents (50-100nA).

Rather than rely solely on linear techniques, our TIA topology employs nonlinear compression and 1-bit digital signal processing to enhance the dynamic range, see Fig. 2. Our topology is capable of canceling baseline currents up to 10 μA, while still resolving 10's of pA. The prototype chip is designed and fabricated in a standard AMI 0.5μm CMOS process with 5V supply. The front-end and the 2^{nd} order sigma-delta modulator occupy 0.029mm^2 and 0.15mm^2 respectively. A microphotograph of the chip is shown in Fig. 3.

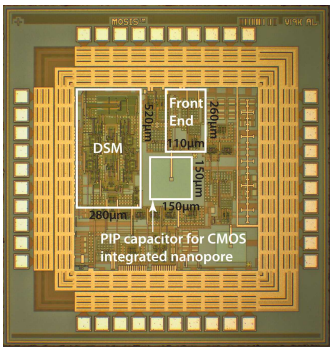

Fig. 3. Microphotograph of the chip implemented in ON-Semiconductor's 0.5μm process.

B. Adaptive Baseline Canceling Transimpedance Amplifier

The overall architecture, shown in Fig. 2a, consists of an input stage, a 2^{nd} order sigma-delta modulator (Σ-Δ-M) to convert the analog voltage into a single-bit stream, a FPGA to perform signal processing and a DAC-resistor pair to convert the processed signal into an analog feedback current. The input stage is a logarithmic I-V converter based on a NMOS ($M1$) source follower operating in subthreshold. The op-amp feedback converts the current through the transistor into a voltage, albeit nonlinearly. The exponential relationship of the subthreshold region results in a logarithmically compressed voltage, given by Equation 1, where A is the open loop gain of the feedback operational amplifier, n is the subthreshold swing factor, kT/q is the thermal voltage, I_{on} is the subthreshold current scaling constant (7.7×10^{-16}) and $\alpha = \exp -\frac{q(n-1)V_{sb}}{nkT}$ accounts for the non-zero source-body bias of $M1$. By employing a compressive first stage, this topology is able to maintain stable operation even in the presence of sudden baseline fluctuations.

$$V_{out} = \frac{A}{A+1}\frac{nkT}{q}\ln\frac{I_{in}}{\alpha I_{on}} \quad (1)$$

The feedback amplifier utilizes a folded-cascode topology with large PMOS input devices (15μm/10μm) to reduce flicker noise, yielding an overall noise floor of 8fA/$\sqrt{Hz}$, as shown in Fig. 4a. An SNR of 5 is desirable to ensure a low-rate of false events[5], resulting in a usable bandwidth of 750KHz for this implementation, see Fig.4b. As shown in Fig. 4c, canceling of the baseline reduces the 1/f noise, while simultaneously reducing the shot noise of $M1$ by reducing the bias current flowing through it.

Though logarithmic compression enables a large dynamic range (1pA-10μA), it reduces sensitivity which scales inversely with the baseline current. Sensitivity was regained by steady-state baseline current cancellation, implemented by a digital feedback loop based on 1-bit signal processing[6]. Unlike conventional DSP architectures, 1-bit signal processing requires no multipliers, since multiplication simply transforms to a scaling implemented easily by a shifter/multiplexer. More importantly, the simplicity of 1-bit signal processing allows for fast real-time feedback control. Transformation of the compressed analog signal to 1-bit encoding is performed by the Σ-Δ-M with an oversampling ratio (OSR) of 32. The 2^{nd} order Σ-Δ-M, oversampled by a 10MHz clock, provides a signal bandwidth of $\approx$150KHz and achieves a maximum dynamic range of 57dB. Non-overlapping clock phases, with delayed falling edges to minimize any input dependent charge injection, were generated using a latch-based clock generator[7]. Input reference voltage ($Vrefi$) and feedback reference voltage ($Vref-$ and $Vref+$) allow adaptive tuning to achieve optimal performance. Since only the gate voltage of $M1$ is fed into the Σ-Δ-M, a quiescent bias current can be forced to flow through $M1$ by using a different reference, $Vrefi$, as a quasi-source voltage (see Figure 2). The bias current and the choice of digital filter completely control the characteristics of the digital feedback loop.

One simple solution for the filter in the feedback loop is a digital differentiator. The drooping frequency response of the differentiator is compensated by placing a pole just inside the unit circle close to the zero at $z = 1$. Pole placement is done via a scaled feedback accumulator, where the scaling, Q, serves as the pole-tuning knob. The scaling is easily implemented as a digital shifter. Further understanding of the entire system was gained by developing a theoretical model shown in Fig. 2b. The small signal gain, G, of the log-compression stage is given by $(nkT/q)/I_{bias}$ and results in a bias dependent gain block. This nonlinearity gives rise to a bias dependent pole location of the feedback loop, as seen from the signal transfer function (STF) through the Σ-Δ-M in Equation 2. Thus, the bias current through M1 serves as an additional pole tuning knob.

$$STF = \frac{Gz^{-2}\left(1 - z^{-1}\right)}{1 - z^{-1} + GQz^{-2}} \qquad (2)$$

The output of the digital filter is then fed to an external 12-bit DAC and then converted to a current via a resistor. The resistor value is chosen based on the maximum allowable input-referred current noise and the required dynamic range.

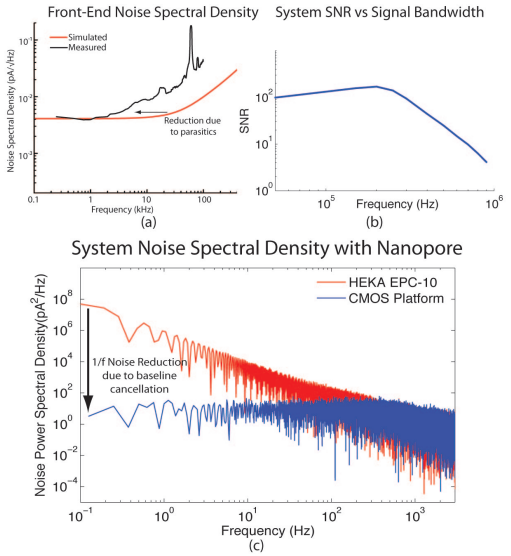

Fig. 4. (a) Measured and simulated noise spectral density of the amplifier.(b) SNR Vs Bandwidth indicating that a usable bandwidth of 750KHz is achieved at an SNR of 5 required for low false event detection rate.

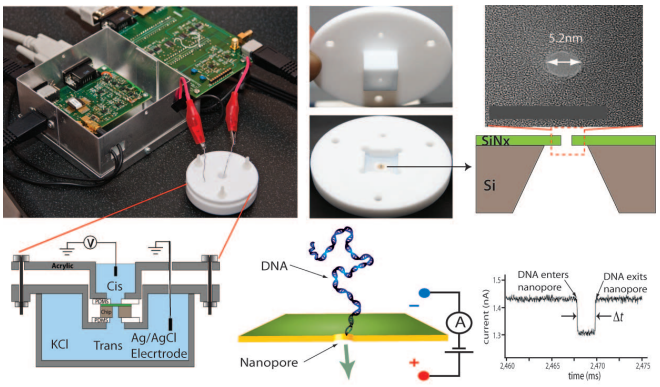

Fig. 5. Measurement setup of the DNA translocation experiments. Also shown are the illustration of DNA translocating through the nanopore and example of blockage current. See text for more details.

III. DNA Translocation Experiments

Quantitative sensing performance was evaluated by comparing the results from the CMOS platform with a commercial potentiostat (EPC 10, HEKA instruments). A solid-state nanopore with a diameter of 5.25 nm was directly drilled in a commercially available 30nm thick silicon nitride membrane using a tightly focused electron beam in a TEM. The chip containing the pore was subsequently mounted between two Teflon fluidic chambers, see Fig. 5. The reservoirs were filled with salt solution, 1 M KCl 10 mM TRIS-HCl buffer at pH 8. The desired transmembrane potential was applied and the resulting ionic current was measured by placing Ag/AgCl electrodes in each reservoir. To perform the translocation studies, 5kbp double-stranded DNA (dsDNA) molecules were added to the cis reservoir at a concentration of 3nM. Results of typical translocation events obtained by the CMOS platform and EPC-10 are shown in Fig. 6. Clearly the CMOS platform is able to resolve faster

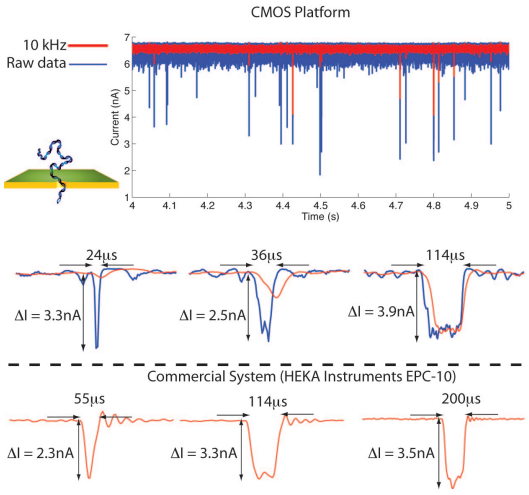

Fig. 6. Typical translocation events recorded by the wide dynamic range CMOS potentiostat. Also shown are a few representative events with and without 10KHz filtering. The results of typical events obtained from a commercial (EPC-10, HEKA Instruments) potentiostat are also shown.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON

	Integrated Circuit Topology		Commercial Instruments	
	This Work	NMETH'12[5]	HEKA	AXOPATCH
Technology	0.5μm	0.13μm		
Max.I_{in}	10μA	7.5nA	100nA	100nA
$I_{noise<RMS>}$	2.5pA	3.2pA	18pA	7pA
Baseline Cancellation	Yes (Digital)	No	No	No
Max. BW @ SNR=5	750KHz	1MHz	10KHz	70KHz

events due to the larger bandwidth. It is common to evaluate typical blockade (ΔI/I) ratios by plotting the event histogram of blockage ratios[5]. Theoretically, the blockade ratio should be independent of the bias voltage and the rate (#events/sec) should increase as the bias increases, due to the increased DNA capture radius. Both these trends are clearly visible in the CMOS platform as shown in Fig. 7, while the EPC-10 shows a biased distribution. To evaluate if this was purely due to the increased bandwidth, the CMOS platform data was filtered by the same filter used for the EPC-10 and the trend still remained. This clearly indicates that the removal of the bias in the distribution is not due to the increased bandwidth but rather due to the superior sensing enabled by baseline cancellation. The performance of the proposed design compared against recently published work is shown in Table I.

IV. CONCLUSIONS

We have presented here for the first time a digitally assisted wide dynamic-range potentiostat for measuring currents in solid-state nanopores. We have shown that by using a combination of nonlinear compression and single-bit digital signal processing the dynamic range is enhanced. Furthermore, we have validated the circuit by performing DNA translocation experiments through a 5nm solid-state silicon nitride nanopore. By utilizing a CMOS process that is compatible for integrating a nanopore, we believe that complete integration with the electronics is possible. Work is

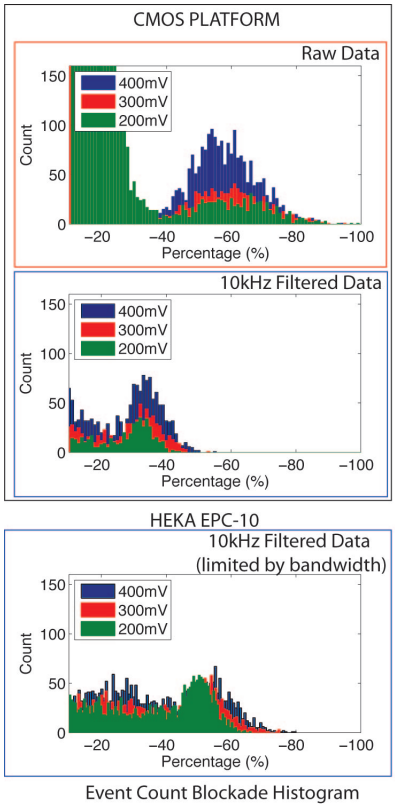

Fig. 7. Event-Count Histogram of Blockade ratio (ΔI/I) at various bias voltages for the CMOS system with and without 10kHz filtering along with the data from the commercial HEKA EPC-10 potentiostat. The CMOS system shows the expected behavior of increased number of events for higher bias voltages, while the commercial system fails to do so.

on-going in our lab to realize this vision, which we believe will realize the promise of fast, cheap nanopore based single-molecule biosensors.

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