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Improved Polyimide Thin-Film Electrodes for Neural Implants

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Abstract — **Thin-film electrode arrays for neural implants are necessary when large integration densities of stimulating or recording channels are required. However, delamination of the metallic layers from the polymer substrate leads to early failure of the device. Based on new adhesion studies of polyimide to SiC and diamond-like carbon (DLC) the authors successfully fabricated a 232-channel electrode array for retinal stimulation with improved adhesion. Layers of SiC and DLC were integrated into the fabrication procedure of polyimide-platinum (Pt) arrays to create fully coated metal wires, which adhere to the polyimide substrate even after 1 year of accelerated aging in saline solution. Studies on the inter-diffusion of Pt and SiC were conducted to establish an optimal thickness for a gold core of the platinum tracks, which is used for reducing the electrical track resistance. Furthermore, the electrochemical behaviour of the stimulating contacts coated with IrOx were studied in a long-term pulse tests over millions of pulses showing no deterioration of the coating.**

I. Introduction

Neural interfaces are a key aspect for the restoration of lost body functions, as they provide the link between complex electronics and the neural tissue. In cases where the complexity of the function to be restored is high, as in the case of blindness, many individual contacts, densely packed are required to interface the targeted cells on the retina. Thin-film based devices produced by applying photolithographic methods have been introduced to achieve high integration densities. Polyimide (PI) as substrate material provides sufficient mechanical protection for the integrated tracks as long as adhesion between the substrate and the embedded thin-film metallization is maintained [1]. A thin-film metal membrane, mostly platinum with thicknesses in the range of only a few hundred nanometers relies on its adhesion to the flexible (but not stretchable) polymer substrate, otherwise any fractional force can damage integrated tracks and electrode contacts.

Recent studies [2],[3], concluded that adhesion to PI is achieved through carbon bindings and not through oxide formation and that the chemical adhesion of polyimide to amorphous diamond-like carbon (DLC) layers and SiC deteriorates only at a minimal rate.

Predominantly, delamination is caused by residual stress, which is not only inevitable but also the major driving force for cracking in thin films. Residual stress (σ_R) is the sum of two components, the intrinsic (σ_i) and the thermally induced component (σ_{Th}). The second is accessible as it arises through deposition of the thin-films at higher temperature than its final application. Each material in a multi-layer stack with varying coefficient of thermal expansions (CTE, α_{Th}) will contract differently when cooling down from process to room temperature. If any adhesion is present they will be hindered in contraction experiencing thermal stress σ_{Th}. The amount of stress (σ_{Th}) is defined by material properties (thickness t, biaxial modulus E and CTE) and the maximum temperature difference they are exposed to during fabrication. The more complex intrinsic stress component is caused by the atom-by-atom film growth leading to a mix of regions with mismatching lattice orientations and lattice constants. This component is also increased by impurities, cavities and lattice orientation in the underlying layer. The higher the melting point of the deposited material and the lower the deposition temperatures during physical plasma deposition, the higher the levels of intrinsic stress in the material will be [4], [5]. Platinum, having a melting temperature (T_M) of ~1770 °C being deposited at around 100 °C to allow photolithographic structuring through photoresists (which withstand only a max. temperature of ~115 °C) on a PI substrate, fulfils all 'prerequisites' for a deposition under high residual stress levels. Furthermore, according to the Pt/C phase diagram, there is no material combination leading to a Pt-C bond at temperatures below 1000 °C. Considering this and the results from [2] added to residual stress in the films it is not surprizing to face delamination in PI/Pt thin-film devices.

To provide stability in a thin-film neural interface two things have to be considered: a) The residual stress in the film has to be minimal and b) the adhesion to the underlying layer has to be maximal, as this defines up to which extent an interface will withstand a separation force. Based on these considerations and inspired by the work of Cogan et al. [6] the authors introduced SiC and DLC into the fabrication procedure of neural electrode arrays to provide higher interfacial chemical adhesion between metal and PI, avoiding delamination and maintaining the electrical and mechanical properties of the fabricated electrode arrays.

II. Materials and Methods

A. Testing of delamination driven by residual stress

Residual stress is easily ignored when fabricating thin-film electrode arrays, as the most commonly used layer stack

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(PI/metal/PI) leads to interfacial stresses, which appear to cancel each other out due to the symmetry of the stack, so no bending is observable. Yet, the residual stress still acts on the interfaces. If the adhesion energy (G_{Ad}) between the layers is larger than the elastic deformation energy ($G\varepsilon$) caused by stress σ_R the system will remain stable. The elastic deformation energy is a function of the σ_R and the biaxial modulus E of the film as presented in eq. 1 [5],[8].

$$G\varepsilon = \tfrac{1}{2} \cdot \sigma_R^2 \cdot E \qquad \textit{(Eq. 1)}$$

$$G_{Ad} - G\varepsilon \geq 0 \qquad \textit{adhesion}$$

$$G_{Ad} - G\varepsilon \leq 0 \qquad \textit{delamination}$$

The proposed low-stress / improved adhesion electrode arrays are estimated to function over many years of application. Based on residual stress analysis, a method for prediction of lifetime is proposed and presented in figure 2. As the chemical adhesion deteriorates over time [2] ($\partial G_{Ad}/\partial t$ in Fig. 1 a) it will reach a critical level where $G_{Ad} \leq G\varepsilon$ and delamination is likely to occur.. If the stress in the layer is known (as in the case of thermally induced residual stress) and a time-to-delamination (T_d) can be determined as a function of the stress, it might be possible to predict the lifetime of a device based only on material parameters (t, E, α_{Th}) and the maximum temperature during fabrication. The absolute value of intrinsic stress is very complicated to calculate. However, annealing a material relieves its intrinsic stress and it is best done at 0.3 to 0.5 times T_M of the material. The 450°C step when curing PI, eliminates intrinsic stress to the extent that only the thermal component dominates on the specimens (*own investigations, unpublished*). The following test was conduced to quantify the proposed failure prediction model.

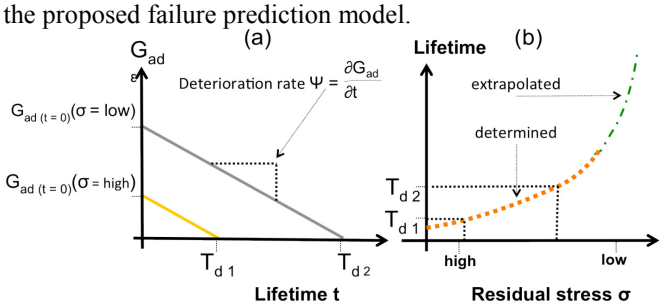

Figure 1: Lifetime prediction model based on measured times to failure dependening on σ_{Th}. (a) the deterioration of adhesion will lead to failure at T_d. By measuring the time to failure for a known high σ_{Th}, the lifetime of a low-stress device can be estimated (b).

Stripes of polyimide (U-Varnish S, UBE America Inc., New York, USA) of rectangular dimensions (20 mm x 7.5 mm x 10 µm) were coated (one-sided) with different thicknesses of SiC (50 – 400 nm) deposited by plasma enhanced chemical vapour deposition (PECVD, PC310 reactor by SPS Process Technology Systems Inc, San Jose, CA USA). 300 nm Pt were sputter-deposited (Univex500, Oerlikon Leybold Vacuum GmbH, Cologne, Germany) on top of the SiC. One sample of each thickness was tempered at 450 °C under nitrogen atmosphere following the temperature curing profile for polyimide suggested by the UBE. The samples were then stored for accelerated aging at 60 °C in 0.9 NaCl solution and remained under constant visual inspection in order to discover the potential onset of delamination over 1 year (*by the time of submission of this paper*).

B. Electrode manufacturing

The first step for integration of SiC into the electrode fabrication process consisted in finding the process parameters (process pressure, gases ratio, plasma frequency and reactor power) at 100 °C which provided a stochiometrical (1:1) SiC layer with the lowest intrinsic stress possible. The measurements were conduced with SiC coated Si Wafers (525 µm thick). These were measured before and after deposition with a wafer geometry gauge (MX203, E+H Metrology GmbH, Karlsruhe, Germany) to extract thickness and stress values of the deposited layers. Chemical characterization was done by x-ray photoemission spectroscopy (XPS).

The actual fabrication procedure starts by spin coating 5 µm PI on a silicon wafer and curing at 450 °C in N_2 atmosphere. Image-reversal resist (AZ5214, Microchemicals GmbH, Ulm, Germany) was photolithographically exposed and developed to create the structures for the metal tracks and pads of the bottom layer. Oxygen plasma was subsequently applied to remove potential residuals of the resists and to activate the binding sites for the next layer. 50 nm of SiC were deposited through PECVD. Immediately after deposition, Pt/Au/Pt (100 nm each) were evaporated onto the wafer (Fig. 2 a). The top of the metal stack was coated with 30 nm SiC and 10 nm DLC to provide a transition into a fully carbon layer for optimal adhesion to the following PI cover layer (Fig. 2 b). Even though sputter deposition with higher deposition energies would lead to a better adhesion between the Pt and the SiC, the decision was taken for evaporation to achieve a more directed, anisotropic deposition. Subsequently, a lift-off step was performed in acetone and isopropanol leaving the fully coated metallic structures behind. The process was repeated with a 2.5 µm PI starting layer to produce the second metallization layer. Using a ~25 µm thick resist (AZ 9260) the masking layer for etching the stimulating contacts was defined. Reactive ion etching (RIE) using oxygen as process gas removed polyimide and SiC/DLC and exposed the electrode contacts. 100 nm Ir and 400 nm IrOx were deposited through sputtering (sputtered iridium oxide film, SIROF) using the same masking layer (Fig. 2 c). The resist was stripped and a new layer of resist was deposited, now covering the IrOx electrode contacts. The contours of the electrode and the contact pads were structured and etched open through RIE (Fig. 2 d). The resist was then stripped and the surfaces were cleaned with oxygen plasma. 100 nm Au were globally deposited by sputtering onto the wafers, providing a seed layer for Au electroplating of contacts for flip-chip bonding. Again, AZ9260 resist was deposited and structured, exposing the contacts for Au to be electroplated as well as a contact rim at the edge of the wafer. The openings were dimensioned 5 µm smaller than the actual openings to ensure that the electroplating starts at the bottom of the contact and not at an opening's edge. 12 µm gold were electroplated in a cyanide gold solution allowing the pads in the lower metal layer to form columns, rising above the top PI layer (Fig 2 e). After resist removal the wafers were exposed for 2 minutes to iodide/potassium-iodide (K/KI) gold etching solution removing the thin Au seed layer. The

wafers were cleaned in acetone, isopropanol and deionized water and the samples were mechanically detached from the wafer (Fig. 2 f).

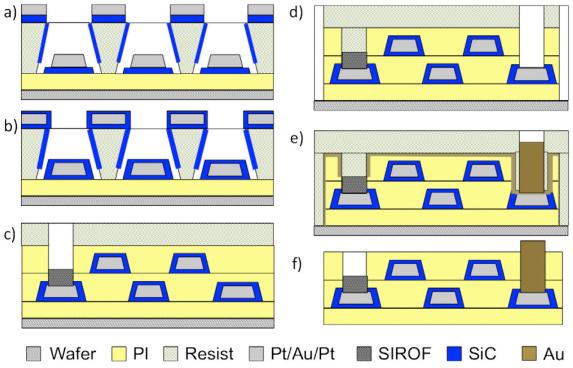

Figure 2: Simplified sketch for the electrode array's fabrication procedure.

C. *Geometrical aspects of the electrode array*

Tracks with 10 µm width, 12 µm spacing and 300 nm height were chosen for most of the thin-film wiring. To keep the area of the actual electrode array below 5 mm in diameter, the track's width as well as the spacing in between was reduced here to 8 µm each, avoiding a fan-out at the head of the electrode due to track routing. The contacts are 100 µm in diameter, having a hexagonal pitch of 0.27 mm. Some aspects regarding the electrode's design are presented on Fig. 3. The double-layered process was required to pack 232-channels into a 4 – 5 mm wide micromachined ribbon cable. To minimize capacitive coupling between the tracks of the top and the bottom layers the parallel wiring of both layers runs dephased (Fig. 2 – c). The spacing of 12 µm between tracks allowed 1 µm misalignment during photo-lithography. It was not possible to avoid crossing of the wires at some point, but the overlapping was on purpose kept minimal. To allow relative motion of top and bottom layers during electrode attachment, the contact pads were spatially separated at the back-end of the electrode.

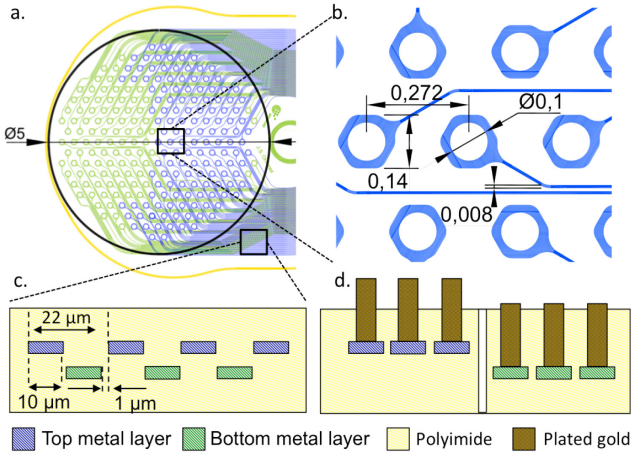

Figure 3: a) and b) CAD extracts of the electrode design with relevant electrode's dimension in mm, c) cross-section showing the tracks' position on different layers, d) re-location of top and bottom layer wires and contacts at the interconnection side of the electrode array. This allows relative motion of contacts lying on the bottom and top layer without damaging the thin tracks during thermosonic bonding.

D. *Interdiffusion of Pt and SiC*

As the curing of PI takes place at 450 °C, an interdiffusion of Pt and SiC was expected, affecting the electrical properties of the metallic tracks. The lower metallization layer experiences the PI curing step twice, while the top layer only once. For quantification of a potential effect, on electrical conductivity, metallic test structures of 100 µm width 40 mm length were integrated into the design and positioned at the north, south, east and west positions of the wafer relative to the primary flat (south). The top and bottom layer structures were designed with full overlapping to provide also information on the capacitive coupling of top and bottom metal structures. A 4-point measurement using an LCR meter was conduced on three wafers, one containing a one-sided SiC coating while the other two were fully coated in SiC/DLC as presented above. The probes were measured directly after production and after repeated temperature treatment at 450 °C for 15 min in N_2 atmosphere.

E. *Electrochemical characterization*

32 out 232 electrode contacts were randomly selected for investigation of electrochemical properties. Impedance spectroscopy using a 3-electrode setup with a Ag/AgCl reference electrode, was carried out in phosphate-buffered saline (PBS, pH = 7.4) solution at room temperature, applying sinusoidal excitation of 10 mV_{pp}. Furthermore, the electrodes were subjected to long-term pulse testing (or voltage transient measurements), using a custom-made set-up of 10 current sources that permit the real-time subtraction of the iR drop (voltage across the electrolyte and metal conductors) from the generated voltage transients, providing the voltage across the phase boundary (V_{PB})[9]. Pulse testing was done within a two-electrode configuration comprising a large-area stainless steel counter electrode. The excitation stimulus was a biphasic (cathodic phase first), symmetrically rectangular and charge balanced current pulse (200 Hz frequency) with a fixed amplitude of 275 µA, 200 µs pulse width and an interpulse phase of 10 µs. Hence, a static charge of 55 nC (~700 µC/cm^2) was applied.

III. Results

A. *Stress driven delamination*

Although absolute intrinsic stress in the incubated probes could not be measured, the reduction of it could be observed, due to the sample's change in curvature from compressive stress to tensile stress, dominated by the Pt with the largest CTE (9 ppm/K). After 9 and 13 days of incubation the probes with 400 nm and 300 nm SiC, respectively, which were not tempered, showed complete delamination of the Pt from the SiC. The SiC remained attached to the PI. All other probes remained stable until the day of submission (390 days). With the two recorded times-to-failure it is not yet possible to predict the time of delamination for the samples with less residual stress, since no trend can be recognized so far. The more complex mathematical stress calculations for the multilayer arrays will be presented elsewhere.

B. *Electrode fabrication*

The least achievable residual intrinsic stress for 50 nm SiC on silicon wafers was that of ~ - 750 MPa with a low frequency (187 kHz) plasma at 100 °C. However, the level of stress is dependent on the thickness and stiffness of the underlying layer and this value is not the same if the SiC is grown on thin PI or Pt. The success of the lift-off process was not compromised by PECVD deposition of SiC and DLC. When mechanically detaching the electrode from the wafer some electrodeplated pads were lost. No increased stiffness of the arrays was noticed during handling of the probes, compared to probes without SiC and DLC layers.

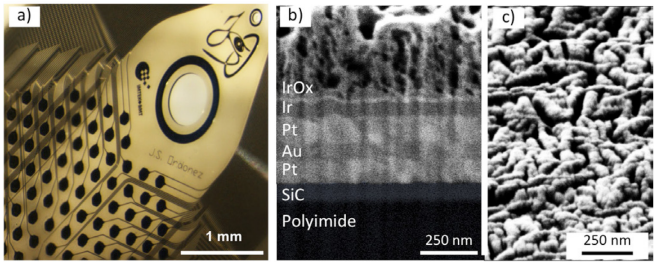

Figure 4: a) Optical view on electrode array detail, b) focused ion beam cross-section image of a stimulating pad showing the layer stack. The thin (~10 nm) transition layer between the Ir and the IrOx coating is unexpected and still under investigation. c) scanning electromicrograph of IrOx surface.

C. *Interdifussion of Pt and SiC*

The measured decrease in conductivity was stronger for tracks fully coated with SiC than for those half coated. The behaviour is presented on Fig. 5. The values at time zero, which indicate the properties directly after fabrication of the probes show on wafers W2 and W3 (average of all 4 test probes on a wafer) a higher resistivity for the lower layer than for the top. Contradictive is W1, which even with the full coating of the top layer it still features a lower resistivity which however increased fast and overtook the bottom half coated layer after 30 min temperature treatment.

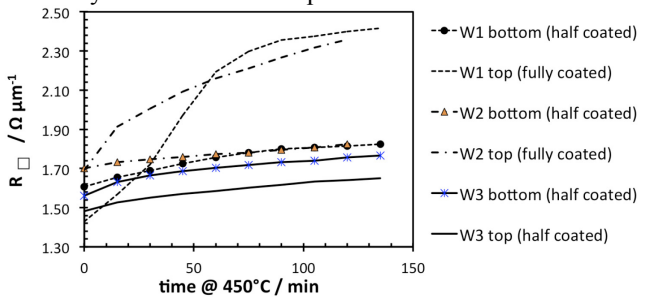

Figure 5: Change in R_{square} with annealing time. The value at time 0 corresponds to the probes directly after fabrication, when the bottom layer has experienced 450 °C twice, while the top layer only once.

D. *Electrode characterization*

SIROF electrode contacts subjected to ~1.5 billion pulses (by the time of submission), whilst V_{PB} was monitored showed no changes of the phase boundary voltage, suggesting great coating's stability. The impedance spectroscopy revealed an access resistance of 5 kOhm, a cut-off frequency of 60 Hz (average over 32 characterized electrodes) and no observable variations across individual contacts. Capacitive coupling between adjacent electrode tracks could be detected neither across layers nor on the same layer. The overlapping testing probes for interdiffusion showed capacitances of 30 pF. The overlapping area is 10 times larger than the area that two wires on top and bottom would have, if they ran parallel along the complete electrode array.

IV. Discussion and Conclusion

The fact that none of the tempered samples delaminated even after ~5 yeas of lifetime (extrapolated for 37 °C), shows a tremendous increase in adhesion to (our) state of the art. The annealing step, which is present through the curing of the PI not only reduces the stress but increases the adhesion strength between the SiC and the Pt, correlating with the interdiffusion measurements. Low pressure PECVD leads to a layer growth through surface reaction, permitting covalent bond formation and thus leading to a strong binding *bottom* interface. For the top interface, the results from [2] were considered: spin-coated PI adheres best to DLC. An increase in resistance is not critical; based on the measured data it is now possible to adapt the thickness of the core Au layer to reach the desired conductivity in the film. Curing PI at lower temperatures could be the cause of early delamination in other PI-based arrays. Different to [6] & [7], the coatings are only ~50 nm thick, focused on adhesion and not on insulation properties or mechanical reinforcement. The flexibility of the array is fully maintained. Alternative fabrication procedures where the resist is coated on the SiC were discarded as the contamination of the chemical surface from the photoresist reduced the amount of Si on the SiC surface from 50% to <20%. Oxygen cleaning of the surfaces leads to SiO_2 formation on the surface of the SiC ruining the adhering properties to Pt. Albeit the isotropic deposition during PECVD, image-reversal structuring was possible. Combining the PECVD with the lift-off step does not only simplify the fabrication process, but it also reduces enormously the production costs.

The process presented in this paper along with the presented long-term studies allows us to apply this technology for long-term implantation of electrode arrays with a much higher confidence in their reliability.

V. Acknowledgements

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