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Design and Measurements of Low Power Multichannel Chip for Recording and Stimulation of Neural Activity

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***Abstract*— A 64-channel Neuro-Stimulation-Recording chip named NRS64 for neural activity measurements has been designed and tested. The NRS64 occupies 5x5 mm^2 of silicon area and consumes only 25 µW/channel. A low cut-off frequency can be tuned in the 60 mHz - 100 Hz range while a high cut-off frequency can be set to 4.7 kHz or 12 kHz. A voltage gain can be set to 139 V/V or 1100 V/V. A measured input referenced noise is 3.7 µV rms in 100 Hz – 12 kHz band and 7.6 µV rms in 3 Hz – 12 kHz band. A digital correction is used in each channel to tune the low cut-off frequency and offset voltage. Each channel is equipped additionally with a stimulation circuit with an artifact cancellation circuit. The stimulation circuit can be set with 8-bit resolution in six different ranges from 500 nA - 512 µA range.**

I. Introduction

Many neurobiological experiments need multichannel readout systems for simultaneous recording and stimulation of neural activity. For this task a high density multi-electrode array and a multichannel readout/stimulation electronic system are required. To increase the number of recording channels and to minimize the volume and weight of the electronic recording system, one can use a VLSI technology to develop an application specific integrated circuit (ASIC), which is suitable for these purposes [1-8]. The design of such a multichannel ASICs requires careful consideration of many problems common to analog design: noise level, power consumption, mismatch problems, filter topology and its tuning range, recording without interference of stimulation artifacts, etc.

We propose a multichannel ASIC named Neural-Recording-Stimulation 64-channel chip (NRS64) which can be used both for recording and stimulation of neural activity. The NRS64 chip is designed in CMOS 180 nm technology and it can be used both for in-vivo and in-vitro experiments. Thanks to a modern technology and an implementation of active digital control and correction circuits we obtained a very good functionality in a single 64-channel chip including: recording both LFP and spike signals with frequency band controlled in a wide range, a low noise performance, an ultra-low power consumption per channel and a very good uniformity of analog parameters in multichannel integrated circuit. The NRS64 integrated circuit has additionally a stimulation block in each channel with a selection of different patterns and with an effective artifact cancellation. Below we present NRS64 chip architecture, measurement results and an example of in-vivo neural recording.

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II. NRS64 Architecture

A. Overall chip architecture

The NRS64 integrated circuit consists of 64 recording and stimulating channels (see Fig. 1). Each channel has a digital register which controls the low and high cut-off frequencies, the channel gain, stimulation parameters, the artifact cancellation block and DC offset voltage of the readout channel. For data output compression an analog multiplexer 64:1 is used with 5 MHz nominal operational frequency.

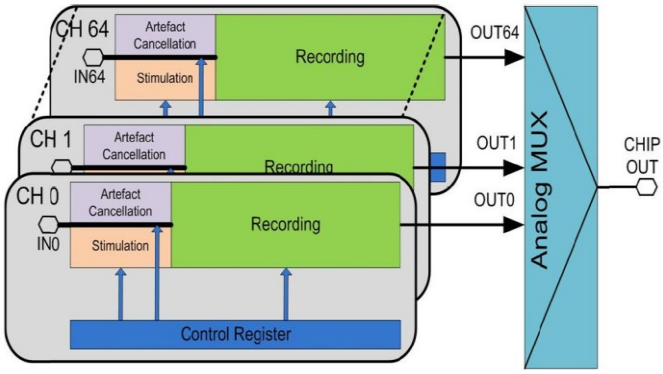


Figure 1. Block diagram of the NRS64 chip.

B. Readout channel with trim DAC

The simplified scheme of a single readout channel is presented in Fig. 2. It consists of two amplifiers (AMP1 and AMP2) based on the differential folded cascode architecture. The AMP1 stage uses the capacitive feedback to set the gain to C_0/C_1 and amplifies input signals with respect to the common input REF connected to a reference electrode.

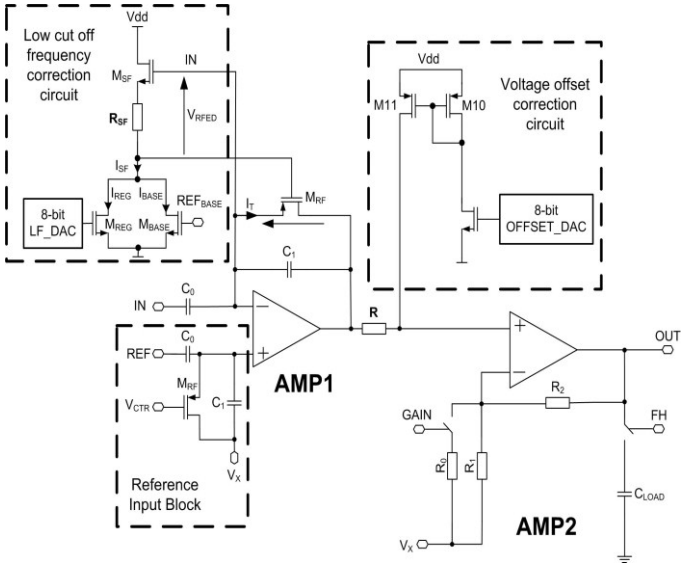


Figure 2. Simplified scheme of the readout channel.

An electrochemical offset at neuron-electrode interface can saturate the AMP1 stage. An AC coupling at the input blocks the DC offsets, however large capacitors are required. In our case the coupling capacitor C_0 is based on the NMOS transistor (W/L = 500µm/50µm) biased in the strong inversion region what results in 205 pF effective capacitance. The M_{Rf} PMOS transistor (W/L = 0.4µm/50µm) biases the input of the differential amplifier and together with C_1 = 19 pF MIM (metal-insulator-metal) capacitor sets the low cut-off frequency in the recording channel. Because the effective channel resistance of M_{Rf} is very high (tens of GΩ), its spread from channel to channel is critical. To solve this problem we put into each channel 8-bit correction LF_DAC which controls the effective gate-source voltage in M_{Rf} transistor and allows to tune the low cut-off frequency in each channel individually.

In order to avoid nonlinearities which can be generated by the M_{Rf} channel resistance when the input stage has a high voltage gain, we set the gain of the AMP1 to 11 V/V which is followed by the AMP2 with either 12 V/V or 100 V/V voltage gain. The AMP1 and the AMP2 amplifiers are DC coupled and the effect of the AMP1 DC output offset propagation is minimized thanks to 8-bit correction OFFSET_DAC placed in each channel [9]. Thanks to a digital register controlling the GAIN and FH inputs (see Fig. 2) the gain and the high corner frequency of the AMP2 stage can be set individually in each channel.

C. Stimulation block and artifact cancellation

Each channel can generate current pulses with a preset value, polarity and duration. The current value can be controlled together for all channels using four 8-bit DACs or separately for each channel with six current buffers placed at the output of the channel (Fig. 3). The buffers have six different ranges (500 nA to up to 512 µA). The DACs are divided into two pairs. Each pair consists of two complementary DACs for negative and positive currents. The inputs of the current buffers can be connected to one of the four DACs. The pulse duration can be controlled globally by the stimulation enable signal (*ENchan*). The pulse generation can be also disabled individually for each channel.

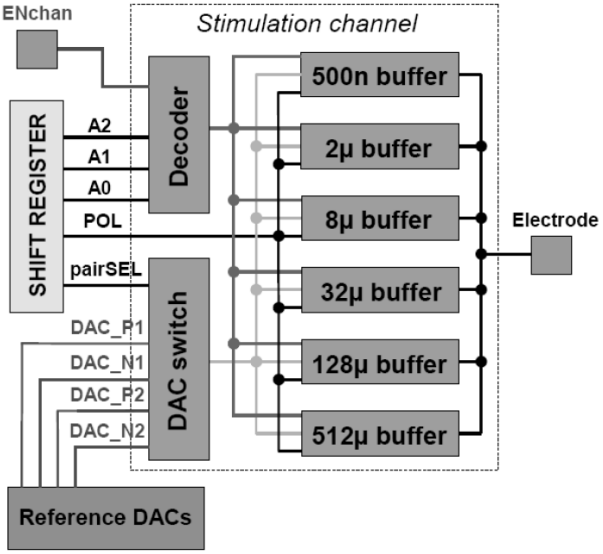


Figure 3. Block diagram of stimulation circuit.

The input of each readout channel is equipped with an artifact cancellation block. Its task is to remove an excess charge which can left on the electrode capacitance after a stimulation pulse. The charge is seen as a DC voltage by the first amplifying stage and may cause its saturation for a time period up to tens of milliseconds. This too long saturation time comes from long time constant of the AMP1 stage which is on the other hand necessary for LFP (Local Field Potentials) recording. A timing diagram and a working principle of the artifact cancellation circuit is presented in Fig. 4. It consists of a discharge amplifier placed in the feedback of the AMP1 stage and it runs as follows. During the stimulation phase the main amplifier and the discharging amplifier are simultaneously disconnected from the electrode and the stimulating current is applied to the electrode. In the next step both the main amplifier and the discharging amplifier are connected to the electrode in order to discharge electrode capacitance. During this phase the DC voltage at the input of recording channel is forced to be equal to the DC voltage in this point before stimulation. Optionally the time constant (the low cut-off frequency of AMP1 stage) may be temporarily changed to decrease the artifact cancellation time. Finally, the discharging amplifier is disconnected from the electrode allowing for normal neural signal recording.

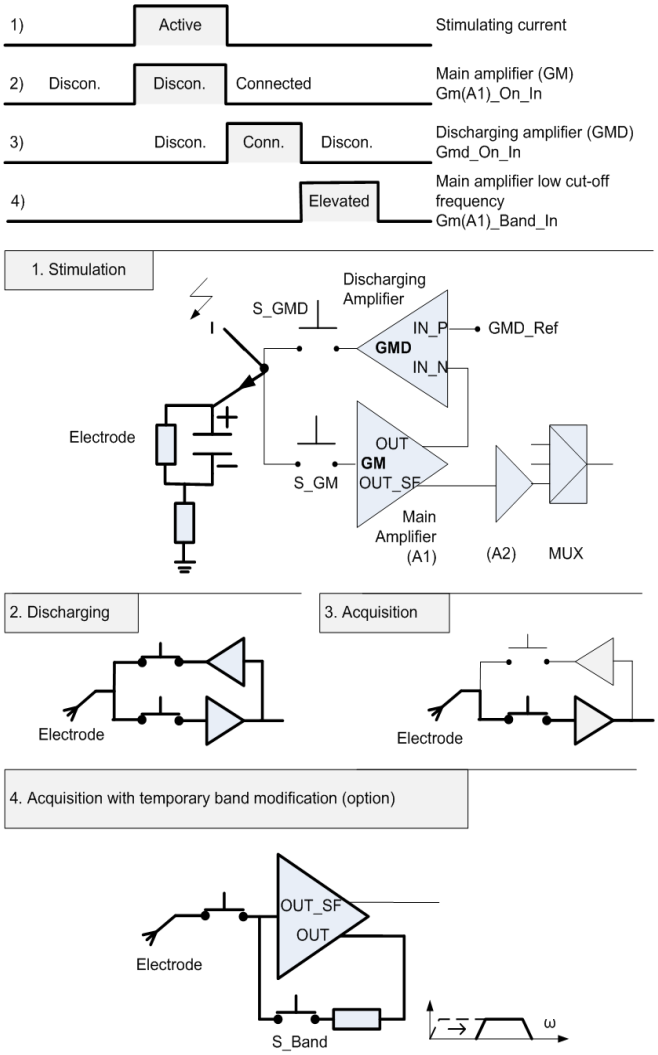


Figure 4. Block and time diagram of the stimulation and artifact cancellation circuits

III. Measurement Results

The NRS64 chip was wire-bonded to the designed Printed Circuit Board (PCB) (see Fig. 5) and the following tests were performed:

- total power consumption measurements,
- verification of functionality of digital parts,
- measurements of main analog parameters (gain, cut-off frequencies, noise) and their spread from channel to channel,
- common mode rejection ratio measurements,
- stimulation functionality tests.

We have checked the functionality of all digital blocks (multiplexer, shift registers, etc.) and they work according to our specification. The measured power consumption per single recording channel is only 25 µW. Tests show that the user is capable to change the low cut-off frequency independently in each channel in the 60 mHz – 100 Hz range. The measurements demonstrate that the high cut-off frequency can be either 4.7 kHz or 12 kHz while the voltage gain can be set to either 139 V/V or 1100 V/V.

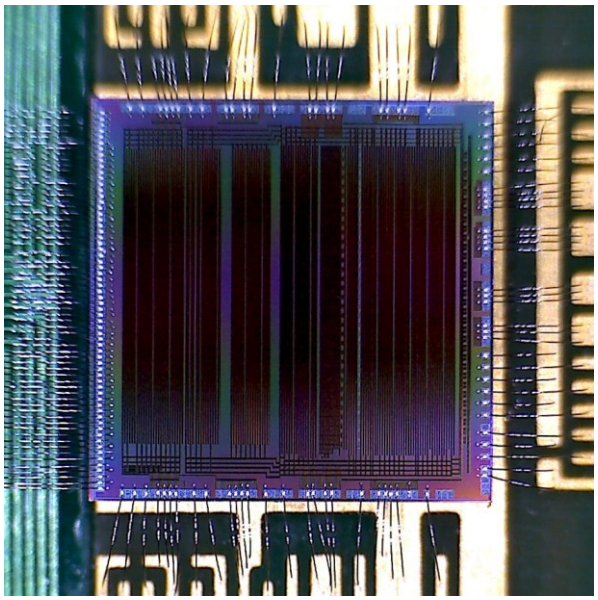


Figure 5. Photo of the NRS64 chip - die area 5 x 5 mm^2.

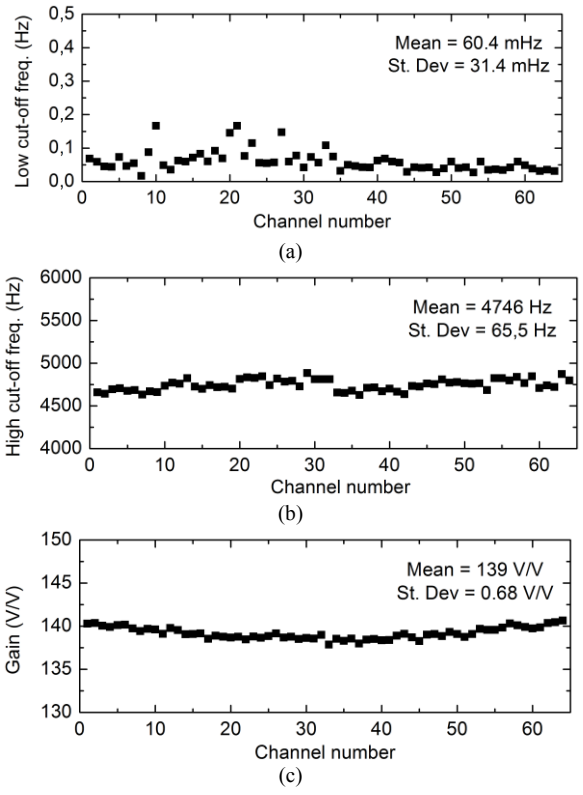
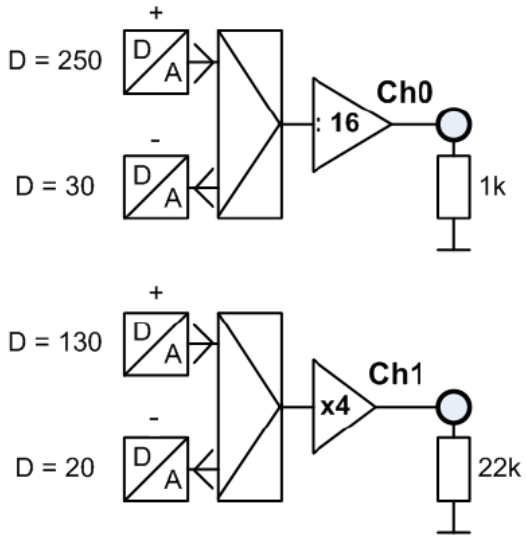


Figure 6. Spread of main analog parameters in 64 channels of NRS64: a) low cut-off frequency, b) high cut-off frequency, c) gain.

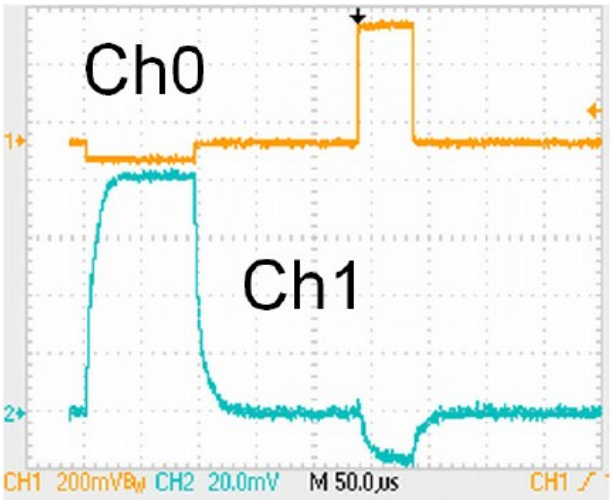
Since the presented ASIC has a multichannel architecture the spread of its main parameters from channel to channel is very important. Typical distributions of the cut-off frequencies and the voltage gain are shown in Fig. 6. In our system the low cut-off frequency can be set even at 60 mHz, while its spread from channel to channel is only 31 mHz (on one sigma level). For setting the low cut-off frequency at 1

Hz the spread is 50 mHz (one sigma). The spread of the voltage gain defined as the ratio of standard deviation to mean value (St.Dev/Mean) is equal to 0.5 %.

We also performed noise measurements of the NRS64 chip and they show that an input referred noise is 3.7 μV_{RMS} (for 100 Hz - 12 kHz range) and 7.6 μV_{RMS} (for 3 Hz – 12 kHz range). The lowest frequency band which we were able to measure was limited by our equipment for noise measurements.



(a)



(b)

Figure 7. Current stimulation test: a) two different loading resistances (1kΩ and 22kΩ) were connected to two channels (Ch0 and Ch1) and stimulated with two consecutive current pulses with different amplitudes and opposite polarization, b) the time durations of pulses were 100 µs and 50 µs and assumed amplitudes were -60µA and 500µA (channel 0) and 4 µA and 0.6 µA (channel 1).

In the first NRS64 prototype a measured CMRR was only 25 dB. The reason of such a low value of the CMRR was the Input Reference Block (see Fig. 2), which was common for all 64 channels to save silicon area. We have corrected this point in the second prototype chip making the Input Reference Block separate for each channel. This improves the measured CMRR equal to 48 dB.

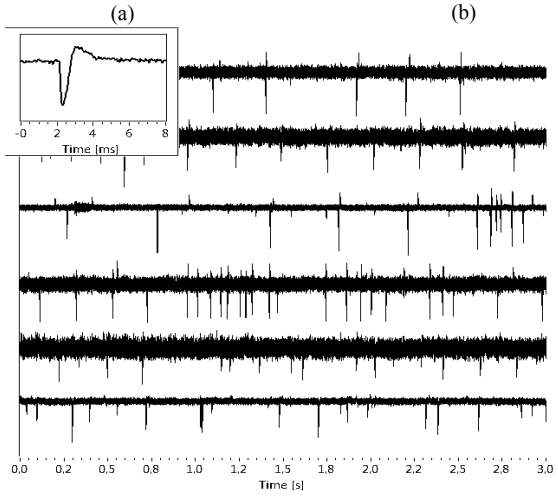
We have also checked the functionality of the stimulation blocks. All stimulation current DACs work correctly up to max. current range equal to 512 µA. The exemplary waveforms are shown in Fig. 7. The tests with artifact cancellation with different electrode types and stimulation patterns are still ongoing.

IV. Multichannel Systems for Neurobiology Experiments

The characteristic feature the NRS64 chips is the ease of building their own measurement systems to suit various in-vivo and in-vitro experiments. Fig. 8a presents a system with NRS64 chip dedicated for in-vivo experiments. The system is equipped with 10 mm long 64-site electrodes from Neuronexus Technologies (Fig. 8b). The experiment was performed on a rat under urethane anaesthesia. The electrodes were implanted into the brain to record infraslow oscillations at the level of neuronal spiking in the intergeniculate leaflet of the rat lateral geniculate nucleus. Signals from 64 channels were recorded for a few hours and the results from selected channels with the neuronal spiking are shown in the Fig. 8c.

(a)

(b)



(c)

Figure 8. a) 64-channel system for in vivo recording, b) dedicated 10 mm long electrodes provided by Neuronexus Technologies, c) exemplary results of neuronal spiking in the intergeniculate leaflet of the rat lateral geniculate nucleus.

V. CONCLUSION

Table I presents the main parameters of NRS64 chip. Thanks to wide tuning range of its corner frequencies and functionality of single channel the presented integrated circuit can be used in many in-vivo and in-vitro experiments.

TABLE I
SUMMARY OF BASIC PARAMETERS OF THE NRS64 CHIP

Number of channels	64
Gain	139/ 1100 V/V
Tuning range for low cut-off frequency	60 mHz - 100 Hz
High cut-off frequency	4.7 kHz / 12 kHz
Power dissipation per channel	25 µW
Input referred noise (3 Hz - 12 kHz) (100 Hz - 12 kHz)	 7.6 μV_{RMS} 3.7 μV_{RMS}
Noise Efficiency Factor (3 Hz - 12 kHz) (200 Hz - 12 kHz)	 9.9 4.8
THD @ 1.5 mV	< 1%
CMRR (first/second prototype)	25/48 dB
Current stimulation with 8-bit resolution in six ranges	± (0.5; 2; 8; 32; 128; 512) µA
Readout channel supply voltage Stimulation block supply voltage	– 1.65 V, + 0.15 V – 1.65 V, + 1.65 V
Max. multiplexer frequency	5 MHz
Technology	0.18 µm
Die area	5×5 mm^2

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