34th Annual International Conference of the IEEE EMBS
San Diego, California USA, 28 August - 1 September, 2012

Virtual electrode stimulation in a multi-channel stimulation system

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Abstract— **Virtual electrode stimulation can provide extra selective spatial stimulation sites given if there is a highly configurable and controllable multi-channel stimulator system. The system has to have low latency between the loaded input data and output stimulation pulse, precise timing on simultaneously stimulation and an interface with external device such that a computer or FPGA can directly control each of the stimulation channels. This paper presents a general concept of virtual electrode stimulation and a multi-channel stimulation system that can support such operation. The system is designed in CMOS 0.35μm occupies 3.4×2.7mm^2 and consumes 2.3mW.**

I. Introduction

Electrical stimulation provides a mean to interact with the neurons—writing to the neurons as oppose to reading or recording neurons activities. To create a spike or an action potential on an axon, a voltage gradient has to occur across its membrane. It is difficult to create such a condition directly, but instead of applying an electric field, a voltage gradient will be created. The only way to apply an electric field is to create a pair of charge source and sink to pump charge between the poles or electrodes of a stimulator. A constant electric field can be created by having a constant electric current which is one of the methods of stimulation—current mode stimulation. Voltage mode stimulation is the other method that applies a constant voltage to the stimulator electrodes. This will deplete the charge carries such as Cl- ions, in the case where electrode is made of Ag/AgCl wire, because the carriers need to move into the solution in order to carry the current to create a complete circuit. As the charge carriers are depleted, the resistance increases, therefore the current drops and the applied field across the axon also drops. Thus, a voltage mode stimulation is unlikely able to produce a constant electrical field across the axon like a current mode stimulation. In addition, a current mode stimulation provides the flexibility of using different type of electrodes because a current source has a high impedance so that any load from the electrodes should not effect the output current. We begin with an introduction to virtual electrode stimulation in section II then extract the required features for a stimulation system to support those operations. Section III presents the design and architecture of a multi-channel stimulation system. Section IV lists the results of the implementation and simulations. Conclusions are in section V.

This work was supported in part by the UC Lab Fees Research Grant. The authors with to acknowledge the support of National Semiconductor for chip fabrication.

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II. Virtual Electrode Stimulation

Constructive and destructive stimuli are the results of stimulation interference due to multiple signal sources with different propagation speeds and/or paths, which suggest the possibility of creating virtual electrodes. Virtual electrodes can be created by the nearby physical electrodes, as illustrated by the hexagonal electrodes configuration in Figure 1, with the right electrode geometry parameters and stimulation pulses. They had been studied and presented in the cardiology field [1], [2] but little have been done in the area of neural stimulation.

A selective stimulation, using virtual electrode idea, is created by choosing different sets of electrodes and changing current pulses. Keynes [3] showed that there is a slow component in on-gating charge of the sodium channels such that it is possible to activate only the *neuron.Virtual* in Figure 1 because of the ultra short biphasic stimulation pulses are unlikely to activate neurons. For example, Suzuki [4] demonstrated that a short $40\mu s$ pulse can not elicit a response from a retinal degenerated mouse. By using a stochastic neuron model which is based on the EM theory, the individual ion channel model, and the compartment cable theory, we have investigated and seen that it is possible to achieve a 1:6 physical to virtual electrode ratio. This alludes to the possibility of increasing the number of stimulation sites without increasing the number of physical electrodes, making it possible to build high-density stimulation systems.

The requirements for a multi-channel stimulation system supporting virtual electrode stimulation includes a method of direct control each of the channels directly with little latency, channels can be operated simultaneously, timing and scheduling on stimulation can be done

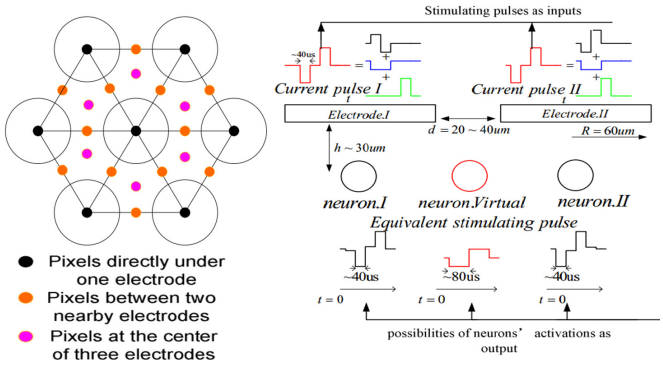


Fig. 1. Virtual electrode stimulation can be created by adjacent electrodes with the appropriate stimulation pulses and geometry parameters. A ratio up to 1:6 of physical to virtual can be achieved based on simulations using stochastic neuron model. Short biphasic stimulation pulses are unlikely to activate neurons which provides a method to create spatial selective stimulation.

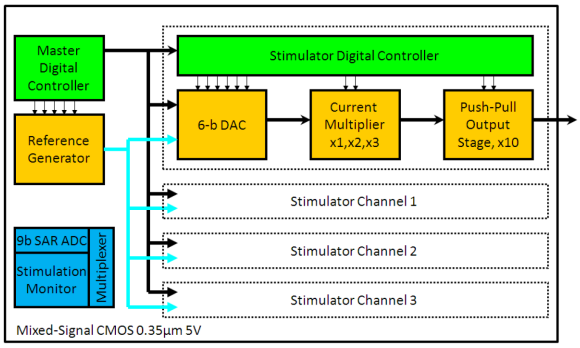


Fig. 2. A proposed multi-channel stimulator systems is composed of 32 stimulator channels with each channel has its own digital controller. A master digital controller programs and orchestrates the stimulation. On-chip reference generator provides reference currents for the DAC and on-chip bias points. A stimulation monitor observers the outputs for irregularities and provides stimulation safety.

on each of the channels with precision, and each channel can generate hundreds of microamps stimulation output.

III. Multi-channel Stimulation System

There are two options of connecting a stimulator chip to the stimulation electrodes that interface with the target tissue. In a single-voltage topology, where V_{DD} is connected to 5V and ground is zero, one supply voltage is sufficient to generate a bi-phasic stimulus through a tissue by controlling the current direction through the electrode and tissue by physically swapping the interconnections of the two electrode leads [5], [6]. In a dual-voltage topology, where V_{DD} and V_{SS} are connected to +/- 2.5V respectively and ground is zero, a bi-phasic stimulus is created by sourcing or sinking currents from and to one electrode lead. The benefit of using dual-voltage, which is implemented in this proposed design, versus single-voltage is only half of number or interconnections between the tissue and electrodes are needed. In other words, an N channels stimulator can $N-1$ as active stimulation channels and one for body ground. While with the single-voltage topology, only $N/2$ sites can be stimulated because output stimulation channels operate in pairs.

A. Architecture Overview

Controllability and precision on timing are the two crucial criteria in this proposed multi-channel stimulator system for supporting virtual electrode stimulation. The key solution for these problems is to employ synchronous digital circuitry to control the analog current stimulator drivers. Figure 2 shows a complete architecture of a multi-channel stimulation system where each of the stimulator has its own digital controller and analog submodules for generating stimulation pulses. A master digital controller supervises all stimulators, tunes reference generator and directs the SAR ADC operation.

B. Analog Current Stimulator and Reference Generator

There a number of fundamental schemes in synthesizing a DAC, mainly voltage, charge or current based architectures. Examples of these categories are resistor string, charge redistribution and current source type. For this particular neural stimulation application, current source based DAC is the best choice for a number of reasons. Recall neural stimulation requires a voltage gradient across its membrane, 'redistribution charge to the nerve tissue is a difficult problem as one has to make a device or the target tissue dynamically change their capacitance values. Through the process of elimination, stimulation can be done in either voltage and current mode, but the later approach provides immunity to resistance variation due to different type of electrodes, surrounding environments, or solutions concentrations. In addition, the operation or manipulation of current sources in CMOS technology can be done more precise and less effort than voltage sources, which alludes the schemes that DAC should be implemented in.

Figure 3 shows a complete implementation of a current stimulator based on current source and mirror concepts, where I_{copy} or I_{out} is typically equal to the ratio W/L of one transistor to another as shown by this equation [7]:

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF} \cdot \left(\frac{1+\lambda V_{DS_{out}}}{1+\lambda V_{DS_{REF}}} \right). \qquad (1)$$

The 6-bit DAC is implemented based on binary weighted cascode current sources with a reference current is in the

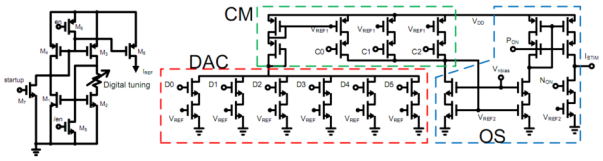
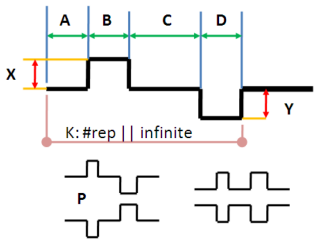


Fig. 3. The analog stimulation current driver is made up of mainly cascode current mirrors. DAC is a 6-bit binary-weight current sources. Similarly, the CM is a 3-bit binary-weighted current sources that multiples its reference current, which is the DAC's output current. The output stage is a push-pull cascode driver. The on/off switches are actually connected to bias points to increase the output voltage swing by reducing a V_{DSAT} drop. The reference current for the DAC and biases are generated from a beta multiplier referenced self-biasing. A 5-bit digital calibration is added to the beta multiplier for fine tuning the I_{ref} .



$\mathcal{R}$	Bits	Sreg[···]
A	8	[7:0]
B	8	[15:8]
C	8	[23:16]
D	16	[39:24]
X	9	[48:40]
Y	9	[57:49]
I	1	[58]
K	10	[68:59]
P	3	[71:69]

Fig. 4. A stimulator can be operated as a low latency with precise timing ADC or a standard preprogrammed pulses stimulator. There are four different type of pulses can be selected by the parameter *P*. Each of the pulse is configured by parameters *A, B, C, D, X,* and *Y* for timing and amplitude. The number of pulses is set by *K* or set to infinite with the flag *I*. The table summarizes the number of bits used for each of the parameter and the address or index of a configuration register file.

range of 0.5–2μA. Since it is implemented based on a binary weighted architecture, each adjacent bit doubles or halves (W/L) on a current source that corresponds to a factor of increase or decrease the output current, which results in 64 different possible current values at the output, ranging from 1–64μA. The transistors are sized to achieve an operation of 1MHz, which is much faster than in a typical neural stimulation where stimulation pulses have time resolution in hundreds of microseconds. Similarly, current multiplier (CM) is implemented as current sources that copies or uses current the output from the DAC as the reference current. The output stage (OS) is implemented as a simple push-pull topology which is adequate for our applications where the electrode impedance is in the range of tens Kohm.

C. Synchronous Digital Circuitry

The controllability is attributed to the digital architecture framework supporting the stimulator array. The whole digital design is divided into two major designs—stimulator and master digital controller. The stimulator digital controller has a small memory block storing a predefined stimulation pulse as shown in Figure 4. Based on the configured parameters, the stimulator digital controller activates the switches accordingly. The stimulator digital controller also has a feature of bypassing configuration parameters, transforming it into a simple ADC that can be controlled directly from an external device such as a FPGA.

The master digital controller orchestrates the stimulation. In the standard self-operated stimulation mode, where the stimulation pulses are preprogrammed, the master digital controller takes external stimulation input data, distributes and program each of the channels. It generates a prescaler clock and provide to all stimulation channels because the main digital design operates in 100MHz domain or faster while the stimulation channel operates around 1MHz. It can switch to external controlled mode, where each stimulation pulse gets a new data from the external device. In this mode, the stimulation system can generate arbitrary waveforms because for each output sample, new data can be loaded and used immediately. The master digital controller has internal timers such that multiple channels can be scheduled to execute at the same time or at a specific delayed time.

D. Stimulation Monitoring Subsystem

Stimulation monitoring subsystem provides a feedback and status on each of the stimulation channels. Its main purpose is to check voltage on the electrode and provide an output voltage value for external device to determine if the stimulation exceeds the water window. This subsystem is mainly comprised of a simple differential SAR ADC, buffers and an analog multiplexer as shown in Figure 5. The architecture of a SAR ADC is composed of mainly two large switch capacitor banks, a latch comparator, and digital logic circuitry as illustrated in Figure 6. The digital logic of the SAR state machine is merged into the previous main synchronous digital circuitry block for synthesis optimization.

IV. Implementation and Simulation Results

The proposed system is implemented with 32 channels using 0.35μm CMOS process. Analog submodules are completely separated from the digital circuitry to reduce cross-talk and digital noise. In addition to the separated well, the analog submodules use different power rails from the digital core. The whole chip as shown in Figure 9, occupies $3.4 \times 2.7 mm^2$ and consumes 2.3mW with the digital circuitry operates at 100MHz. The 32-channel analog driver array occupies only about a quarter of the whole chip. So when this design is

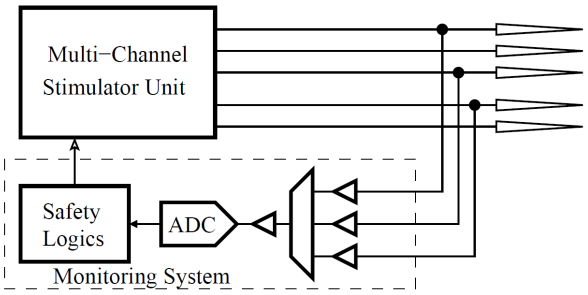


Fig. 5. The monitoring system has a SAR ADC that is shared by all the stimulation channels. Each of the output stimulation channel is probed, multiplexed and converted to digital bits. Safety logic, not implemented in this work, can be used to change the behavior of the stimulator unit.

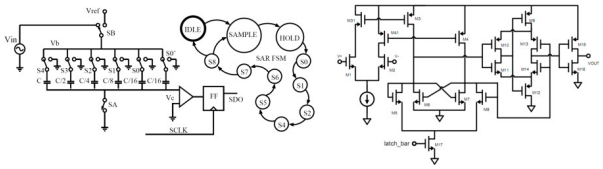


Fig. 6. A SAR ADC is utilized in stimulation monitoring system. It is actually implemented as a differential inputs SAR ADC with two sets of switch capacitor banks. The state machine and digital circuitry are implemented in Verilog controlling the switches. Left side shows a latch based comparator is employed to reduce power consumption.

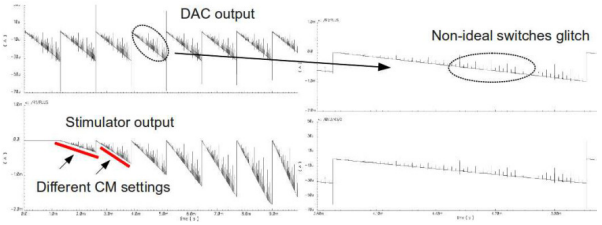


Fig. 7. A post-layout simulation of a stimulation channel output. Input is a counter implemented in Verilog model. It sweeps across different DAC and CM values. DAC can output up to $64\mu A$ while the actual stimulator output up to 2mA. There is lot of spikes around the switches transition because of many/all switches performed at the same time. To mitigate this problem, all switches except the last one that controls the push-pull driver get set prior to activating the push-pull switch.

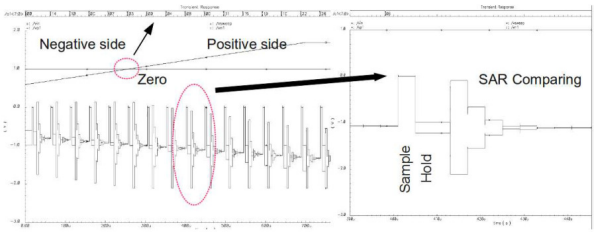


Fig. 8. A full simulation of a SAR ADC. This simulations show the transition between the difference of the inputs between negative to positive. A detail SAR conversion is shown on the right of the figure.

migrated to a better technology such as 65*nm*, then much of the space occupied by the digital circuitry can be shrunk significantly.

A. Stimulator Simulation

A complete design was extracted for parasitic components before performing a full simulation. The simulation was done in mixed-mode using Verilog model of a counter to get the test input vector. The counter sweeps across a range of number, which sets the DAC and CM switches for changing the stimulation output. Figure 7 shows a long simulation result that covered the operation of the DAC and CM and illustrated the imperfection of switches. All the digital control signals on switches happen at same time so this aggravates the spiking problem at the transitions. To mitigate this problem, values on DAC and CM should be set one clock cycle prior to activating the push-pull driver. This blocks all the spikes because only one switch is actually operated at the stimulation.

B. ADC Simulation

A post layout simulation of an SAR ADC is shown in Figure 8. An differential input pairs with one clamped at 1V and the other sweep from a voltage below 1V to above 1V. The purpose of this simulation is to show the transition between negative to positive differences between the pair. The output of the SAR is sample duration delayed after the inputs are sampled as shown in the figure. The detail operation of the SAR is depicted on the left of the figure where it shows all steps in converting analog sample to digital bits. First the differential inputs are sampled then held for a clock cycle. After this process, the successive approximations are done in eight steps.

V. Conclusions

This paper presents a highly configurable and controllable multi-channel stimulator system with the focus on the digital framework to provide an interface in creating virtual electrode stimulation. Virtual electrode can be created by the adjacent physical electrodes given right stimulation pulses can be generated with precise timing. A simple architecture for a stimulator is implemented as a current driver can generate accurate stimuli was presented. A monitoring subsystem is also included in the design to monitor the voltage at the stimulation site. The whole design occupies an area of $3.4 \times 2.7mm^2$ and consumes 2.3mW.

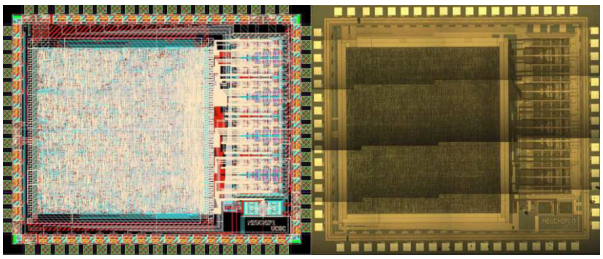


Fig. 9. The 32-channel stimulator system is implemented with CMOS $0.35\mu m$ with 4 metal layers using National Semiconductors fabrication processor. Left side of the chip is the digital controller for the stimulator IC. The right side has 32 analog stimulator drivers. Bottom right is the differential SAR ADC along with amplifiers and analog multiplexer, which are part of the monitoring system. The power ring is carefully separated so that the digital power rails do no couple noise into the analog section. The chip occupies an area of $3.4 \times 2.7mm^2$ and consumes 2.3mW.

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