34th Annual International Conference of the IEEE EMBS
San Diego, California USA, 28 August - 1 September, 2012

Architecture of a Mixed-mode Electrophysilogical Signal Acquisition Interface

Ding-Lan Shen and Jyun-Min Chen
Department of Electrical Engineering
Fu Jen Catholic University, New Taipei 24205, Taiwan

***Abstract*—This paper proposes mixed-mode architecture for the acquisition interface of electrophysiological signals. The architecture advances the analog-to-digital converter (ADC) from the second chopper signal in the conventional approach and performs the second chopper operation in the digital domain. The demanded low-pass filter (LPF) is realized with a digital type. The analog LPF in feedback path is substituted with a digital one accompanying with a digital-to-analog converter (DAC). The analog variation is decreased due to the digitization of these operations. The entire architecture is simulated with the ECG input in a behavior model of Simulink.**

I. Introduction

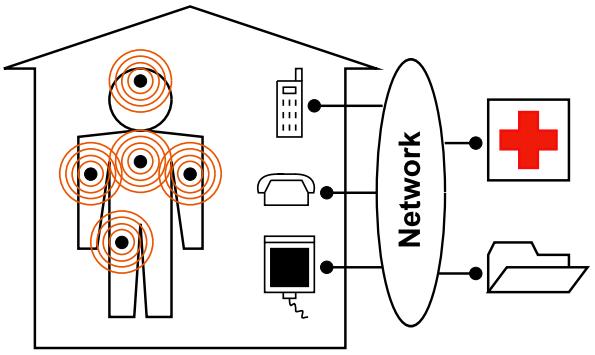

Fig. 1. Remote monitoring system of electrophysiological signals.

In the diagnosis and therapy of some patients with epilepsy or cardiopathy usually demands a long period monitoring of electrophysiological signals to acquire enough information for medical treatment. To provide the non-hospitalized monitoring in daily life, the system must be capable of small volume, low power, and short distance wireless communication accompanying with the computer network for the purpose of remote monitoring as depicted in Fig. 1 [1]. The most important key component in the monitoring systems is the electrophysiological signal acquisition circuit. The earlier approach connects the measured signals with large-scaled machine powered by the electricity system thereby limiting the activity of the patients. With the progress of integrated circuit technology, the modern trend is developing a small integrated sensor circuits which combines the digital signal processing (DSP) with digital communication techniques to achieve the requirement of portability and robustness.

The acquisition of the electrophysiological signals usually demands to amplify the weak physiological signals from the human body. In the CMOS dominated integrated-circuit process technology, circuits normally have some serious flicker noise ($1/f$) at low frequency which affects the amplification results. Accordingly, the amplifier fabricated with CMOS technology commonly applies the chopper modulation to remove the noise in the circuits [2], [3], [4], [5]. And a feedback path with a low-pass filter is included in the chopper modulation to overcome the external electrode offset. This work proposes a mix-mode electrophysiological signal sensing architecture by associating the chopper modulation technique with analog-to-digital converter (ADC) operation. This mix-mode architecture advances the ADC after the first square-wave modulation that differs from two-time square-wave modulation before analog-to-digital conversion in the conventional chopper operation. The low-pass filter in the feedback path is replaced with a digital-to-analog converter (DAC) and DSP. This early digitized approach effectively associates with the powerful DSP technique to improve the performance of the entire acquisition system.

II. Characteristic of Electrohysiological Signals

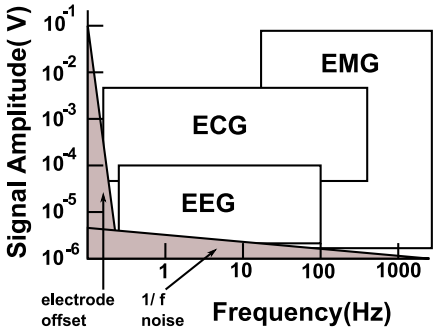

Fig. 2. Characteristic of electrophysiological signals.

The characteristic of amplitude and frequency of the usually present electrophysiological signals such as Electroencephalogram (EEG), Electrocardiogram (ECG), and Electromyogram (EMG) are depicted in Fig. 2 [6]. The amplitudes of electrophysiological signals are weak and range between several tens μV to several tens mV. Moreover, the offset induced from electrodes and the $1/f$ noise arisen from amplifiers distort the electrophysiological signals at low frequency. Consequently, the electrophysiological signal acquisition interface requires

not only large-scale amplification but also a high common-mode rejection ratio (CMRR) and a high-pass filter with ultra-low cut-off frequency to avoid the interference.

III. Mixed-mode Interface

A. Three Opamps Instrumentation Amplifier

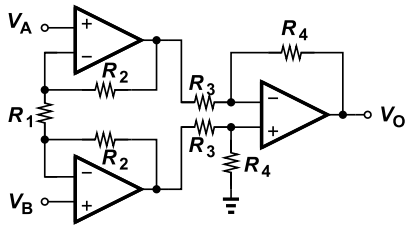

Fig. 3. Three opamps instrumentation amplifier.

The most common instrumentation amplifier is the three-opamp architecture as shown in Fig. 3. Nevertheless, the CMRR of this instrumentation amplifier is deeply affected by the matching of R_3 and R_4. In addition, the larger $1/f$ noise in modern CMOS technology and the greater power consumption in the feedback resistors prevent the application of this architecture in the design of integrated electrophysiological amplifications.

B. Chopper Modulation

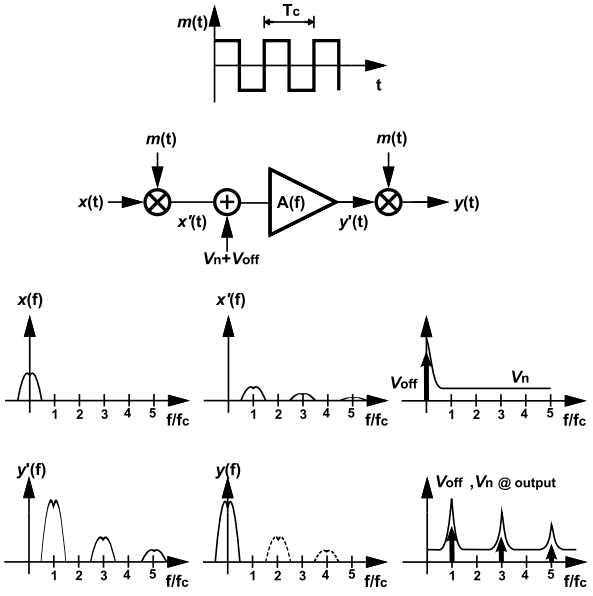

Fig. 4. Chopper modulation.

The instrumentation amplifiers with CMOS transistors usually apply chopper modulation to eliminate low frequency interference. As illustrated in Fig. 4, the input and output of the amplifier mix with a square wave , $m(t)$, which is symmetry to zero. Assume the frequency of input signal is limited within $f_c/2$, then the input square wave modulate the input signal to the odd multiple frequency of f_c. After amplification, the signal is modulated back to the baseband by the square wave at the output. If the offset and the $1/f$ noise of the amplifier is referred to the input noise, then the amplified noise is modulated to the odd multiple f_c. These high frequency noises and the higher order harmonica distortion are easily removed with a low-pass filter (LPF).

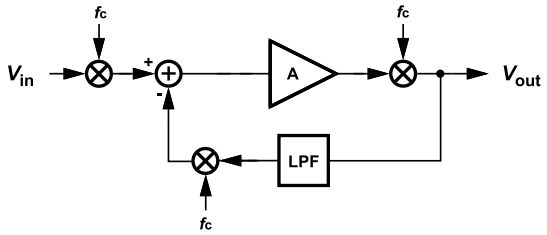

Fig. 5. AC-coupled chopper modulation.

In biomedical applications, the instrumentation amplifier has to overcome not only the self offset and $1/f$ noise but also the large offset induced by the electrode. To perform a high-pass filter (HPF) characteristics in chopper modulation without affecting the functionality, the output signal passes through a LPF and is fed back to the input of the amplifier after square wave modulation as shown in Fig. 5 [7]. Suppose order of the LPF is first with bandwidth of $\omega_{LP}/2\pi$ and f_c is larger than $\omega_{LP}/2\pi$, then the transfer function, $A_v(s)$, is obtained as

$$A_v(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{A}{1 + A \cdot \frac{\omega_{LP}}{s+\omega_{LP}}} = A \cdot \frac{s + \omega_{LP}}{s + \omega_{LP}(1 + A)} \approx A \cdot \frac{s + \omega_{LP}}{s + A\omega_{LP}}. \quad (1)$$

Therefore, the feedback path construct a HPF to prevent the saturation of the amplifier.

C. Mixed-mode Interface

The conventional CMOS electrophysiological interface usually employs the architecture in Fig. 6(a). The chopper modulation is processed in the analog domain then the output signal is digitized by the ADC. The analog signal processing does not have the strong relationship with the ADC. The ultra-low frequency LPF may demand a quite large capacitor which is not feasible to realize in the integrated chip. Consequently, the off-chip component is required and extra I/O pads increase the occupation of chip area. In this work, architecture of the mix-mode electrophysiological interface in Fig. 6(b) is proposed. The input chopper is performed in analog domain. Then the modulated signal accompanying with the feedback signal passes through the amplifier to the ADC. The architecture of the boxcar sampling [8] is associated with the chopper operation to perform some anti-aliasing filtering to avoid the high-frequency noise folding. The digitized signal is represented as the format of two's complement data. Therefore, the chopper after the amplification is accomplished with multiplying ± 1 in digital domain. Finally, this signal is processed with a digital LPF to obtain the digital-output data, D_{out}. The LPF in

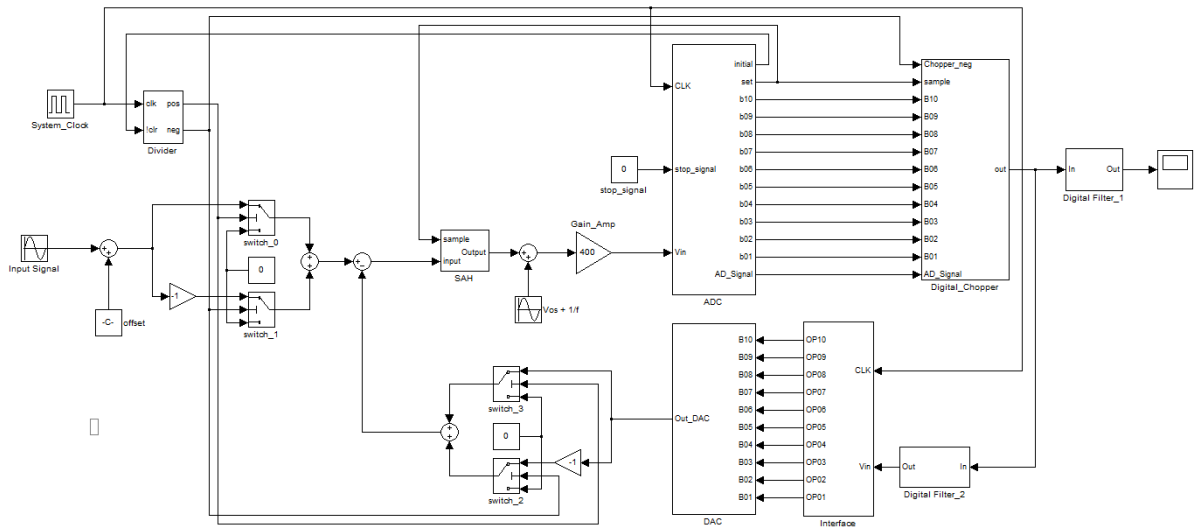

Fig. 7. Behavior model of proposed mixed-mode electrophysiological interface in Simulink.

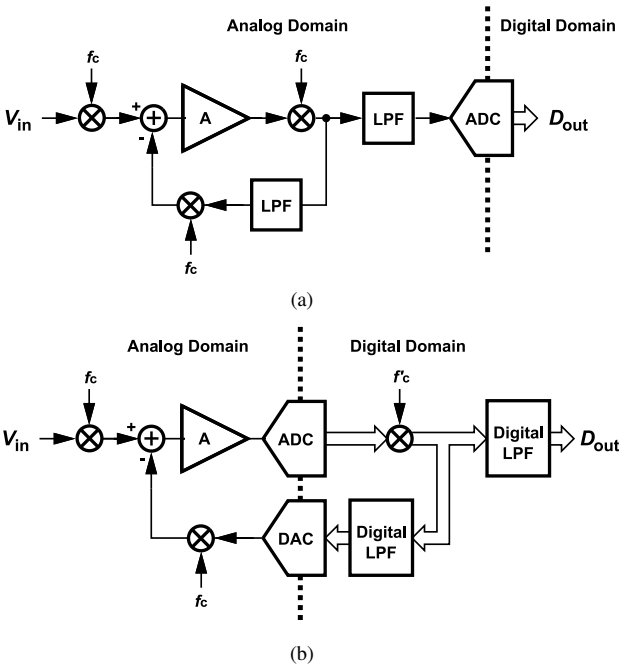

Fig. 6. (a) Conventaional mixed-mode electrophysiological interface. (b) Proposed mixed-mode electrophysiological interface.

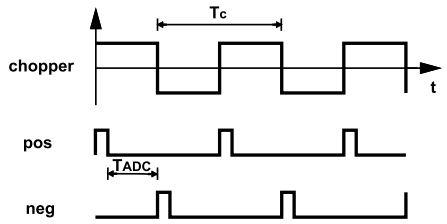

Fig. 8. Timing diagram of chopper.

feedback path is now executed with a digital LPF and a DAC. The filtered offset is modulated with the input square wave and is fed back to the input of the amplifier. This architecture digitizes the signal at earlier stage and processes the LPF in digital domain. This approach is benefited with the robustness and flexibility characteristics of today's powerful DSP.

IV. Simulation Results

The behavior model with Simulink (Matlab R2011, MathWorks Inc.) is demonstrated in Fig. 7. The frequency of the system clock is 100 kHz. The electrode offset is modeled at the input and the low-frequency flicker noise is modeled as $V_{OS} + 1/f$. Because the ADC requires a period of time (T_{ADC}) for conversion, the controlling signals of chopper are demanded to generate pos and neg as depicted in Fig. 8. The corresponding chopper signal operates at the frequency of 100/26 kHz. The sample and hold (SAH) block samples the input when pos or neg is high, and holds the sampled value during both pos and neg are low. After the first chopper modulation and amplification at the factor of 400, the input signal is digitized with a 10-bit ADC. The digitized data is choppered with the digital chopper which is realized by simply inverting the inputs depending on the chopper signal. For the convenient processing in digital domain, the individual bits are converted into decimal data. Then these data pass through the $Digital\ Filter\_1$ with bandwidth of 200 Hz to remove the high frequency harmonics. The LPF in the feedback path is achieved by the $Digital\ Filter\_2$ with bandwidth of 0.05 mHz. The outputs of $Digital\ Filter\_2$ are converted to analog signals with a 10-bit DAC, and then be choppered by the switches. After that, the siginals are fed back at the input of amplification.

Figure 9(a) is simulated input signal of ECG. The peak amplitude of this input signal is about 1 mV, and the period is about 0.833 second. The converted signal of the input

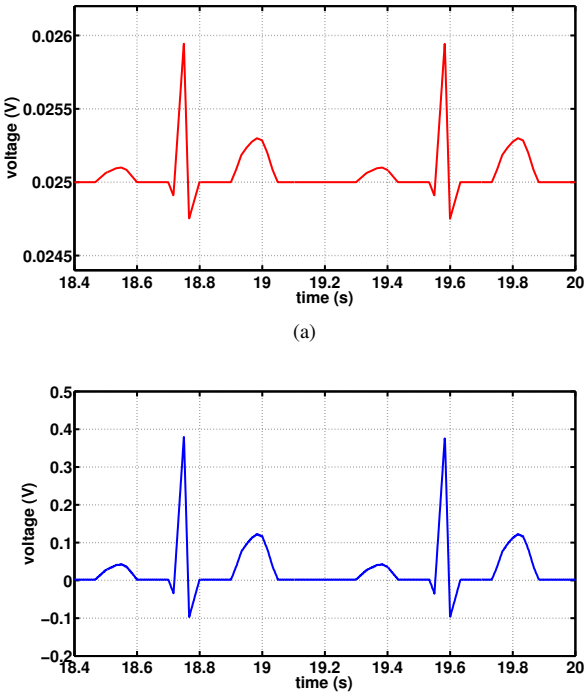

Fig. 9. (a) Input signal of ECG. (b) Converted signal of ECG.

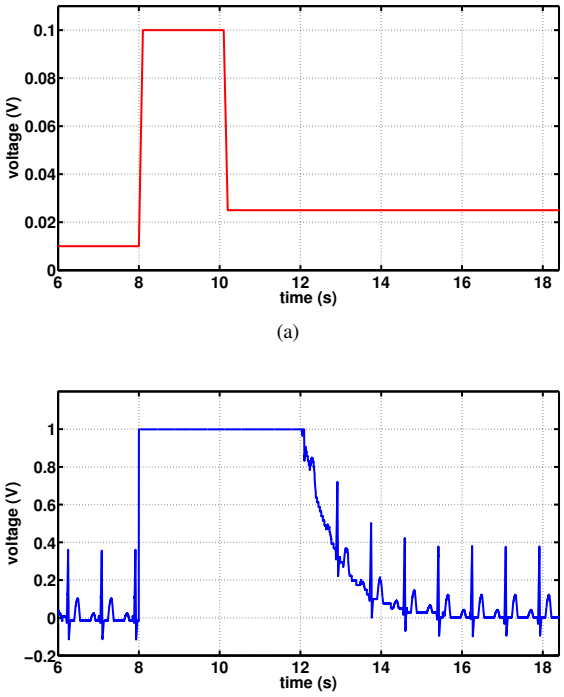

Fig. 10. (a) Simulated electrode offset at input. (b) Converted signal of ECG.

ECG after amplification is illustrated in Fig. 9(b). Since the sampling rate is relatively higher than the frequency of input ECG, the phase delay of the conversion is not obvious. The corresponding voltage amplitude of the converted digital value demonstrates the scaling factor of 400. Some transient occurs when electrocardiograph are switched from one lead to another, because there are different offset potential at each electrode. To simulate this transient response, the simulated electrode offset is applied at input as in Fig. 10(a). The initial offset is set to 10 mV. After a 2-second large pulse at 8 second, the offset is set to 25 mV. The output ECG of this interference is depicted in Fig. 10(b). The large pulse causes the output saturating at period of time, and then drifting back to the baseline with a time constant determined by the corner frequency of the LPF at the feedback path.

V. Conclusion

This paper presents mixed-mode interface architecture in the application of electrophysiological signal acquisition. In the CMOS dominated integrated-circuit process technology, circuits normally suffer from the serious flicker noise at low frequency and thereby affect the amplification of the weak physiological signals. This architecture associates the conventional chopper modulation technique with ADC's operation. The interface advances the ADC after the first square-wave modulation that differs from the two-time square-wave modulation before the analog-to-digital conversion in the conventional chopper operation. The low-pass filters after modulation and in the feedback path are replaced with digital LPFs. These digitized operations reduce the variation affection in analog components in designing the electrophysiological signal acquisition system.

Acknowledgment

The authors thanks the support of National Science Council and the simulation assistance of National Chip Implementation Center (CIC).

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