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Real Time Digitally Assisted Analog Motion Artifact Reduction in Ambulatory ECG Monitoring System

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Abstract— **This paper proposes a real time digitally assisted analog motion artifact reduction ASIC with ECG measurement simultaneously. It features one ECG monitoring and in- and quad-phase electrode-skin impedance measurement, which are used to estimate motion artifacts. The implemented ASIC is capable of actual motion artifact reduction in the analog domain before final amplification.**

I. Introduction

Motion artifacts are the biggest source of noise in portable biopotential signal recordings. These artifacts are potentials that are superimposed onto the target biopotential signal. These artifacts occur in the electrode cables, in the skin and at the electrode/electrolyte interface. While artifacts coming from cables can be reduced by appropriate electrode cables designs, artifacts from the skin and electrode/ electrolyte interface that are known to have high correlation with motion/movement artifact [1] are difficult to reduce by design. Since these artifacts may have similar frequency spectrum to the target biopotential signals, both the amplitude based and the frequency based biomedical signal analysis algorithms can significantly suffer from these motion artifacts.

A possible approach to tackle this problem is to reduce motion artifact using analog and digital filtering. Several approaches have been tried in the literature. For example, the digital adaptive filter which uses the collected signal from other sensors that have maximum correlation with the motion artifact signal and minimal correlation with the target biopotential signals as a reference can reduce the motion artifact from the biopotential signals [2]. In addition, the statistical analysis such as ICA (Independent Component Analysis) or PCA (Principal Component Analysis) algorithm can be used to remove motion artifacts in digital domain for the multi-channel biopotential signal acquisition system [3].

However the analog motion artifact reduction requires analog adaptive filter which consumes excessive power and limits its reconfigurability. Therefore purely analog motion artifact reduction is not suitable for portable biomedical applications. The various digital filters enable low power and high reconfigurable motion artifact reduction. However, the target biopotential signal in analog domain still contains the motion artifact which requires the high dynamic range for multiple analog blocks, such as ADC which induces high power consumption and large area. In addition, the target biopotential signal can be lost due to the system saturation when there is large motion artifact. In this case, the digital filtering cannot recover the lost biopotential information. To reduce the overall system power consumption and prevent loss of the target biopotential signal, the motion artifacts should be reduced in analog domain before final amplification.

The proposed system adopts a digital adaptive filter to extract the estimated motion artifact from the reference signals (In Figure1, the in- and quad–phase electrode-skin impedance signals, IMPI and IMPQ, respectively) and the input signal (In Figure1, the ECG signal with motion artifact signal, ECG+MA). The estimated motion artifact signal is converted into an analog signal through low power DAC and fed back to the input of the PGA to reduce the motion artifact in analog domain. The advantages of this solution over the existing ones can be listed as:

- Since the estimated motion artifact signal after digital adaptive filtering is subtracted from the ECG with motion artifact signal (ECG+MA) in front of the PGA, the output signal of the PGA only includes the ECG signal without motion artifact signal which enable significant reduction of the dynamic range requirements of the ADC. It leads the power and area reduction of the system.
- Since the PGA has a reference input to determine the input DC level, the estimated motion artifact signal can be applied to this reference input of the PGA. It can eliminate the requirement of the analog subtraction block to enable analog feedback.
- Since the PGA has a gain higher than 1, the feedback system doesn't require additional gain stage for feedback. It eliminates the extra power consumption and area.

II. Real Time Digitally Assisted Analog Motion Artifact Compression

A. Methodology

To reduce the motion artifact, digital adaptive filter requires reference signal which has high correlation with motion artifact and low correlation with target ECG signal. By measuring electrode-skin impedance and adopting it as a reference signal for the digital adaptive filter, this system doesn't need any extra sensors for the digitally assisted analog motion artifact reduction.

The operation of the digitally assisted analog motion artifact reduction is as follow. In Figure 1, the in- and quad-

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phase electrode-skin impedance signals (IMPI and IMPQ) and the target biopotential signal, ECG with motion artifact signal (ECG+MA), are measured simultaneously. The measured analog signals are converted to digital signals and post processed using digital adaptive filter. The 4th order least mean square (LMS) filter generates the estimated motion artifact signal from the listed input signals and feedbacks the extracted signal to the input of the PGA. The PGA performs the coarse motion artifact reduction by subtracting the estimated motion artifact signal from the measured ECG with motion artifact signal. (ECG+MA) The output of the PGA is processed again with the digital adaptive filter to estimate more accurate motion artifact signal which enables the fine motion artifact reduction.

B. *System Analysis*

Figure 1 shows the simple architecture of the proposed system. The transfer function of the system is as follow.

$$\text{Digital Output } e(n) = d(n) - y(n) = A \times [EM(n) - (1 + \frac{1}{A}) \times y(n)]$$

$$\text{Analog output } a(n) = A \times [EM(n) - y(n)]$$

It shows that cleaned ECG can be achieved after digital and analog motion artifact reduction and the difference between two outputs will be reduced if we have high PGA gain.

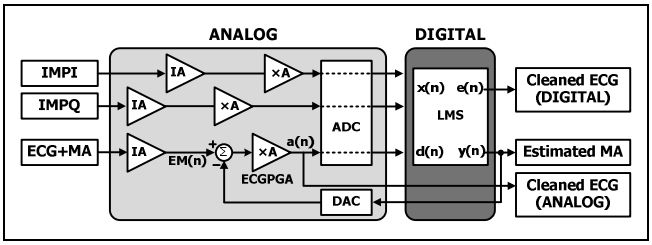

Figure 1. Architecture of the motion artifact reduction with the offchip µC

III. System Architecture

Figure 2 shows the system architecture of implemented ASIC with motion artifact reduction. The system consists of ECG readout and complex impedance readout. To accommodate electrode-skin impedance measurements, impedance channel has an AC-current source. The channel outputs are digitized by SAR ADC, which can be selectively operated at 8kS/s/channel (oversampling mode) or 500S/s/channel (normal mode). The outputs of the ADC are time-multiplexed on a master SPI output line. The outputs of the impedance channels are post-processed and fed back to the ECG channel through DAC to accomplish motion artifact suppression.

A. *Instrumentation Amplifier (IA)*

Among several requirements to enhance signal quality such as high CMRR, high input impedance, low noise, and low power consumption, one of the most important design factors is high DC electrode offset (DEO) rejection in IA, especially in multi-channel systems. To reject the DC offset efficiently without external components, a fully integrated 0.2Hz HPF is implemented with digitally controlled sub-fF capacitor tuning. It achieves 120dB CMRR, rail-to-rail DEO rejection, low power (5µA) and low noise (1.3µVrms) [4].

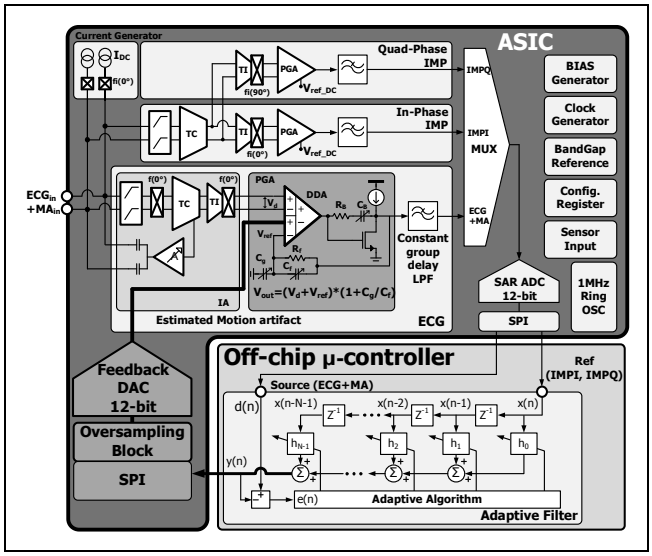

Figure 2. System Architecture of the ASIC with motion artifact reduction.

B. *Programmable Gain Amplifier (PGA)*

Figure 3 shows the proposed programmable gain amplifier to enable both variable gain functionality and analog feedback from DAC after digital adaptive filtering.

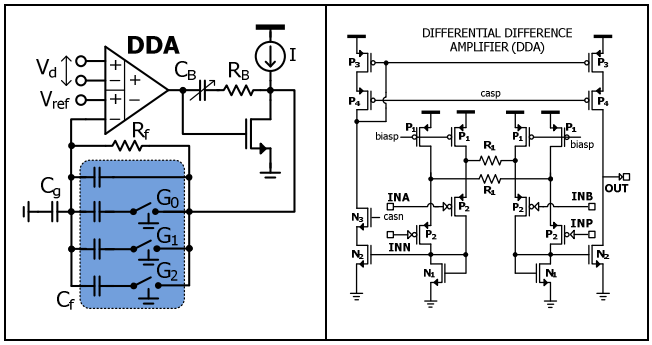

Figure 3. PGA and DDA architecture

The PGA is designed as a two stage amplifier with a differential difference amplifier (DDA) as the first stage and a common source amplifier. The AC gain of the complete PGA is given by $1+C_g/C_f$ and the DC gain is always unity. One of the main advantages of this architecture is the flexibility to set the DC output of the PGA to the voltage V_{ref}. The PGA gains are controlled by three digital inputs (G<0:2>), and the corresponding gain values are given as 1.2, 1.5, 2 and 3. In order to remove the effect of the off-state switch resistance, the variable capacitances are always connected either to the ground or to the output node. The PGA has an AC-coupled architecture that uses MOS pseudo-resistor R_f to create a unity gain configuration at very low frequencies. In order to keep the bandwidth of the PGA constant for all the gain settings, the Miller capacitance C_B is adjusted along with the gain settings. The DDA used as the core of the PGA is a circuit block whose basic property in negative feedback configuration can be described as INA-

INN=INB-INP. The source-degenerated input structure is used for better linearity of a wide range of input voltage.

The PGA behaving as a band-pass filter also introduces a group delay which is affected by both the high and low-pass cut-off. However, the worst case group delay between 10Hz-100Hz is less than 1ms.

C. Low Pass Filter with Constant Group Delay

The most important consideration to implement digitally assisted analog motion artifact reduction system is related to the channel delay. That means, two impedance channels and the ECG channel should have same group delay and these channels should have minimum delay to enhance motion artifact reduction ratio and to prevent system instability. The low-pass filter is designed to obtain constant group delay within the bandwidth of interest. Figure 4 shows the top-level schematic of the low-pass filter. The type of the filter is 4^{th} Bessel Sallen-Key filter. The cut-off frequency can be configured to 100Hz by changing the values of R_{11} and R_{12} depending on the application. The two amplifiers are used in the design are identical. The transfer function H(s) of the filter is calculated and written as the equation below:

$$H(s)=\frac{1}{\{R_{11}R_{12}C_{11}C_{12}s^2+(R_{11}C_{12}+R_{12}C_{11})s+1\}\{R_{21}R_{22}C_{21}C_{22}s^2+(R_{21}C_{22}+R_{22}C_{21})s+1\}}$$

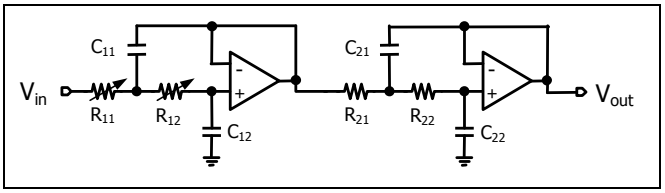

Figure 4. Architecture of the Low-pass filter

IV. Feedback DAC Design

The design of the DAC has several requirements such as resolution, output noise and power consumption to facilitate the implementation of real time motion artifact reduction for error signal subtraction from the readout channels.

A. Overall Architecture

Figure 5 shows the architecture of the implemented DAC. It consists of a main DAC with current steering architecture and a sub DAC with binary weighted resistor string and unit current sources. The output of the complete DAC can be represented by the summation of the main and sub DAC outputs as below:

$$V_{out}=V_{MAIN}+V_{SUB}$$

$$V_{MAIN}=\left(\sum_{M=0}^{A-1}b_{M+N}\times 2^M I\right)\times R, V_{SUB}=\left(\sum_{N=0}^{B-1}b_N\times 2^N R\right)\times I$$

In this implementation, the main-DAC represents the most significant 7 bits and the sub-DAC represents the least significant 5 bits of the 12-bit DAC architecture. This way of sharing the bits of the DAC significantly reduces both the area and the power dissipation.

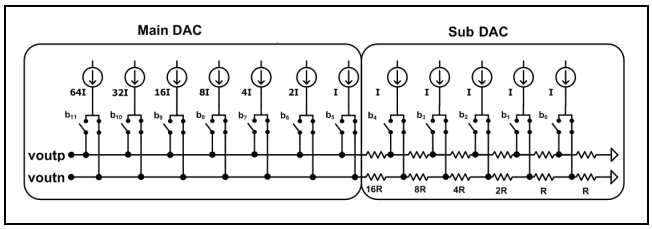

Figure 5. The architecture of the low-power 12-bit DAC

In the case when the 12-bit design would have been implemented using only Main DAC architecture and a fixed resistor, the total required current would be 4096I, whereas, if the design of the Sub-DAC is used as a 12-bit architecture a total of 2048R will be required. On the other hand, in this design the total current is 132I and the total resistance is only 32R, which is much lower in both power and area. Based on the design optimization, I and R are decided to 10nA and 24.5kΩ respectively.

B. Noise

One of the first considerations of the DAC design is the total power dissipation. This means that the current sources of the DAC should be minimized. However, this reduction in current source will require the use of larger resistors, which in turn will increase the noise of DAC. Hence, for a given noise the number of the Main-DAC bits should be minimized. The target noise level of the design was 540nV/√Hz, which is 10 times lower than the output noise of the IA, which is 5.4μV/√Hz

C. Accuracy

In this design, the increasing Main DAC bits helps reducing the mismatch of the resistors, where as increasing the Sub DAC bits reduces the mismatch of the current sources. Hence, the decision on to favour Main or Sub DAC will depend on the matching characteristics of transistors versus the matching characteristics of the resistors. As a conclusion the combined mismatch from the total resistance and the current should be such that it is much smaller than the LSB voltage of the DAC which is $1V/2^{12}$=244μV.

V. Oversampling DAC

Since the ADC in the system offers oversampled mode to enable high resolution according to different applications, the feedback DAC also have to provide high resolution to prevent loss of information when oversampled ADC is operating. The basic way to increase the resolution of the DAC is to add additional number of bits which increases design difficulties and area drastically. To increase effective resolution of the DAC without physical addition of required extra number of bits, upsampling method can be used. However, since upsampling by M gives $\log_4$ (M) bits of resolution in general, 16 times higher sampling frequency is required if 2 additional bits are required for DAC. Therefore, the DAC should operate in high sampling frequency which increases power consumption. To prevent the operation in excessively high sampling frequency and to increase the effective number of bits of the DAC without any addition of physical bits, a new oversampling method is suggested and

implemented. Figure 6 shows a principle of the oversampling DAC. Since the DAC has 12 bits and the oversampled ADC offers 14bit in our system, we will have additional 2 LSBs from the oversampled ADC which have information but cannot be used in DAC. We use these additional 2 LSBs to adopt oversampling operation with 4 time higher sampling frequency instead of 16. According to the value of 2LSB, additional pulses which have different width are added on top of the DAC output value. Since the PGA has internal low pass filter, the oversampled DAC output is averaged. Therefore, the implemented DAC has effectively 2 more bits when it is operated in oversampling mode.

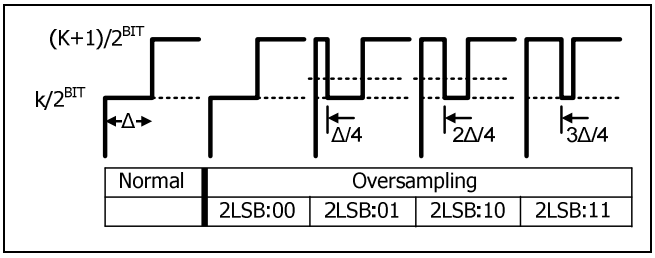

Figure 6. Operation of the proposed oversampling DAC

VI. Measurement Results

Figure 7 shows the chip micrograph of designed ASIC which is implemented in 0.18µm CMOS.

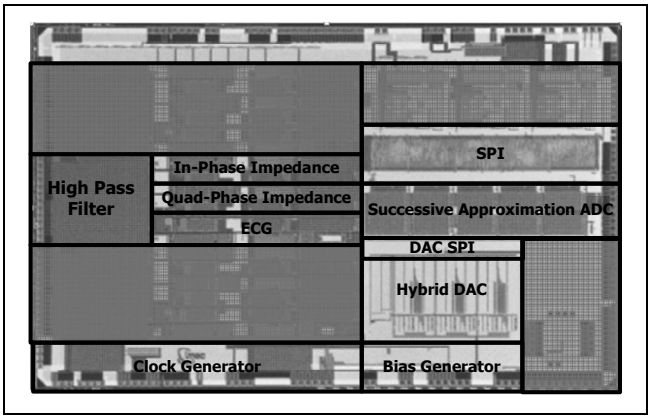

Figure 7. Chip microphoto.

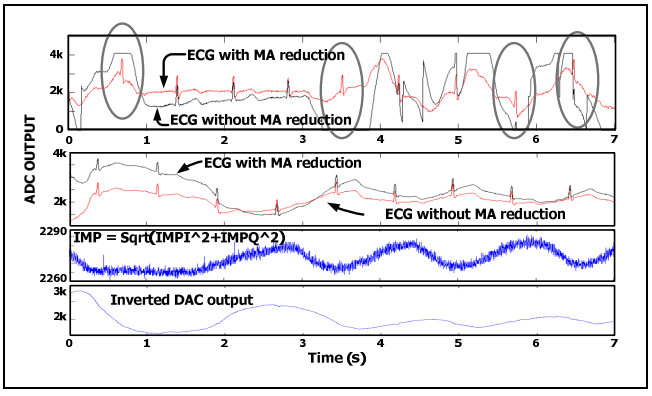

Figure 8. Measured ECG traces with and without the MA reduction

Figure 8 shows measured ECG traces with and without the motion artifact reduction, clearly showing the benefit of the proposed solution. After 5 sec, an artificatl push and pull action is given to the electrode to generate large motion artifact. Due to the channel saturation, ECG signal is disappeared and it is impossible to recover the lost information even if we try to remove motion artifact in digital domain solely. By adopting proposed method, a large motion artifact can be reduced in front of PGA to prevent channel saturation. Therefore, ECG signal can be preserved. Figure 9 shows the measurement results of DAC noise. Since the output noise of the DAC is much less than the output noise of the IA, the noise contribution of the feedback DAC to the ECG channel is negligible. Figure 10 shows the measurement results of oversampling DAC performance. Output voltage of DAC is changed linearly according to the 2 LSB values.

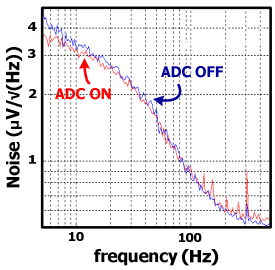

Figure 9. Measured output noise of DAC

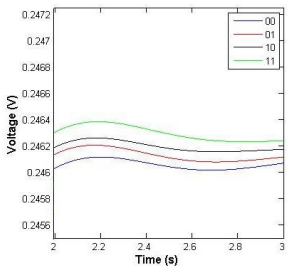

Figure 10. Oversampling results of DAC

TABLE I. Performance Results

Technology	0.18 µm	
Supply	1.2 V	
CMRR	120 dB	
ADC	> 13 bits	
Current amp.	50-2000 nA (4 step)	
Power consumption	ECG channel	8 µA
	IMP channel	13 µA
	ADC	31 µA (Norm.) / 70 µA (Over.)
	DAC	1.34 µA (Exc. bias)
	Digital+Bias	65 µA
Features	ECG + Electrode-Skin Impedance Fully integrated HPF with >1V DEO rejection Motion artifact suppression	

VII. Conclusion

The implemented system achieves digitally assisted analog motion artifact reduction through measuring in- and quad-phase electrode-skin impedance measurements and feeding back to the analog domain. This improves the ECG signal quality during ambulatory acquisition system in real time.

References

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