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Optimizing Analog-To-Digital Converters for Sampling Extracellular Potentials

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***Abstract*— In neural implants, an analog-to-digital converter (ADC) provides the delicate interface between the analog signals generated by neurological processes and the digital signal processor that is tasked to interpret these signals for instance for epileptic seizure detection or limb control. In this paper, we propose a low-power ADC architecture for neural implants that process extracellular potentials. The proposed architecture uses the spike detector that is readily available on most of these implants in a closed-loop with an ADC. The spike detector determines whether the current input signal is part of a spike or it is part of noise to adaptively determine the instantaneous sampling rate of the ADC. The proposed architecture can reduce the power consumption of a traditional ADC by 62% when sampling extracellular potentials without any significant impact on spike detection accuracy.**

I. Introduction

Design of low-power analog-to-digital converters (ADCs) for neurological implants is a vibrant area of research with many innovative proposals for achieving high resolution and high sampling rate on an extremely tight power budget. One recent research theme in ADC design for neurological implants is to incorporate signal-specific characteristics of a target application to the ADC specification so that ADC power consumption can be reduced [1]–[3].

The applications in the case of extracellular recordings usually have a signal processing path starting with spike detection and optionally continue with spike sorting followed by processors for higher functionality (such as seizure detection for epilepsy [4]).

Recent studies show ADC power consumption can be reduced by adaptively reducing the resolution of an ADC. O'Driscoll *et al.* proposed an adaptive resolution ADC [1], which goes through a training phase of 120 s, every 12 hours using a spike sorter to estimate the lowest resolution that can allow sorting spikes with a maximum allowable error rate. Sepehrian *et al.* [2] proposed a signal-specific ADC for electrocardiogram signals, where they rely on the observation that if the difference between two consecutive samples is small, the code for these samples only differ at the few low significant bits, thus just digitizing these bits at a lower resolution would be adequate yet power efficient.

Another way to reduce the ADC power consumption is to reduce its sampling rate. Yet, reducing sampling rate, if not done properly, can affect the accuracy of the subsequent stages.

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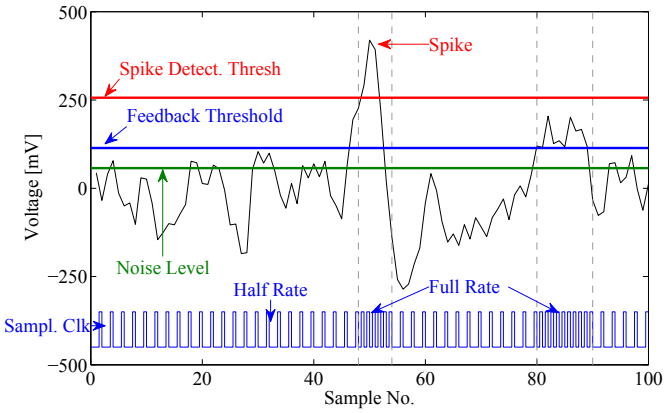

Fig. 1. An extracellular recording showing a spike, noise level, and spike detection and feedback thresholds ($10,000\times$ amplification).

In this paper, we argue that an ADC dissipates unnecessary power, if its sampling rate does not adapt to the *significance* of the instantaneous value of the neurological signal in an extracellular recording. By using the term significance, we distinguish between a sample that is significant, *i.e.,* a sample that is part of a spike and a sample that is not part of a spike (*i.e.,* noise). Since, a spike detector is readily available, and it can distinguish the spikes from the noise by means of a spike detection threshold, we propose to use this threshold as a control signal to determine the sampling rate of the ADC.

In Fig. 1, we illustrate the proposed method. When the instantaneous value of the input signal is above the spike detection threshold, this indicates that there is a spike in the signal. Then to properly sample all the samples from a spike, the ADC operates at full sampling rate above the detection threshold. The ADC sampling rate is reduced when the instantaneous value of the input signal is below the threshold *i.e.,* noise. This change in the sampling rate is represented by the sampling clock signal shown at the bottom of the figure which runs at full rate when there is a spike in the input, and at half rate, when the input is only noise. Using this approach, neither the quality of the detected spikes, nor the low-power requirements need to be sacrificed. Besides, noise information is still kept in the sampled signal (albeit at a lower quality) to aid noise level calculations. Note that, the sampling rate selection is done based on another threshold called feedback threshold in the figure, which is lower than spike detection threshold so that minor fluctuations of a spike around the spike detection threshold are not considered as noise.

We have showed that by adapting the sampling rate based

on whether the current input is part of a spike or noise, an ADC power reduction of 62% is achievable without having any significant impact on the spike detection accuracy.

The rest of this paper is organized as follows. Section II outlines the proposed ADC architecture for extracellular recordings. Section III characterizes the performance of the proposed ADC architecture. Section IV provides further discussions on the proposed architecture and Section V concludes the paper.

II. The Proposed ADC with Threshold Feedback

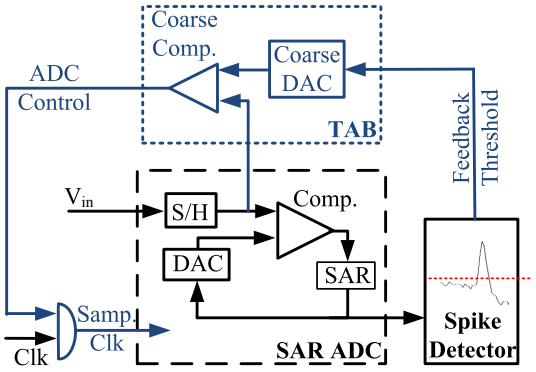

Fig. 2. The proposed ADC with the *Threshold Adaptation Block (TAB)*.

In this section, we first sketch a traditional feed-forward system where an ADC continuously converts the analog signal to digital domain and the spike detector determines the noise level and identifies the spikes. Then, we introduce the proposed closed-loop ADC architecture with a feedback from the spike detector by introducing the Threshold Adaptation Block (TAB) in Section II-C. The proposed closed-loop ADC architecture is introduced based on a regular Successive Approximation (SAR) ADC design, though, it can be beneficial to any other ADC design, as well.

A. A Traditional SAR ADC

A typical SAR ADC block diagram is shown in the dashed rectangle in Fig. 2. Briefly, the input signal v_{in} is sampled-and-held (S/H) and compared against possible values generated by the digital SAR block and converted into analog domain by the Digital-To-Analog Converter (DAC). The analog-to-digital conversion operation is carried in multiple steps as each value generated by the SAR gets progressively closer to the input value until it matches exactly with the input value. At that time, the SAR output reports the digital equivalent of the analog input, v_{in}, and thus the conversion is complete.

B. Spike Detector

Spike detection is carried in two steps: (1) noise level detection, and (2) spike detection. Background noise varies with time [5], and so we assume noise level is calculated continuously in an adaptive manner using a noise level detection method [6] (here, we use the P84 method from [5]) for each non-overlapping time window with a duration w. At the end of each window, the spike detection and feedback thresholds are updated.

Once the noise level is determined, a multiplier M is factored in to determine the spike detection threshold. The spike detection algorithm is relatively simple, any two consecutive samples above the threshold is considered to constitute a spike. Here, the following parameters are used $w = 50\ ms$, $M = 4$, and $F = 2$, where F is the multiplier for the feedback threshold. Due to the space constraints, the selection of these parameters will be covered elsewhere.

C. Threshold Adaptation Block (TAB)

The *Threshold Adaptation Block* (TAB), shown in a dotted-rectangle in Fig. 2, provides the feedback from the spike detector to the ADC to control the sampling rate of the ADC. First, a DAC converts the feedback threshold generated by the spike detector to the corresponding analog value. The comparator constantly compares the input v_{in} with this threshold. If v_{in} is found to be below the threshold, the input is considered as part of the noise and the sampling rate of the ADC is reduced by means of the ADC control signal, whereas, if the v_{in} input is above the threshold the input is considered as part of a spike, and sampled at the full rate.

The TAB is a very low-power design with minimum impact on the overall power consumption. This is mainly because the DAC is only updated infrequently once every $w = 50\ ms$ when the feedback threshold is updated, thus DAC power is negligible. Secondly, the resolution of the two components of the TAB can be made coarser compared to the comparator and the DAC of the SAR ADC, since even with low resolution the TAB can still perform well with high accuracy for spike detection (Section III).

III. Performance

In this section, we illustrate that our proposed ADC provides significant power reduction while having no or minimal influence on the spike detection accuracy.

To evaluate the proposed ADC with respect to a traditional ADC, first the TAB is designed using $180\ nm$ technology with a 1.8 V power supply and its power consumption is characterized under Cadence for 25 kS/s. The TAB consumes 304 nW power, and its power consumption is dominated by the course comparator (209 nW). For the SAR ADC power, the characteristics of a 12-bit ADC designed in the same technology node is considered [7] at 25 kS/s.

Using this power profile, we evaluate and compare the power consumption and accuracy of the open-loop ADC and the proposed closed-loop ADC architecture for various parameters in Matlab against synthetic traces [8].

To make sure the generated traces cover a reasonable range of signals encountered in extracellular recordings, the Signal-to-Noise Ratios (SNR) [6], [9] and firing rates (FR) — the average number of spikes per second — of previously acquired multi-unit recordings from rats [4] are considered.

In these recordings, we found the SNR value range between 3 and 8, and firing rates can go as high as $100\ Hz$, which are in par with previous findings [6], [8]. Accordingly,

54 10-second synthetic traces labeled with spike times are generated covering these SNR and FR ranges.

A. Accuracy

To evaluate the impact of the proposed ADC architecture on the spike detection accuracy of the spike detector, true and false positive (TP and FP) ratios are used as error metrics:

$$TP = \frac{N_i}{N}, \qquad FP = \frac{N_m}{N} \tag{1}$$

where N_i is the number of spikes correctly identified by the spike detector, N_m is the number of times a non-spike waveform is misidentified as a spike, and N is the total number of spikes in the recording.

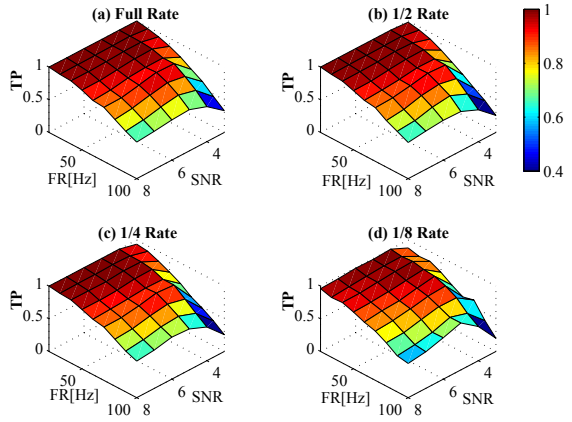

Fig. 3. The true positive (TP) ratio for various SNR and FR. (a) Open-loop setting at full sampling rate. (b)-(d) The proposed closed-loop setting. Sampling rate below feedback threshold is reduced to $1/2$, $1/4$, and $1/8$ of the full sampling rate, respectively. The feedback resolution is 8 bits.

Fig. 3 shows the TP for all the traces with respect to SNR (*x-axis*), and FR (*y-axis*) in open and closed-loop settings. In Fig. 3 (a), the TP is given for an open-loop ADC running at full sampling rate as a reference, where TP stays over 85% for SNR = 4-8, and FR up to 70 but drops rapidly below 70% for low SNR (SNR $<$ 3) and high FR (FR $>$ 90). Since, improving the spike detector performance is beyond the scope of this paper, we use these results to represent the open-loop ADC as a reference to evaluate our closed-loop design.

In Fig. 3 (b)-(d) the TP is shown for the closed-loop setting for different sampling rates below the threshold. Reducing the sampling rate below the threshold to half of the full sampling rate (Fig. 3 (b)) causes no significant change in TP with respect to the open-loop setting (the decrease in TP over the open loop case is on average 1.72% for all the traces and is no more than 3% for 82% of the traces. The maximum reduction in TP is 9.7% and it is observed for SNR $= 3$ and FR $= 80$). Further reducing the sampling rate below threshold to a quarter of the original sampling rate (Fig. 3 (c)) has hardly an impact on the TP, with an average decrease in TP of 2.64% for all the traces and is no more than 5% for 80% of the traces. When the sampling rate is reduced to one eight of the full sampling rate below the threshold, TP decrease is more pronounced though it still stays within 21% for entire SNR and FR ranges. Similarly, FP is compared in Fig. 4. When the sampling rate is reduced below the threshold in many traces, the FP rate is in fact improved around 2%, and 3%, for half and quarter of the sampling rate below the threshold, respectively. For the rest of the traces, the FP is increased only slightly (on average an increase of 0.91% and 1.75% for half and quarter of the sampling rate below the threshold, respectively.), except when sampling rate is reduced to one eighth of the full sampling rate (up to 15.16% increase in FP).

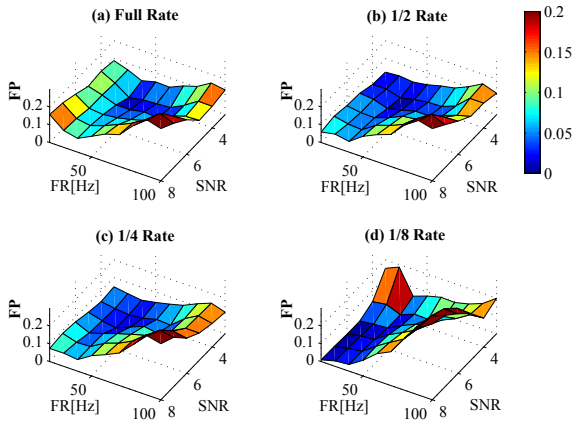

Fig. 4. The false positive (FP) ratio for various SNR and FR. (a) Open-loop setting at full sampling rate. (b)-(d) The proposed closed-loop setting.

Once the sampling rate below the threshold is determined as $1/4$ of the full sampling rate, the second parameter to determine is the resolution of the threshold feedback signal. Having a 4-bit threshold resolution, while keeping the sampling rate below the threshold as $1/4$ of the full sampling rate, decreases the TP no more than 2% for 92% of the traces and the impact on FP is even smaller. However, decreasing the threshold resolution further down to 2 bits significantly deteriorates the TP and so is not preferable.

Thus, we conclude that reducing the sampling rate as low as a quarter of the full sampling rate below the threshold and having a 4-bit feedback threshold resolution have no significant impact on the spike detector accuracy for a large range of SNR and FR values.

B. Power Consumption

To compare the power consumption of the open-loop and closed-loop ADC, we use the power profile developed at the beginning of this section. For the open-loop system we only consider the power consumption of the SAR ADC. For the closed-loop ADC, we assume the SAR ADC is in the sleep mode, when it is not sampling, and only the S/H and TAB are working, whereas when sampling, we assume both SAR ADC and the TAB are working. For instance, when evaluating the closed-loop ADC with half sampling rate below the threshold, we assume that above the threshold, the closed-loop ADC is running at full sampling

rate (25 kHz), and its power consumption is the total power consumption of the SAR ADC and the TAB. When below the threshold, we assume the closed-loop ADC is running at half sampling rate (12.5 kHZ), so it skips half of the input without sampling and SAR ADC is in sleep mode during this time but the S/H and TAB are running.

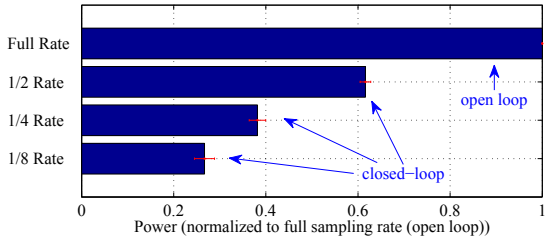

Fig. 5. Power consumption of the ADC. Feedback threshold resolution is 4 bits. The error bars representing the max. and min. power consumption for the full range of SNR and FR values shows no significant impact of neither SNR or FR on power consumption.

Fig. 5 shows the power consumption for different sampling rates below the feedback threshold. The power consumption values are normalized with respect to the open-loop full sampling rate case (top bar). The proposed method reduces the power consumption by 38%, 62%, and 73% if $1/2$, $1/4$, and $1/8$ of the full sampling rate is used below the threshold, respectively. Since, in Section III-A, it is shown that $1/4$ of the sampling rate below the threshold provides good accuracy, it can be concluded that the proposed method can reduce the power consumption by 62% without any significant impact on the accuracy.

IV. Discussions

A. Analog Spike Detection

In this paper, we assume that the spike detection threshold is calculated in the digital domain. The threshold can also be determined before the conversion to digital using analog techniques [5]. In fact, in [10] it is reported that analog spike detectors are more power-efficient at resolutions above 8-9 bits. The major reason for the higher power consumption of the digital spike detection is the need to keep the ADC on all the time to provide the digital spike detector with all the samples. Yet, digital methods are intrinsically flexible and they provide complex but more accurate techniques.

By using the proposed closed-loop ADC, we can have the best of both worlds. Using the closed-loop ADC, power consumption of the digital spike detectors can become in par with the analog-domain spike detectors, and advantages of digital processing techniques can still be fully utilized.

B. Channel Multiplexing

The proposed method implicitly assumes that the ADC is dedicated to a single channel. In many implementations, a single ADC is used to digitize multiple channels by multiplexing the channels at the input of the ADC. Since, we assume the feedback threshold is only updated infrequently, this may raise concern since the threshold can be different for each channel. There are two potential solutions for this issue. First, note that in order to support multiple channels, the only necessary addition to the TAB is additional DACs to keep the value of the feedback threshold for individual channels. Since, these DACs consume a tiny fraction of the TAB power, this does not increase the power consumption critically. Secondly, the lowest feedback threshold among multiple channels can be used as the feedback threshold of all channels. This does not degrade the accuracy but slightly reduces the power savings since a channel with an higher feedback threshold than minimum in reality, spends more time than necessary in the full sampling rate.

C. Latency

A decision based on an input value at time t to reduce or increase the sampling frequency takes effect starting from the input time $t+\Delta t$, where Δt is the duration of a single sample at the current sampling rate. Our simulations incorporate this latency, yet no noticeable impact on the accuracy is observed.

V. Conclusions

In this paper, a low-power ADC architecture for sampling extracellular recordings that eliminates two thirds of the power requirement without any significant impact on the spike detection accuracy is proposed. To operate at such low power a spike detector is used in a closed-loop with an ADC to determine the instantaneous sampling rate of the ADC.

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