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Investigation of voltage source design's for Electrical Impedance Mammography (EIM) Systems

Tabassum R Qureshi, Chris R Chatwin, Zhou Zhou, Nan Li and W Wang

Abstract: **According to Jossient, interesting characteristics of breast tissues mostly lie above 1MHz [1]; therefore a wideband excitation source covering higher frequencies (i.e. above 1MHz) is required. The main objective of this research is to establish a feasible bandwidth envelope that can be used to design a constant EIM voltage source over a wide bandwidth with low output impedance for practical implementation. An excitation source is one of the major components in bio-impedance measurement systems. In any bio-impedance measurement system the excitation source can be achieved either by injecting current and measuring the resulting voltages, or by applying voltages and measuring the current developed. This paper describes three voltage source architectures and based on their bandwidth comparison; a differential voltage controlled voltage source (VCVS) is proposed, which can be used over a wide bandwidth (>15MHz). This paper describes the performance of the designed EIM voltage source for different load conditions and load capacitances reporting signal-to-noise ratio of approx 90dB at 10MHz frequency, signal phase and maximum of 4.75kΩ source output impedance at 10MHz. Optimum data obtained using Pspice® is used to demonstrate the high-bandwidth performance of the source.**

I. INTRODUCTION

To reconstruct conductivity and permittivity distributions in the body under investigation electrical impedance mammography systems require a wide range of frequencies for the measurement of voltage and current. Previous studies show that breast tissue characteristics may be best explored above 1MHz [1]. Therefore in order to study breast tissue characteristics an EIM system should at least extend measurements up to 10MHz to effectively characterize the breast [1].

An EIM excitation system can be either a current injecting system or a voltage source system. If currents are injected, then voltages on some or all electrodes are measured. If voltages are applied, then current through the active electrodes are measured [2][3]. High precision applied and measured signals are required in an EIM system. Additional complex trimming circuits make it difficult to achieve a high precision and high output impedance using a current source [4][5]. Precision is also degraded if we are dealing with a wide range of frequencies.

A voltage source with high precision can be implemented using a broadband operational amplifier [2][3][6][7][8][9] to overcome the current source problems which are generally less costly and easier to implement. However, while designing a voltage source it is desirable to know the applied voltage and its resulting current. If a constant voltage drop is desired across a wide range of load impedances, then the voltage source should have low output impedance.

This paper describes three voltage source circuitries. Based on preliminary voltage source results, the circuitry which gives best bandwidth is chosen to design a differential voltage source along with its other performance parameter. All voltage source design has a current sensing capability with variable voltage gain and controllable feedback current. Depending upon the requirement, the voltage gain of the system is fixed and can be used to determine feedback current. The purpose of the feedback path is to control the current passing through the load. In this paper primarily the bandwidth of the design is considered along with other performance parameters like output impedance, SNR etc. The circuitry is designed to achieve a bandwidth of greater than 15MHz over a wide a range of loads in the presence of load capacitance and to achieve as low an output impedance as possible without any oscillation in the system at higher frequencies. Preliminary simulation results are generated to establish the bandwidth performance of the source.

II. SOURCE ARCHITECTURE

Three suggested voltage source architectures are shown in figures 1, 2 and 3 respectively. These sources have an ability to sense how much current is generated / injected into the object and it can also control the maximum amount of current passing through the load. The current flowing through the load is limited by the feedback path. These sources give a voltage gain depending upon the requirement of the system.

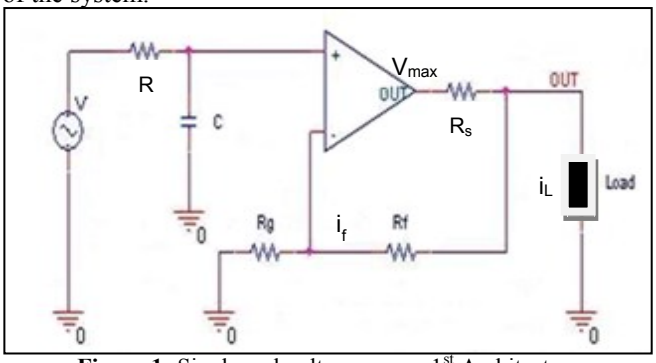

Figure 1: Single end voltage source 1st Architecture

T R Qureshi is with School of Engineering & Informatics, University of Sussex Brighton UK BN1 9QT, on leave from COMSATS Institute of Information Technology Islamabad, Pakistan for PhD studies. (+44 750 618 7973; e-mail: t.r.qureshi@sussex.ac.uk).

C R Chatwin, is with School of Engineering & Informatics, University of Sussex, Brighton UK BN1 9QT, (c.r.chatwin@sussex.ac.uk).

Zhou Zhou is with College of Electrical Science and Engg, National University of Defense Technology, China, (zhouzhou@gfkd.edu.cn).

Nan Li is with School of Engineering & Informatics, University of Sussex, Brighton UK BN1 9QT, (N.Li@sussex.ac.uk).

Wei Wang , is with School of Engineering & Informatics, University of Sussex, Brighton UK BN1 9QT, (Wei.wang@sussex.ac.uk)

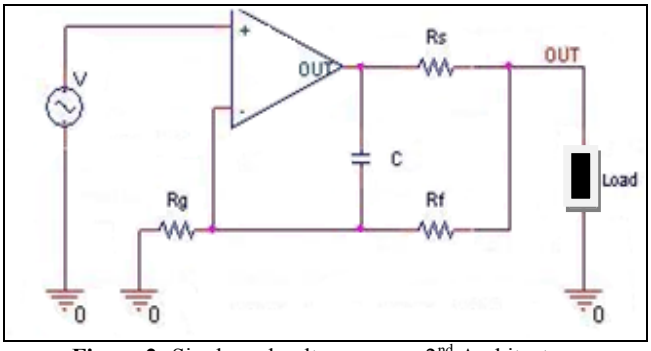

Figure 2: Single end voltage source 2nd Architecture

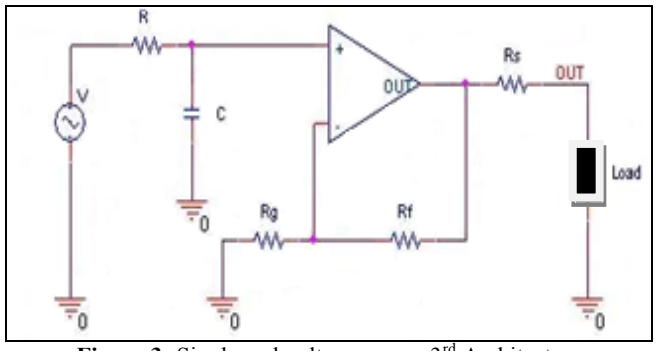

Figure 3: Single end voltage source 3rd Architecture

The three architectures shown in figures 1, 2 & 3 were simulated with exactly the same circuit parameters. The circuits were also simulated with a load capacitance of 30pF, 50pF and 100pF parallel with load values of 5k, 10k, 15k, 20k, 25k and 30k ohms. The initial bandwidth result using the above architectures show that the first architecture provides better performance over a wide range of frequencies as compared to the other two architectures. The detailed bandwidth results for the above architectures are given in the table 1.

Therefore the 1st architecture shown in figure 1 was chosen to design the differential voltage source; detailed source performance results are established which are described in the methodology and results section.

The output current for the operational amplifier using the 1st architecture is given by:

$$i_s = \left[\frac{(R_g + R_f) + R_L}{R_g R_L}\right] V_{in} \qquad (1)$$

The maximum operational amplifier output using 1st architecture is given by:

$$V_{max} = \left[\frac{R_s R_L + (R_s + R_L)(R_g + R_f)}{R_g R_L}\right] V_{in} \qquad (2)$$

Current passing through load depends upon the voltage gain of the system and can be expressed as:

$$i_L = \left[\frac{R_g + R_f}{R_g R_L}\right] V_{in} \qquad (3)$$

III. METHODOLOGY

The circuit shown in figure 1 was simulated using Pspice® over a wide range of frequencies i.e. up to 1GHz. In order to facilitate high frequency capabilities wide bandwidth components were chosen. The device selected as a source

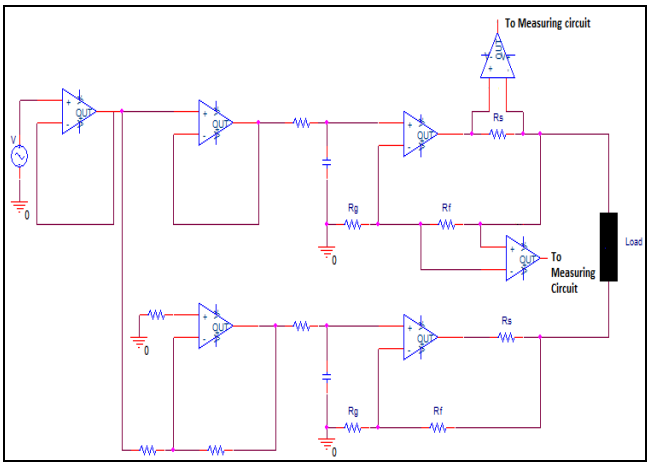

Figure 4: Differential source architecture

was the OPA656 from Texas instruments whose unity gain bandwidth product is 500 MHz and can give 230 MHz gain bandwidth product with a gain of greater than 10. The minimum theoretical value of the load was assumed and the circuit was tuned in such a manner that a constant voltage was dropped across the load with a maximum amount of current (i.e. 1mA) passing through the load. As mentioned earlier this is a preliminary investigation of VCVS therefore the current monitoring for medical safety standard was not considered at this stage and the design was tested to check the maximum achievable performance based on certain fixed parameters.

A differential amplifier was used across the sense resistor R_s to indirectly measure how much current was generated / injected into the object. Another differential amplifier was used across a feedback resistor R_f to measure the amount of feedback current. The difference of I_{sense} and $I_{feedback}$ can be used to know the amount of current injected into the object. The op-amp output voltage varies with the change of the sense resistor R_s, as mentioned in equation 2. Firstly, the voltage gain of the system is set according to our requirement. Theoretically the maximum current (i.e. 1mA) will pass through the load when the ratio of load and voltage gain becomes 1. For this case that value of the load can be considered as the minimum value of load attached to the source having a maximum current of 1mA. To find the optimum value of R_s, the value of V_{max} can be fixed in equation 2 and can be expressed as,

$$R_s = \frac{V_{max} R_g R_L - (R_g + R_f) R_L V_{in}}{V_{in}(R_L + R_g + R_f)} \qquad (4)$$

The circuit was tested in the presence of load capacitance and the results are shown in the following section.

IV. RESULT AND DISCUSSION

The differential source circuit shown in figure 4 was simulated with an ideal and non-ideal amplifier. System gain was set to 2.5. Theoretically, the amount of maximum current to be injected is known. By knowing the voltage gain and injected current the load value can be predicted. This load value can be the minimum condition to allow maximum current. Load values tested are 5k, 10k, 15k, 20k, 25k, 30k, 35k, 40k, 45k and 50k ohms in differential mode.

A single source signal was used to test the circuitry. In order to make a differential source, the generated signal was inverted using additional circuitry and both inverted and non-inverted signals were applied to the load simultaneously. (i.e. V^+ & V^-). There is a slight difference in bandwidth of the individual voltage pulse (V^+ & V^-) when applied in differential mode. An additional RC circuit was used before the voltage source to minimize this difference and to control the oscillation in the system at higher frequency as shown in figure 1. To set a gain we need to specify feedback resistor values. Any of the feedback resistors can be fixed. Suppose the value of R_g is fixed. Depending upon the predefined gain of the circuit, R_f can be calculated as:

$$R_f = (Gain - 1)\, R_g$$

The circuit was simulated in the presence of load capacitances i.e. 10pF, 30pF, 50pF and 100pF. The simulation result shows that in the presence of load capacitance the circuit shows some oscillation at higher frequencies i.e. above 5MHz. In order to control this; an additional capacitor was added in parallel with the sense resistor. The result shows that the bandwidth of the circuit not only remains stable with the increase in load but also increases with the decrease in load capacitance. Simulation results with load capacitance 10pF and 50pF are shown in figure 5 and 6 respectively.

The bandwidth using ideal device is limited by the cut off value of the RC circuit. This cut off value is used to remove the oscillation in the system at higher frequencies and to minimize the difference in the bandwidth of V^+ & V^-. Results show that by adjusting the RC circuit values the difference can be minimized to approx. less than 3%. The detailed bandwidth difference of V^+ & V^- is mentioned in table 6. Result shows that if load capacitance is decreased higher bandwidth can be achieved. The average bandwidth achieved with 10pF, 30pF, 50pF and 100pF load capacitance are 20.81MHz, 22.15 MHz, 23.40 MHz and 26.30MHz respectively. The bandwidth achieved using different loads are shown in Table 3. The bandwidth achieved in the table 3 is -3db point of the original signal. Ryan Halter [3] reported an EIT system which can achieve a system bandwidth between 10 – 12.5 MHz. If the design is fabricated with high accuracy and precision then the design will less effected by stray capacitance. As a result a wider bandwidth system greater than 12 MHz can be achieved.

The phase difference between the input and output signal is also considered. The result shows that there is phase difference of approx -3˚ to -62˚ across the whole range of tested load for a positive terminal output voltage and a phase difference of approx 180˚ to 113˚ with a negative terminal output voltage. Phase difference is very small until 1MHz and increases above this frequency. Detailed phase difference is described in Table 2.

Signal-to-noise ratio is shown in figure 7. SNR remains within defined limits for different values of loads and load capacitance. This limit varies between 127dB to 80dB. SNR was calculated using Pspice® Noise analysis functions. At each frequency, the total noise contribution was calculated in Pspice®. Probes were used to measure the total RMS noise across the band. The total noise is the overall variance of the combined noise fluctuations at each frequency. The total noise power was calculated by squaring the RMS-summed output noise for the entire circuit. The average signal power was assumed to be 2.5V ideally according to the set gain for the circuit. Signal-to-noise ratio is determined from equation 5. Ryan Halter [8] claims a SNR of greater then 94dB up to 2 MHz, 90dB up to 7 MHz and 65dB at 10 MHz.

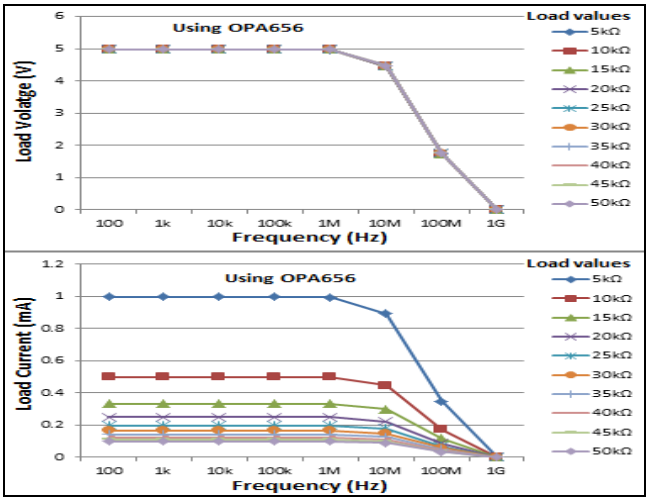

Figure 5: Load current and voltage with 10pF load capacitance

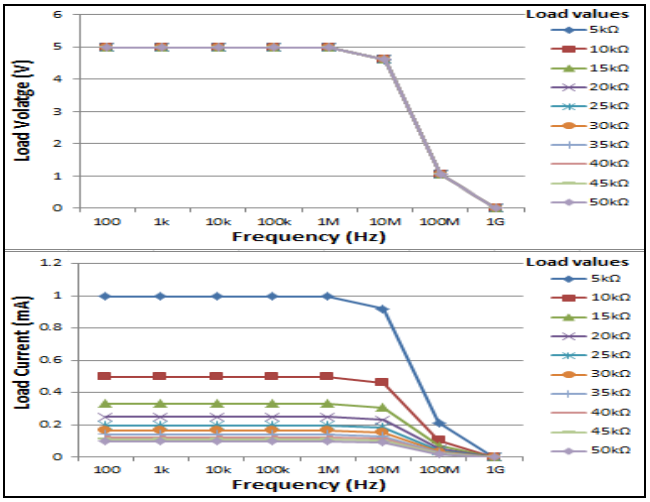

Figure 6: Load current and voltage with 50pF load capacitance

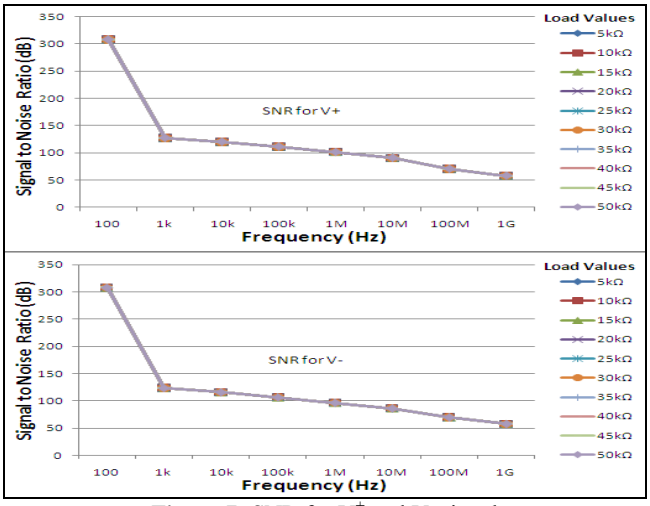

Figure 7: SNR for V^+ and V^- signal

According to our findings a SNR of 100 dB up to 1 MHz and between 100 to 90 dB up to 10 MHz can be achieved by building good quality printed circuit boards and by minimizing the on board parasitic impedances. Detailed SNR is given in Table 4.

$$SNR = 20\ log_{10}\left(\frac{Signal}{Total\ noise}\right) \qquad (5)$$

Ideally, the voltage source should have zero output impedance. Practically it is not possible; but to get better performance it should be as low as possible. The circuit had been simulated to evaluate the output impedance for various frequencies. The results show that output impedance varies between approx 13Ω to 4.75kΩ. The entire circuit is converted into its Thevenin's equivalent and the output impedance / resistance and can be determined using the voltage divider rule as shown in equation 6. The detailed output impedance is described in Table 5.

$$Z_{Out} = \frac{Z_{Load}V_{in} - V_{Load}Z_{Load}}{V_{Load}} \qquad (6)$$

TABLE 1: INITIAL BANDWIDTH RESULT FOR VOLTAGE SOURCE ARCHITECTURES

Load (k Ω)	Bandwidth (M Hz)			Load Cap (pF)
	1st Architecture	2nd Architecture	3rd Architecture	
5 - 30	27.82 – 28.39	21.74 – 22.37	6.03 – 5.26	30
5 - 30	17.35 - 17.62	19.71 – 20.11	3.73 – 3.23	50
5 - 30	15.52 – 15.70	14.97 – 15.15	1.89 – 1.63	100

TABLE 2: PHASE DIFFERENCE OF INPUT VS OUTPUT VOLTAGE AT 5K AND 30K LOAD WITH 10pF LOAD CAPACITANCE

Frequency (Hz)	V+		V-	
	Input	Output	Input	Output
100k	0°	0°	0°	180°
1M	0°	-3.55°	0°	176°
10M	-1.70°	-35°	-1.70°	142°
20M	-3.41°	-62°	-3.41°	113°

TABLE 3: LOAD VOLTAGE BANDWIDTH AT CORRESPONDING LOADS

Load (Ω)	Bandwidth (MHz)				
	Ideal Device	Non Ideal Device			
		Load Capacitance (pF)			
		10	30	50	100
5k	>30	20.69	22.04	23.26	26.16
10k	>30	20.80	22.16	23.39	26.26
15k	>30	20.83	22.20	23.43	26.30
20k	>30	20.85	22.22	23.45	26.31
25k	>30	20.86	22.23	23.47	26.32
30k	>30	20.87	22.24	23.48	26.33
35k	>30	20.87	22.24	23.48	26.33
40k	>30	20.88	22.25	23.49	26.34
45k	>30	20.88	22.25	23.49	26.34
50k	>30	20.88	22.25	23.49	26.34

TABLE 4: SIGNAL-TO-NOISE RATIO FOR VOLTAGE SOURCE

Frequency (Hz)	SNR (dB)	
	V^+	V^-
1k - 100k	127 – 110	123 – 106
100k – 1M	110 – 101	106 – 96
1M – 10M	101 – 90	96 – 86
10M – 30M	90 - 83	86 – 80

TABLE 5: OUTPUT IMPEDANCE FOR VOLTAGE SOURCE WITH 10pF LOAD CAPACITANCE

Load (Ω)	Output Impedance (Ω)		
	100kHz	1MHz	10MHz
5k	13.23	16.86	492
10k	25.67	32.51	965
15k	37.90	48.15	1.44k
20k	50.53	64.21	1.91k
25k	63.16	80.26	2.38k
30k	75.91	96.31	2.86k
35k	88.43	112.36	3.33k
40k	101.05	128.41	3.80k
45k	113.67	144.46	4.28k
50k	126.32	160.51	4.75k

TABLE 6: BANDWIDTH DIFFERENCE OF VOLTAGE SIGNAL WITH 10pF LOAD CAPACITANCE

Load (k Ω)	Bandwidth (MHz)		Difference (%age)
	V+	V-	
5 – 50	21.00 – 21.18	20.43 – 20.62	< 3% approx.

V. CONCLUSION

A voltage controlled voltage source (VCVS) has been simulated in this paper with a non-ideal operational amplifier for the EIM system. The best possible source architecture has been presented among different architectures. The behavior of the circuit is described using theoretical equations. The source has been simulated over a wide band of frequencies with the presence of load capacitance. Other performance parameters like output impedance, Signal-to-noise ratio, Magnitude and signal phase are also reported. Efforts have been made to increase the bandwidth of the source and have achieved a bandwidth of greater than 15MHz. The source has achieved low output impedance with an acceptable level of SNR. As mentioned earlier, medical safety standards will be added once the maximum possible performance of the voltage source has been achieved.

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