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Recent Advances in Power Efficient Output Stage for High Density Implantable Stimulators

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Abstract— **A major drawback of a current-controlled stimulation is its power efficiency. However, it is commonly used in implantable stimulators due to its safety. The power efficiency of a current-controlled stimulation can be improved by reducing the headroom voltage needed in the current driver. A promising technique is to bias the transistor in triode region whereas improving output impedance through the regulated cascode structure. This comes with a feature of implicit compliance monitor which is used for the supply voltage adaptation. This paper presents an overview on recent power efficient high voltage-compliance output drivers.**

I. INTRODUCTION

Functional electrical stimulation (FES) has been used to overcome missing or lost body functions, such as the cochlear or retinal implants. The goal of an implantable stimulator is to excite a neural reaction upon the transfer of electric charge into the tissue. Commonly used techniques to transfer the charge are voltage-controlled and current-controlled stimulation.

A current-controlled stimulation is preferred over a voltage-controlled because the level of neuronal membrane depolarization is directly related to the injected charge [1]. Since the electrode-tissue interface impedances are time-dependent variable, a current-controlled stimulation can provide a constant excitation regardless of the impedances, while the stimulus voltage has to be adapted regularly in a voltage-controlled stimulation in order to maintain the level of excitation. However, a voltage-controlled is commonly employed in high current stimulators because of its higher power efficiency in order to increase the battery life time and reduce power dissipation in general [2].

In high electrode density applications such as retinal implants, area and power consumptions are of most importance. Both area and power consumptions are dominanted by the stimulator front-ends, especially the current drivers, which are typically implemented using one current source per one or two electrodes. These current drivers need some headroom voltage (V_{HR}) across their output transistors in order to provide constant currents, for instance, approximately 2V headroom voltage was required in the high voltage (HV) compatible current driver in [3]. As shown in Fig. 1, the headroom voltage reduces the voltage-compliance

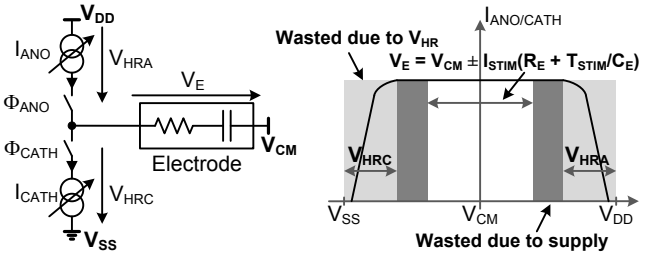

Fig. 1. A biphasic current stimulator with its voltage/current relationship. The power which is not functionally needed is obviously shown in the shaded region.

with respect to the supply voltage, and increases the power consumption of the stimulator. Thus, one way to improve the power efficiency in current-controlled stimulator is to reduce the headroom voltage of the current driver. Moreover, a stimulator is typically supplied with a constant supply voltage which is calculated under worst-case assumption of the required electrode voltage swing. The latter is given by the assumed electrode impedance and the required maximum stimulus current. In case the electrode impedance is smaller than expected or the stimulus current is smaller than the worst-case maximum, a major part of the power dissipation is wasted for too large compliance or supply. Hence, the power supply for an implantable stimulator should be adapted to the needed value for the ongoing stimulus current and electrode impedance.

This paper reviews recent advances in power efficient output stages for implantable stimulators and also presents a new power efficient, high voltage-compliance output current driver for implantable stimulators. The headroom voltage in this stimulator is reduced by using a symmetrical regulated cascode current mirror [4], [5]. This structure also gives the possibility to simply detect the voltage-compliance which can be used to adapt the supply voltage. The power consumption is reduced further by applying a current-copying approach [6] in which the biasing branch is needed only a fraction of time.

Part of this paper has been published in [7].

II. STATE-OF-THE-ART

Current mirrors are typically employed to transfer the stimulus current from a digital-to-analog converter (DAC) to the electrode. In order to operate properly, the transistors in the current mirror must be in saturation region. This means they require a minimum drain-source voltage of

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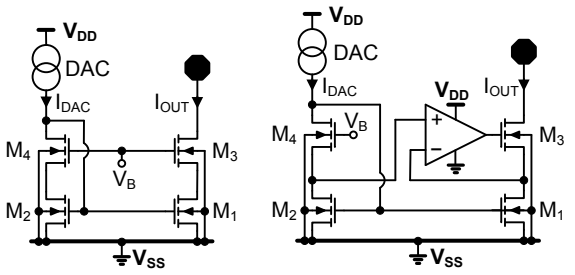

Fig. 2. (a) Typical wide-swing cascode current mirror and (b) with output impedance boosted via active feedback [10], [11].

$$V_{DSsat} = \sqrt{\frac{2I_{OUT}L}{K_pW}} \tag{1}$$

where I_{OUT} is the stimulus output current, K_p is the intrinsic transconductance, and W and L are the transistor dimension, respectively. The output impedance (r_{out}) of current mirror is equal to the drain-source impedance (r_{ds}) of the output transistor which is not high enough for biomedical applications.

To improve the output impedance, a fully cascode current mirror is employed [8] which improves the output impedance by a factor of $g_m r_{ds}$, where g_m is the transconductance of the cascode transistor. However, it needs at least $2V_{DSsat} + V_{TH}$ headroom voltage, where V_{TH} is the threshold voltage, which decreases the voltage-compliance.

In order to efficiently deliver the charge into the tissue, the highly compliant output stage is developed based on reducing the headroom voltage while maintaining the high output impedance.

A. Wide-Swing Cascode

In a wide-swing cascode as illustrated in Fig. 2(a) [9], the stacking transistors are biased by an external voltage as opposed to a fully cascode current mirror. The headroom voltage can be reduced to $2V_{DSsat}$ by adjusting the biasing voltage V_B. Furthermore, the output impedance can be enhanced by applying an active feedback to the circuit as shown in Fig. 2(b) [10], [11]. The output impedance is given by

$$r_{out} = Ag_{m3}r_{ds3}r_{ds1} \tag{2}$$

where A is the amplifier gain, g_{m3} is the transconductance of transistor M_3, and r_{ds1} and r_{ds3} are the output impedance of the transistor M_1 and M_3, respectively.

From (1), it is obvious that the voltage-compliance of this topology depends on the output current, since both output transistors (M_1 and M_3) operate in saturation region.

B. Voltage Controlled Resistor

Another method to reduce the headroom voltage of the current driver is to apply a voltage controlled resistor (VCR) concept to the current generation part of the current driver.

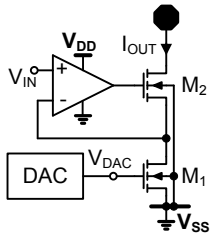

Fig. 3. A voltage controlled resistor based current driver where a linearization circuit is incorporated with the DAC [2].

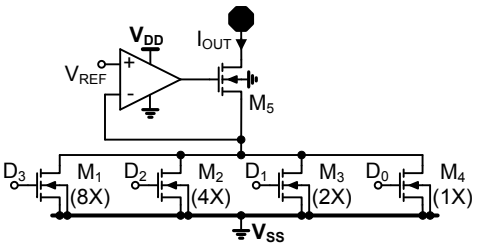

Fig. 4. Binary weighted controlled resistor [12].

The circuit is depicted in Fig. 3 [2], where the linearly biased transistor M_1 acts as a resistor controlled by the output voltage of a DAC. The output current is then set by the bias voltage V_{IN} and r_{ds} of transistor M_1. By operating M_1 in deep triode region, the bias voltage V_{IN} can be set to a small value. Hence, the required headroom voltage is reduced to be $V_{DSsat2} + V_{IN}$. In addition, the output impedance is boosted through the regulated cascode structure. Again, the output impedance can be calculated using (2).

However, since a voltage DAC was used in [2] as the input to gate of M_1, a linearization circuit is needed to minimize the non-linearity between the gate voltage to the drain current of transistor M_1, especially if a wide output current range has to be provided. This increases the area and power consumptions of this topology [2].

C. Binary-Weighted Transistors as Current DAC

In order to get rid of the linearization circuit in the previous VCR topology, the binary-weighted transistors as current-mode DAC was introduced in [12]. Fig. 4 shows the circuit where all VCR transistors M_1 to M_4 are biased with either V_{SS} for logic '0' or a constant voltage for logic '1'. The voltage-compliance and output impedance are high as in the VCR topology. However, this is not appropriate for a biphasic current driver, especially in HV applications. This is because it requires a high number of switches and level shifters to drive these switches.

D. Symmetrical Regulated Cascode

In Fig.5, a symmetrical regulated cascode with current mirror operated in the triode region is illustrated [4], [5]. By combining the linearity advantage of a current mirror with the voltage controlled resistor topology, the circuit provides high voltage compliance with high output impedance without the need for a linearization circuit. Since there is no need

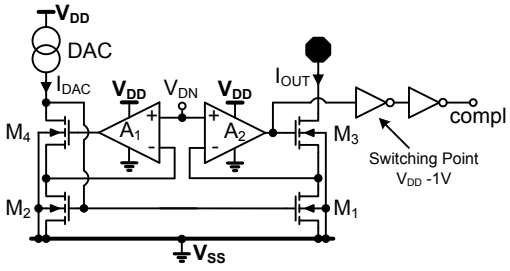

Fig. 5. A symmetrical regulated cascode current mirror where the mirror transistors (M_1 and M_2) are biased in triode region with a compliance monitor.

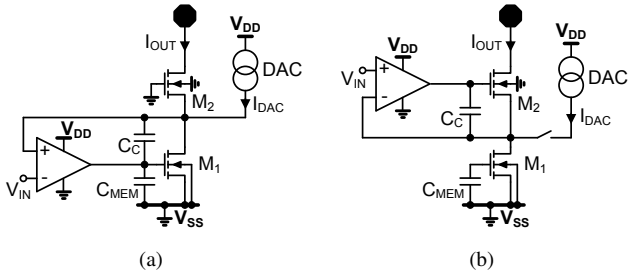

Fig. 6. Operation of current-copying stimulator; (a) storage phase and (b) stimulation phase [6].

to switch several binary-weighted transistor as in [12], this circuit is suitable for HV applications.

However, one important factor that needs to be concerned in this structure is the current mismatch. There are two sources of mismatch, one from the current mirror transistors M_1 and M_2, and another one from the difference in the controlled bias voltage V_{DN} caused by amplifiers A_1 and A_2 [5].

In addition to the advantage concerning the voltage-compliance, this structure allows to effectively monitor the currently available compliance of the output stage [4], [5]. This is done by monitoring the feedback mechanism of the regulated cascode loop. If the current driver is running into a compliance problem, the output current starts to drop, the feedback loop counteracts by increasing the amplifier output voltage towards V_{DD}. The compliance monitor is simply a level detector of this output voltage through an inverter with switching point around $V_{DD} - 1V$. Using the compliance monitor with an adaptive power supply, the stimulator then consumes only the just needed power based on stimulus current and electrode impedance.

III. POWER AND AREA REDUCTION

Two major disadvantages of all current mirror based stimulators are the static power consumption in the biasing branch and the usage of the current-mode DAC in every current driver. In order to overcome these drawbacks, a current-copying stimulator was proposed in [6]. It operates in two phases: during storage phase (Fig. 6(a)), the gate voltage of transistor M_1 is set and the stimulus current is then steered to the electrode in the stimulation phase (Fig. 6(b)). By using this approach, the power needed in the biasing branch is small, since it is not always on as compared to common current mirror. Also, since the DAC is not required per output driver all the time, it can be shared within a group of current drivers or the whole stimulator. This reduces the area consumption of the stimulator.

Nonetheless, the headroom voltage is still high (700mV at 250μA) due to the biasing transistor is operated in saturation region.

IV. HIGH POWER EFFICIENT STIMULATOR

By combining a symmetrical regulated cascode current driver with a current-copying stimulator, a power efficient, high voltage-compliance output stage is presented in Fig. 7 [7]. In order to explain the operation, only the cathodic driver is shown in this paper. The operation is separated into two phases. During storage phase (Φ_1), the circuit is configured as the left-half (biasing) of the symmetrical regulated cascode in Fig. 5 with additional storage capacitor (which can also be just the C_{gs} of transistor M_1). The storage capacitor C_{MEM} is charged to store the gate voltage of transistor M_1 corresponding to the DAC current. Moreover, the drain voltage of transistor M_1 is regulated to the bias voltage V_{DN}. In stimulation phase (Φ_2), the circuit is configured as in the right-half (output) of Fig. 5. The capacitor voltage sets the stimulus current and the amplifier loop regulates the drain voltage of transistor M_1 and the gate voltage of the output transistor M_3 is adjusted accordingly. Besides, the maximum stimulus current depends on the dimension of M_1 and the bias voltage V_{DN}.

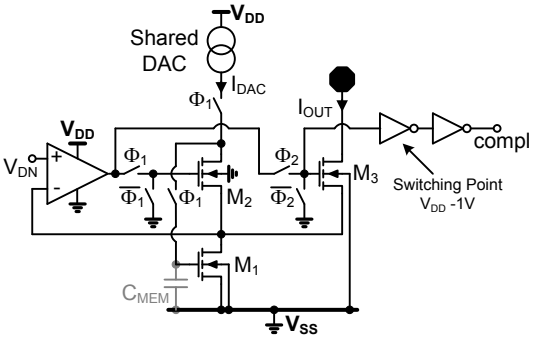

Fig. 7. Switched symmetrical regulated cascode stimulator with a compliance monitor.

The advantages of this stimulator are fourfold. First, since there is no need to concern about current mismatch, the biasing voltage V_{DN} can be small which increases the voltage-compliance. Second, the unused power in biasing branch is almost eliminated. Third, the area is also decreased because the DAC can be reused. Finally, the structure still allows the simple realization of the compliance monitor.

V. SIMULATION RESULTS

The cathodic output current driver in Fig. 7 was verified using a 0.35μm CMOS technology. The amplifier was a single-stage amplifier with 1μA biasing current. The supply voltage V_{DD} was set to 3.3V. The transistor M_1 was designed to deliver a maximum current of 500μA. The biasing voltage

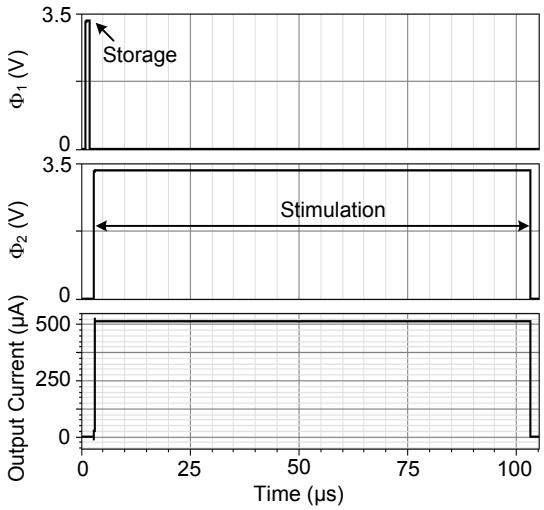

Fig. 8. Transient operation of the proposed current driver.

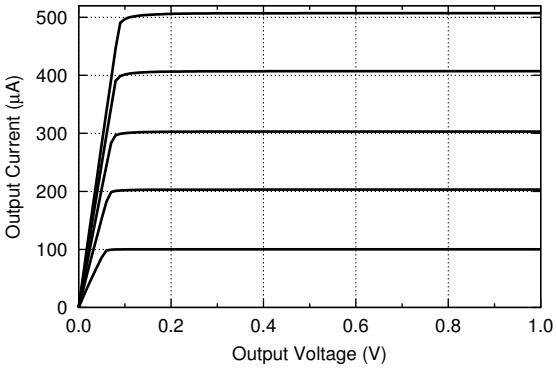

Fig. 9. Output characteristic.

V_{DN} was 50mV and the cascoding output transistor was designed to have V_{DSsat} of around 50mV at 500μA stimulus current. The storage capacitor C_{MEM} was exemplarily chosen as a 150fF poly capacitor.

Fig. 8 depicts the storage and stimulation phases of the current driver. The storage and stimulation times were set to 1μs and 100μs, respectively. The driver was adjusted to deliver 500μA current to a 10kΩ load.

The output characteristic is illustrated in Fig. 9. It is obviously seen that at 500μA stimulus current this current driver needs only 100mV headroom voltage while the output impedance is approximately 50MΩ.

Finally, a comparison of recent high compliance current drivers and this work is shown in Table I.

VI. CONCLUSIONS

An overview of power efficient current drivers for implantable stimulators is presented in this paper. In order to improve power efficiency of current driver in stimulator, the headroom voltage needs to be as small as possible since this is not functionally needed. A promising technique is to bias the transistors in triode region. Whereas, the output impedance is high through the active feedback. The power consumption of biasing branch is nearly omitted by current copying approach. Finally, an adaptive power supply with a feedback signal from compliance monitor, the power is best controlled to the right value.

TABLE I

COMPARISON OF HIGH COMPLIANCE CURRENT DRIVERS

	I_{Max}	V_{HR}	r_{out}	Power
[9]	216μA	500mV	n/a	n/a
[10]	600μA	500mV	n/a	500μW
[11]	94.5μA	300mV	1GΩ*	45μW
[2]	210μA	750mV	18.8MΩ*	43μW*
[12]	1mA	400mV	100MΩ*	n/a
[4], [5]	1mA	300mV	$>$10MΩ	136μW*
[6]	250μA	700mV	n/a	2.76μW
This paper*	500μA	100mV	50MΩ	4.5μW

*Simulated results

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