34th Annual International Conference of the IEEE EMBS
San Diego, California USA, 28 August - 1 September, 2012

Animal Experiments with the Microelectronics Neural Bridge IC

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***Abstract*—The combination of the neural science and the microelectronics science offers a new way to restore the function of central nervous system. A neural regeneration module is used to be implanted into body to bridge the damaged nerve. A microelectronics neural bridge IC designed in CSMC 0.5□m CMOS process which can detect the neural signal and stimulate the nerve is presented. The neural regeneration module is composed of the microelectronics neural bridge IC and some discrete devices. An animal experiment has been done to check whether the neural signal can be transmitted with the chip normally or not. The animal experiment results suggest that the neural regeneration module can make the neural signal transmit normally.**

Keywords: neural signal; CMOS; IC; neural regeneration module; animal experiment

I INTRODUCTION

Neural injury and regeneration has been an important topic in neuroscience research. The traditional biology and medical technology employs the surgery and physical training methods generally. Although it has some effect, it is still not can be used in practical applications. Extensive attention has been held by the neural regeneration method which is based on bio-electricity phenomenon [1~3].

The neural regeneration module, which is combined with the advanced research results in modern microelectronics technology and neural science, has significant value for the research of neural science and neural regeneration [4~5].

II MICROELECTRONICS BRIDGE IC

The neural signal spectrum concentrates in low frequency band from 400 Hz to 4 kHz, and CMOS device's 1/f noise in this band is very high. So, the microelectronics neural bridge IC should have good noise performance.

There is a DC offset voltage as high as 1~2 V between the neural signal detecting microelectrodes and neural interface. At the same time, there is strong disturbed myoelectric signal and biological background noise in organism. So, the microelectronics neural bridge IC should have high common mode rejection ratio (CMRR). System diagram of the IC is shown in Fig. 1.

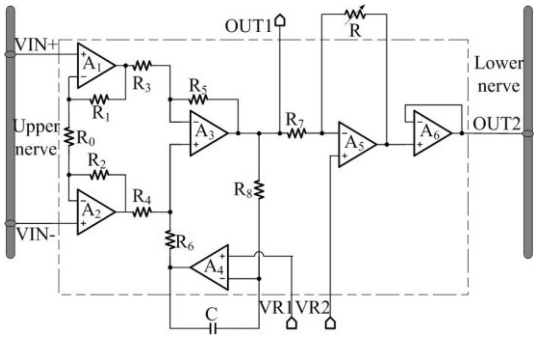

FIG.1 SYSTEM DIAGRAM OF THE MICROELECTRONICS NEURAL BRIDGE IC

As shown in Fig. 1, inside of the box is the microelectronics neural bridge IC, and outside of the box are off-chip components, output ports, input ports, signal sources and reference voltages.

The microelectronics neural bridge IC is composed of the neural signal detecting circuit, the signal amplifying circuit, the DC offset compensating circuit and the functional electrical stimulation circuit.

In order to satisfy the requirement of the high CMRR, the neural signal detecting circuit is designed with the structure of 3-op-amp in-amp [6]. The neural signal detecting circuit is composed of the op-amps A_1, A_2, A_3 and the resistors R_0~R_6. Setting $R_1 = R_2$, $R_3 = R_4$, $R_5 = R_6$, the gain of the neural signal detecting circuit A_{v1} is given by:

$$A_{v1} = \left(1 + 2R_1 / R_0\right)\left(R_5 / R_3\right) \tag{1}$$

The signal amplifying circuit is designed with the structure of op-amp scaling circuit and is composed of the op-amp A_5 and the resistors R and R_7. The variable resistor R is an off-chip component which is used to adjust the gain of the IC. The gain of the signal amplifying circuit A_{v2} is given by:

$$A_{v2} = R / R_7 \tag{2}$$

The DC offset compensating circuit is composed of the op-amp A_4, the resistor R_8 and the capacitor C. The capacitor

Supported by National Science Foundation of China (Grant Nos. 61076118), Special Foundation and Open Foundation of State Key Laboratory of Bioelectronics of Southeast University, Nanjing, China

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C (33nF) is an off-chip component which is used to adjust the -3dB cut-off frequency.

The functional electrical stimulation circuit is designed in the structure of unit-gain buffer circuit and is composed of the op-amp A_6.

The system gain of the microelectronics neural bridge IC A_V is given by:

$$A_v = A_{v1}A_{v2} = (1+2R_1/R_0)(R_5/R_3)(R/R_7) \quad (3)$$

In the microelectronics neural bridge IC, two high performance op-amps are designed including low noise op-amp (A1, A2, A3, A4 in Fig.1) and constant-g_m rail-to-rail input/output op-amp (A5, A6 in Fig.1).The details of them are shown in Fig.2 and Fig.3.

The schematic of low noise op-amp is shown in Fig. 2 [7~8].

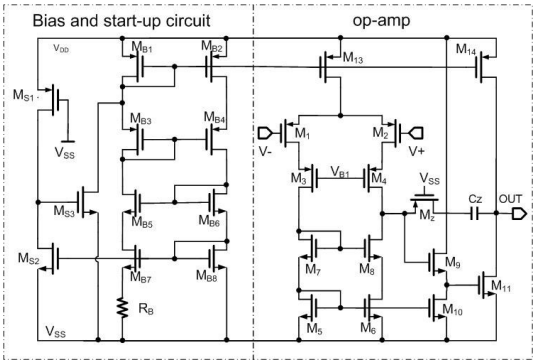

FIG. 2 SCHEMATIC OF LOW NOISE OP-AMP

The left part of Fig. 2 is the start-up circuit and the bias circuit of the low noise op-amp. The right part of Fig. 2 is 2-stage telescopic op-amp.

The schematic of the constant-g_m rail-to-rail input/output op-amp is shown in Fig. 3 [9~10].

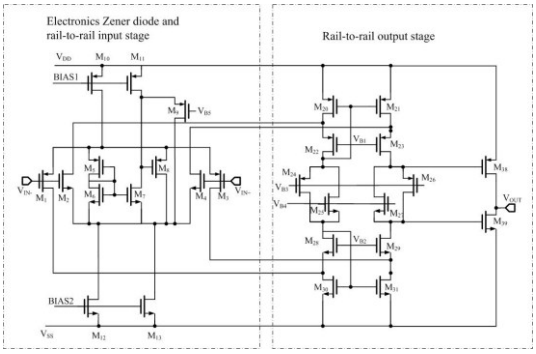

FIG. 3 SCHEMATIC OF CONSTANT-GM RAIL-TO-RAIL INPUT/OUTPUT OP-AMP

In order to meet the requirement of rail-to-rail input, NMOS differential pair and PMOS differential pair are connected in parallel as the differential input stage.

In order to make rail-to-rail input op-amp's g_m constant, an electronic zener diode is used in the op-amp. As shown in Fig. 3, the electronic zener diode is composed of the transistors M_5~M_8.

In order to meet the requirement of rail-to-rail output, the AB mode complementary structure is employed as the output stage.

The layout of the microelectronics neural bridge IC is shown in Fig. 4. The area of the layout is 1050□m×850□m.

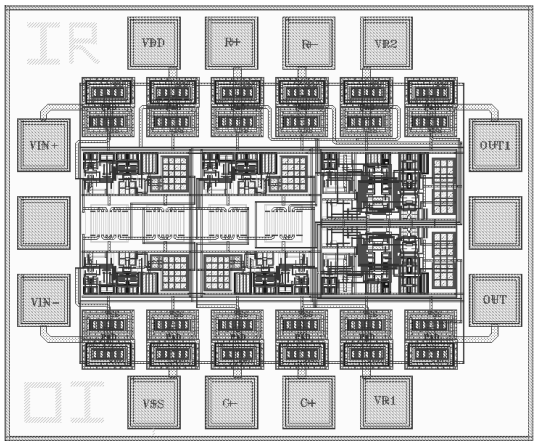

FIG. 4 IC LAYOUT

The microelectronics neural bridge IC is simulated with the tool of Spectre. The post-simulation results of the microelectronics neural bridge IC are shown in TABLE 1 and TABLE 2.

TABLE 1 POST-SIMULATION RESULTS OF LOW NOISE OPAMP

Parameter	***Post-simulation***
Open Loop Gain	104.9 dB
GBW	6.98 MHz
Phase Margin (The Load Capacitor Equals 5pF)	82.1 º
Integrated Noise in the Band of 0.1 Hz~50 kHz	3.29e-10 V^2
The Range of the CM Input Voltage	-1.24V~1.8 V
PSRR+	-119.5 dB
PSRR-	-103.98 dB
CMRR	-124.6 dB
DC power consumption	0.613 mW

TABLE 2 POST-SIMULATION RESULTS OF CONSTANT-GM RAIL-TO-RAIL INPUT/OUTPUT OP-AMP

Parameter	***Post-simulation***
Open Loop Gain	110 dB
GBW	5.437 MHz
Phase Margin (The Load Capacitor Equals 5pF)	81.15 º
Integrated Noise in the Band of 0.1 Hz~50 kHz	8.128e-9 V^2
The Range of the CM Input Voltage	-2.5 V~2.5 V
PSRR+	-120.6 dB
PSRR-	-139.7 dB
CMRR	-116.6 dB
DC power consumption	0.984 mW
The rate of change of g_m	4.7 %

The simulation results suggest that the CMRR of the microelectronics neural bridge IC is 145dB, and the DC power consumption is 4.57mW when the supply voltage is ±2.5V.

III NEURAL REGENERATION MODULE

When the chip is taped out, an electrical test is needed to check whether the chip works properly or not. The diagram of the chip'pads is shown in Fig. 5.

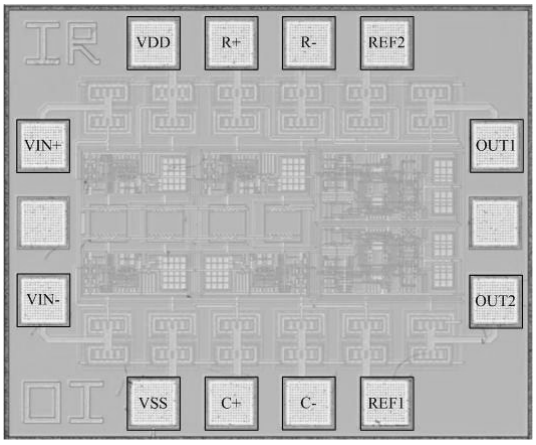

FIG. 5 THE DIAGRAM OF THE CHIP' PADS

As shown in Fig. 5, the pad VDD is the positive supply voltage port, the pad VSS is the negative supply voltage port, the pads R+ and R- are the adjustable resistor ports, the pad C+ and C- are the adjustable capacitor ports, the pads VIN+ and VIN- are input ports, the pads REF1 and REF2 are reference voltage input ports which are used to adjust the DC offset, the pad OUT1 is the output port of the neural signal detecting circuit, the pad OUT2 is the output port of the chip.

For the input signal amplitude of 1 mV, frequency of 1 kHz sinusoidal wave, the waveforms of the output signal is shown in Fig. 6.The abscissa axis is time，and the vertical axis is voltage.

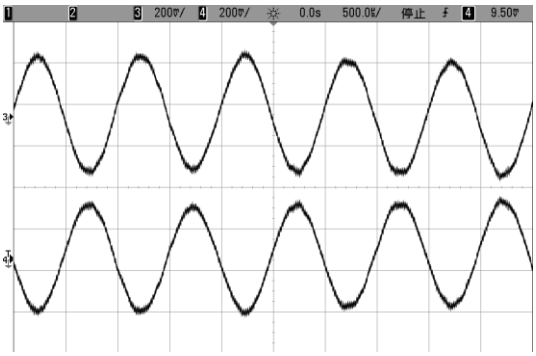

FIG. 6 THE OUTPUT SIGNAL FOR THE INPUT SIGNAL AMPLITUDE OF 1 MV, FREQUENCY OF 1 KHZ SINUSOIDAL WAVE

The electrical testing results suggest that the chip can amplify low frequency weak signals normally. The neural regeneration module is composed of the microelectronics neural bridge IC and some discrete devices. The diagram of the neural regeneration module is shown in Fig. 7.

As shown in Fig. 7, the high-pass filter is used to filter out interfering signal in low frequency. The resistor R is adjustable and is used to adjust the gain of the chip. The value of the capacitor C is set to be 33nF and the -3dB cut-off frequency of the DC offset compensating circuit is 100Hz. According to the electrical testing results, the DC offset of the chip is extremely low, so the reference voltage ports are connected to the ground.

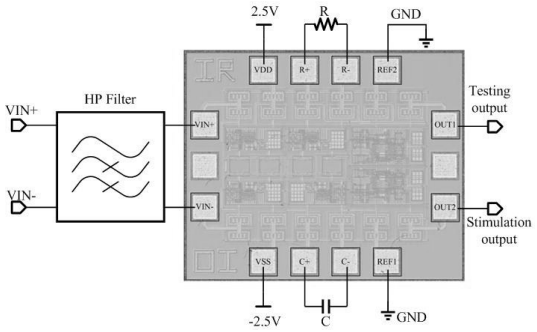

FIG. 7 THE DIAGRAM OF THE NEURAL REGENERATION MODULE

The photo of the neural regeneration module is shown in Fig. 8. Compared with the coin placed at the right side, the testing board is indeed small.

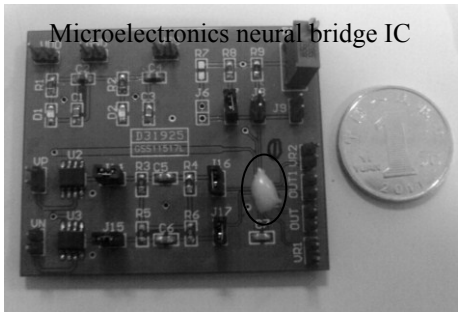

FIG. 8 THE PHOTO OF THE NEURAL REGENERATION MODULE

IV ANIMAL EXPERIMENT

Because the neural signal is more complex than the sinusoidal wave, the well electrical testing results don't mean that the chip can be used to bridge the damaged nerve. So, the animal experiment is needed to check whether the neural signal can be transmitted with the chip normally or not.

In the animal experiment, the neural regeneration module is connected to the source toad and the controlled toad by the cuff type electrodes and the ancistroid electrodes [11]. The neural regeneration module is used to detect the action potential signal from the source toad and stimulate the sciatic nerve of the controlled toad. If the controlled animal acts as well as the source toad, that suggests that the neural regeneration module can detect the neural signal and stimulate the nerve normally; and if not, the neural regeneration module can't be used to bridge the damaged the nerve [12].

The followings are the procedures of the animal experiment:

1) Debug the neural regeneration module, and adjust the gain of the chip to be 7000.

2) Make the source toad. Cut out the head of the source toad.

3) Make the controlled toad. Cut out the head of the controlled toad, and damage the spinal cord of the controlled toad to cut off the reflex arc.

4) Sort out the sciatic nerve of the source toad, and connect with cuff type electrodes.

5) Sort out the sciatic nerve of the controlled toad, and connect with ancistroid electrodes.

6) Connect the cuff type electrodes to the input ports of the neural regeneration module.

7) Connect the ancistroid electrodes to the output ports of the neural regeneration module.

8) Drip the 5% acetum to the left hind leg of the source toad, and observe the reactions of the source toad and the controlled toad.

Photo of the animal experiment is shown in Fig. 9.

FIG. 9 PHOTO OF THE ANIMAL EXPERIMENT

The animal experiment phenomenon is: when the source toad is stimulated by the 5% acetum, it pulls its left hind leg; at the same time, the controlled toad pulls its left hind leg.

When the gain of the chip is 7000 decided by the effect of stimulation in animal experiment, the peak-to-peak value of the output voltage is 1V approximately. The action potential signal detected in animal experiment is shown in Fig. 10. The abscissa axis is time，and the vertical axis is voltage.

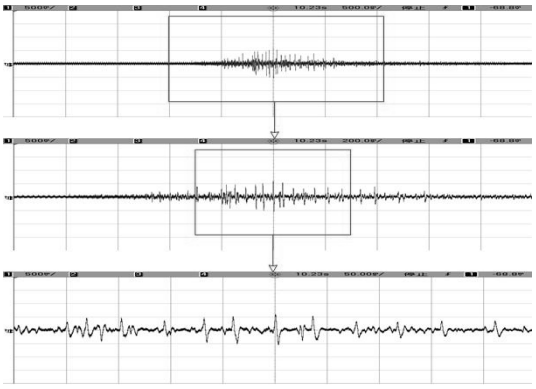

FIG. 10 THE ACTION POTENTIAL SIGNAL DETECTED IN ANIMAL EXPERIMENT

The upper part in Fig.10 is the action potential signal detected. The intermediate section is the enlargement of the above one. The third one is also the enlargement of the intermediate one. The animal experiment results suggest that the chip can detect the action potential signal and can stimulate the sciatic nerve. So the chip can be used to bridge the damaged nerve and can transmit the neural signal normally.

CONCLUSION

A neural regeneration module is designed which is composed of the microelectronics neural bridge IC and some discrete devices. The chip is designed in CSMC 0.5□m CMOS process. The neural regeneration module is used in animal experiment. The animal experiment results suggest that the microelectronics neural bridge IC can be used to bridge the damaged nerve.

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