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A 1.5-to-5 V Converter for a Battery-Powered Activity-Dependent Intracortical Microstimulation SoC

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Abstract-**This paper reports on the design, analysis, implementation, and testing of a 1.5-to-5 V converter as part of a battery-powered activity-dependent intracortical microstimulation (ICMS) system-on-chip (SoC) that converts extracellular neural spikes recorded from one cortical area to electrical stimuli delivered to another cortical area in real time. The highly integrated voltage converter is intended to generate a 5-V supply for the stimulating back-end on the SoC from a miniature primary battery that powers the entire system. It is implemented in AMS 0.35 µm two-poly four-metal (2P/4M) complementary metal-oxide-semiconductor (CMOS) technology, employs only one external capacitor (1 µF) for storage, and delivers a maximum dc load current of ~88 µA with power efficiency of 31% with its output voltage adjusted to 5.05 V. This current drive capability affords simultaneous stimulation on all eight channels of the SoC with current amplitude up to ~100 µA and average stimulus rate >500 Hz, which is comfortably higher than firing rate of cortical neurons (<150 spikes per second). The measurement results also agree favorably with theoretical derivations from the analysis of converter operation.**

I. Introduction

New design methodologies in application-specific integrated circuit (ASIC) development have fueled the recent increase in the number of devices that bidirectionally interface with the nervous system in awake, behaving subjects for neuroscience and neuroengineering applications. These neural interface devices typically incorporate low-power, low-voltage circuitry for low-noise recording and real-time processing of neural signals, high-voltage circuitry for efficient microstimulation of the nervous system, and communication circuitry for bidirectional data telemetry. Depending on their application, they can be powered via a continuous, radio-frequency (RF) inductive link [1], an RF-rechargeable secondary battery [2], or a miniature primary battery [3].

Low power supplies are typically desirable for neural recording and signal processing functionalities to reduce the power consumption and benefit from technology scaling. On the other hand, higher voltage levels are generally required in neurostimulation for increased voltage compliance (depending on stimulus intensity and electrode-tissue interface impedance) as well as for enabling new stimulation modalities such as exponential stimulus current waveforms and optogenetics [4], [5]. While such higher voltage levels can be directly generated in inductively powered systems by rectification and regulation of the sinusoidal carrier received at the secondary, they need to be generated by means of voltage-conversion circuitry in battery-operated systems, especially when neural recording, signal processing, and microstimulation functionalities are combined in a single device with autonomous operation. In this paper, we report on the design, analysis, implementation, and testing of an integrated 1.5-to-5 V converter as part of a larger system-on-chip (SoC) for activity-dependent intracortical microstimulation (ICMS) [3]. The circuit has been implemented in AMS 0.35 µm two-poly four-metal (2P/4M) complementary metal-oxide-semiconductor (CMOS) technology and enables simultaneous, multichannel, constant-current stimulation at average stimulus rates that comfortably exceed maximum cortical neuronal firing rates.

II. Activity-Dependent ICMS SoC Architecture

Figure 1 depicts the block diagram and a die micrograph of the activity-dependent ICMS SoC that has been previously developed. The system and transistor-level circuit architectures as well as performance characterization during electrical benchtop measurements and biological experiments with anesthetized rats were thoroughly described in [3].

Briefly, the system consists of two identical four-channel modules per chip, each incorporating a recording front-end, digital signal processing (DSP) unit, and stimulating back-end. It is capable of recording extracellular neural spikes from one cortical region and delivering neurally-triggered ICMS sequences to a distant cortical region in real time. Spike discrimination is performed on-the-fly using the on-chip DSP unit based on thresholding and two user-adjustable time-amplitude windows [3]. The decision circuitry can generate any logic combination of the four spike discriminator outputs (SDO) as a trigger signal for stimulation activation. The back-end circuitry can be programmed to stimulate the target cortical tissue with an asymmetric biphasic as well as a monophasic current waveform, with passive discharge performed after each stimulation cycle. The anodic and cathodic current pulse amplitudes are programmable from 0 to 94.5 µA and 31.5 µA, respectively, with 6b resolution (i.e., LSB of 1.5 µA). Given a typical site impedance of ~50-60 kΩ for our stimulating microelectrode, a 1.5-to-5 V converter is also designed to generate a power supply of ~5 V from a 1.55-V battery for the stimulating back-end of the two modules, increasing the available voltage headroom for stimulation.

The voltage converter should be highly integrated with minimum number of external components and with adequate current drive capability to ideally support

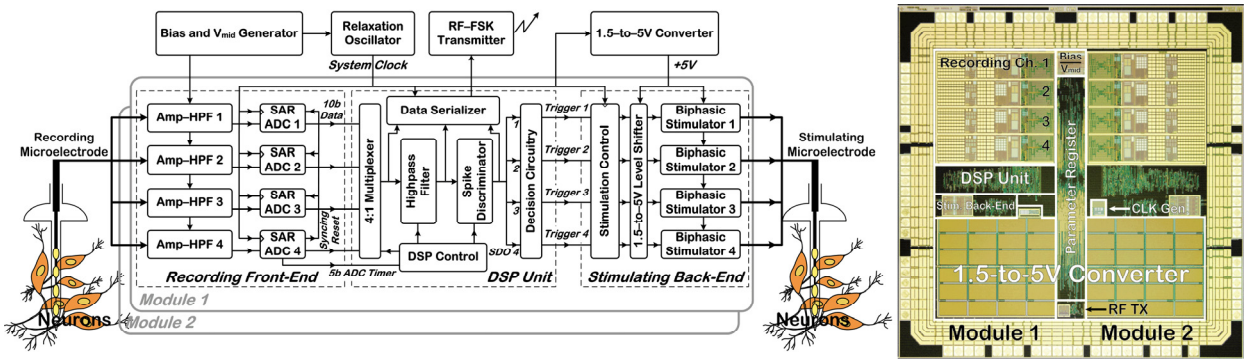

Fig. 1. Block diagram and a die micrograph of the 3.3 × 3.3-mm^2 SoC for activity-dependent ICMS [3].

simultaneous stimulation on all eight channels of the SoC with maximum available current and at stimulus rates that are determined by cortical neuronal firing rates (<150 spikes per second [6]). At the system level, the requirement on the converter power efficiency is rather relaxed, since the total SoC power consumption is highly dominated by that of the analog recording front-end circuitry (42% *vs.* 7% for the stimulating back-end) [3]. Similarly, employing cascode structures and active feedback circuitry in the design of the stimulating current sources and associated biasing circuitry to boost their output impedance has largely reduced the supply sensitivity in the stimulating back-end (maximum of 70.4 nA/V) [3], requiring the converter output voltage ripple to be e.g. <140 mV_{pp} to stabilize the stimulator output current within ±5 nA.

III. 1.5-to-5 V Converter Architecture

Figure 2 shows the circuit schematic of the 1.5-to-5 V converter. While a voltage doubler and tripler with similar circuit architectures have been previously reported [7], [8], the converter in this work comprises eight voltage-multiplier modules, providing an output voltage up to ~4 × V_{DD} to a 1-μF external capacitor for storage. Each voltage multiplier incorporates a symmetric charge pump, operating with two non-overlapping clock signals, $\phi_{1,2}$. When ϕ_1 is low (and ϕ_2 is high), the three bucket capacitors, C_b, in the left half of the charge pump are charged up to V_{DD}, whereas the three capacitors in the right-half circuit are stacked up to pump their accumulated charge to the output load. The charge pump operation is then reversed when ϕ_1 is high (and ϕ_2 is low). Using non-overlapping clock signals prevents charge leakage from the bucket capacitors to the power supply, which can cause an output voltage drop and significantly degrade charge pump efficiency. An output stage is added to the charge pump in each module to generate a rectified output voltage for storage on the external capacitor. A Schmitt trigger comparator with 3b user-adjustable threshold regulates the converter output voltage between predefined levels by switching the charge pumps on and off. The voltage-multiplier modules are clocked *sequentially* to reduce the output voltage ripple [8]. This can also reduce the transient peak current drain from the power supply, leading to less power supply noise affecting the operation of the sensitive neural-recording front-end circuitry in the SoC. To analyze the charge pump operation in further detail, two simplified equivalent circuits for *charge-up* and *stack-up* phases are shown in Fig. 3(a) and (b), respectively. The right-half circuit is omitted for simplicity given the symmetric structure of the charge pump. Excluding the feedback loop for output voltage adjustment (i.e., assume the *Enable* signal is always high regardless of V_{out} value), the converter circuit can be simplified to an equivalent circuit shown in Fig. 3(c) [9]. When the charge pumps are in steady state and there is no dc current load, V_{out} reaches its maximum value of V_{NL} that can ideally be as high as 4 × V_{DD}. In practice, however, it is always less than that due to parasitic capacitors. The parasitic stray capacitor, C_p, between the bottom plate of the bucket capacitors and the substrate is typically much larger than other parasitic capacitors in the circuit and the dominant factor in determining V_{NL} and charge pump efficiency. When there is no load at the output node, V_{NL} can be determined by writing charge-distribution equations at V_1 and V_3 in Fig. 3(b):

$$V_{NL} = V_5 = \frac{4 + 4\times\alpha + \alpha^2}{1 + 3\times\alpha + \alpha^2} \times V_{DD} \qquad (1)$$

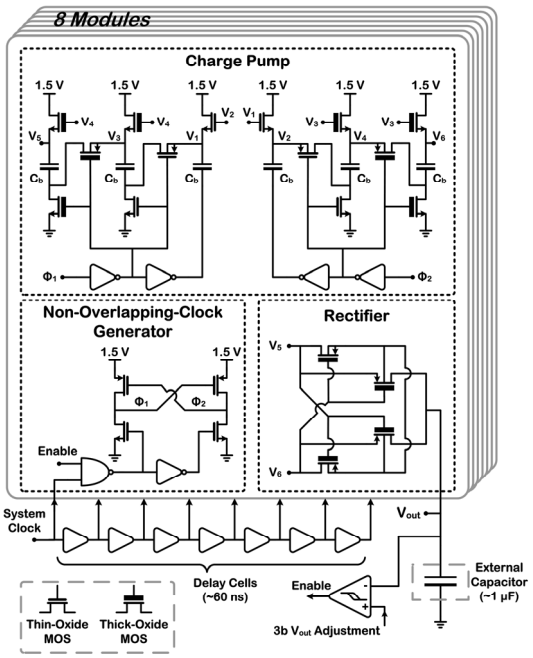

Fig. 2. Circuit schematic of the 1.5-to-5 V converter with eight voltage-multiplier modules clocked sequentially at a nominal rate of 1 MHz.

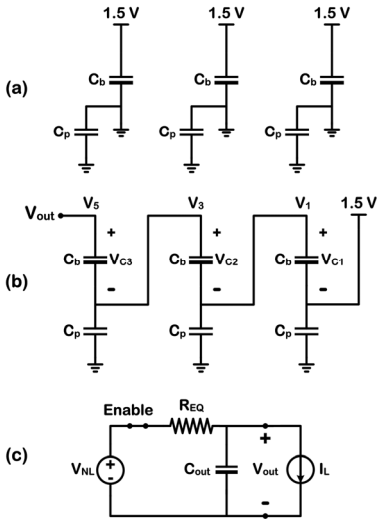

Fig. 3. Simplified equivalent circuits for charge pump operation in a) *charge-up* and b) *stack-up* phases. c) Simplified equivalent circuit for the voltage converter, assuming that the *Enable* signal is always high.

where $\alpha = \frac{C_p}{C_b}$. Given that there are 16 half-circuits in the converter, it can be shown that [9]:

$$V_{out} = V_{NL} - R_{eq} \times I_L$$
$$R_{eq} \cong \frac{3}{16} \times \frac{1}{f \times C_b} \quad (2)$$

where f is the charge pump clock frequency. Charge pump transistors should be sized judiciously so that they can fully charge up the bucket capacitors in one half of the clock cycle; otherwise R_{eq} would be larger than that estimated in (2). The power efficiency of the converter, η, can be expressed as:

$$\eta = \frac{E_{out}}{E_{in}} = \frac{V_{out} \times Q_{out}}{V_{DD} \times Q_{in}} \quad (3)$$

where Q_{in} is the total charge drained from the power supply in one clock cycle and Q_{out} is the total charge given to the load as expressed below:

$$Q_{in} = Q_{Charge-up} + Q_{Stack-up}$$
$$Q_{out} = \frac{I_L}{f} = \frac{V_{NL} - V_{out}}{f \times R_{eq}} \quad (4)$$

where $Q_{Charge-up}$ and $Q_{Stack-up}$ refer to total charges drained from the power supply during the *charge-up* and *stack-up* phases, respectively. Given that there are 16 half-circuits in the converter, it can be shown that:

$$Q_{Charge-up} = 16 \times C_b \times (3 \times V_{DD} - (V_{C1} + V_{C2} + V_{C3}))$$
$$Q_{Stack-up} = 16 \times C_b \times (2 \times V_{DD} - V_1) + 16 \times \alpha \times C_b \times V_{DD} \quad (5)$$

where V_C is the voltage across the bucket capacitors at the end of the *stack-up* phase. It is clear from Fig. 3(b) that $V_{C1} + V_{C2} + V_{C3} = V_{out} - V_{DD}$. Also, if $\alpha << 1$, it can be shown that:

$$V_1 \cong \frac{2}{3} \times V_{DD} + \frac{1}{3} \times V_{out}. \quad (6)$$

Combining all the above equations, the converter power efficiency can be expressed as:

$$\eta \cong \frac{V_{out} \times (V_{NL} - V_{out})}{4 \times V_{DD} \times (4 \times V_{DD} - V_{out})}. \quad (7)$$

Equations (1) and (7) suggest that α should be minimized to maximize V_{NL} and η. To that end, the bucket capacitors are realized by a poly-insulator-poly (PiP) capacitor with a metal insulator-metal (MiM) interdigitated capacitor on top of it. Using the MiM capacitor also increases the bucket capacitor density and reduces the required silicon area to realize the converter. The stray capacitor C_P is further reduced by placing a floating n-well underneath the PiP structure. Given our design geometry and process parameters, C_b and α are estimated to be 45 pF and 0.055, respectively, resulting in a value of ~5.42 V for V_{NL}. As stated previously, the feedback loop turns the charge pumps on and off to maintain the output voltage between two predefined levels. With no load current, the charge pumps remain off for a long period of time. As I_L increases, the charge pumps turn on more frequently and when I_L exceeds $\frac{V_{NL} - V_{out}}{R_{eq}}$ they stay on continuously with V_{out} decreasing below its adjusted value. For simplicity, this analysis excluded the feedback control loop to adjust the output voltage level. However, the converter power efficiency can still be estimated by (7), because no significant extra power is dissipated in the converter by adding the feedback control loop. For an output voltage of 5 V, the converter power efficiency is then estimated to be 35.3%.

IV. Measurement Results

The activity-dependent ICMS SoC was fabricated in a 0.35-μm 2P/4M CMOS technology, measuring 3.3 mm × 3.3 mm including the bonding pads. Figure 4 depicts the measured transient and steady-state output voltage of the 1.5-to-5 V converter with an external capacitor of 1 μF when delivering a dc load current of 10 μA. It took ~7.4 ms for the output voltage to reach 90% of its adjusted value of 5.05 V. In steady state, a ripple of 40 mV_{pp} was present on the output voltage due to the hysteresis of the Schmitt trigger comparator in the feedback control loop, which could adjust the output voltage between 5.35 and 4.86 V in steps of approximately 100 mV. Figure 5 depicts the converter dc output current, I_L, and its power efficiency, η, measured *vs.* the output voltage as well as the corresponding theoretical relationships derived in (2) and (7), respectively. With V_{out} adjusted to 5.05 V, the converter could provide a maximum I_L of ~88 μA with η of 31%. The measured V_{NL} of 5.35 V was slightly below its estimated value of 5.42 V from (1). This is because our simplified analysis does not account for charge-leakage paths from the bucket capacitors, especially if the clock signals $\phi_{1,2}$ slightly overlap in time. Further, as seen in Fig. 5(a), when V_{out} decreased below ~4.7 V, the measured R_{eq} started to increase compared to its theoretical value. This is because as V_{out} decreases all internal voltages of the charge pump ($V_{1\text{-}6}$)

decrease too, causing a drop in the overdrive voltage of the nMOS transistors, which charge up the bucket capacitors. With the capacitors not fully charged up, equation (2) underestimates the value of R_{eq}.

The core area of the activity-dependent ICMS SoC, including both modules and excluding input-output (I/O) pads, measured 2.6 mm × 2.6 mm [3]. The 1.5-to-5 V converter occupied 34% of the silicon area, making it the largest circuit block in the SoC followed by the analog recording front-end circuitry at 26%. According to [3], the stimulating back-end dissipated 3.5 µW per channel from 5 V when delivering a biphasic stimulus current (anodic: 94.5 µA, 192 µs – cathodic: 31.5 µA, 576 µs) at a rate of 33 Hz. Given that the converter could provide a maximum dc output current, I_L, of ~88 µA with V_{out} adjusted to 5.05 V, it is capable of supporting such biphasic stimulation on all eight channels of the SoC at average stimulus rates >500 Hz. Given cortical neuronal firing rates of <150 spikes per second [6], the same converter architecture can support activity-dependent ICMS on an even higher number of channels. Alternatively, the number of voltage-multiplier modules in the converter can be reduced to three, if silicon area is of major concern. The area can be further reduced by increasing the operation frequency beyond 1 MHz. Further, the converter power efficiency can be slightly improved with an enhanced Dickson topology [10].

V. Conclusion

This paper presented an integrated voltage converter to generate a 5-V supply from a miniature battery (1.55 V) for the stimulating back-end on an activity-dependent ICMS SoC. The circuit architecture employs eight voltage-multiplier modules, incorporating a symmetric, 3-stage, capacitive charge pump and associated circuitry, which are clocked sequentially at a nominal rate of 1 MHz. The converter regulates its output voltage from 4.86 to 5.35 V with 3b resolution and delivers a maximum dc load current of 88 µA with its output voltage adjusted to 5.05 V. This current drive capability comfortably affords simultaneous, multichannel ICMS with current amplitudes <100 µA at average stimulus rates determined by cortical neuronal firing rates.

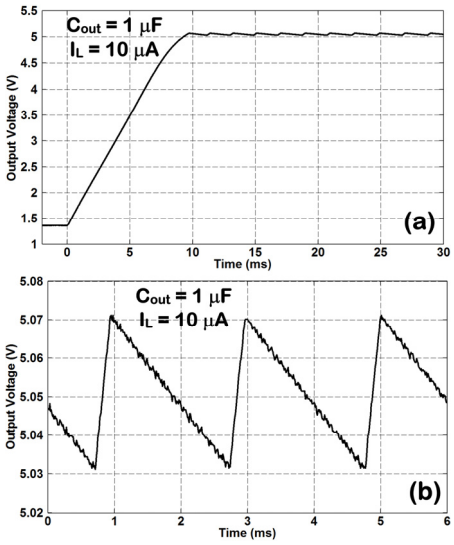

Fig. 4. Measured a) transient and b) steady-state output voltage of the 1.5-to-5 V converter with a 1-µF external storage capacitor when delivering a dc load current of 10 µA.

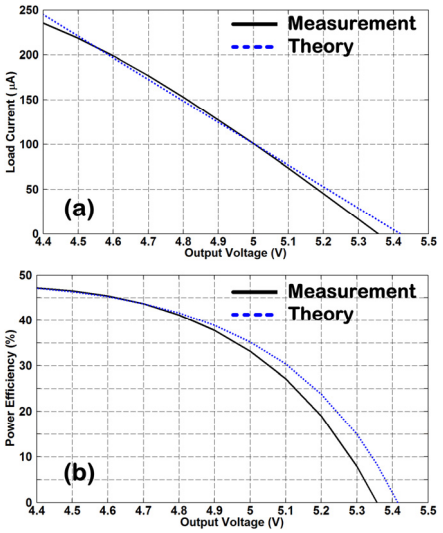

Fig. 5. Measured a) load current and b) power efficiency of the converter versus the output voltage, which is initially adjusted to 5.35 V. The corresponding theoretical relationships are also plotted in dashed lines.

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