34th Annual International Conference of the IEEE EMBS
San Diego, California USA, 28 August - 1 September, 2012

Event-driven Neural Integration and Synchronicity in Analog VLSI

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***Abstract*— Synchrony and temporal coding in the central nervous system, as the source of local field potentials and complex neural dynamics, arises from precise timing relationships between spike action population events across neuronal assemblies. Recently it has been shown that coincidence detection based on spike event timing also presents a robust neural code invariant to additive incoherent noise from desynchronized and unrelated inputs. We present spike-based coincidence detection using integrate-and-fire neural membrane dynamics along with pooled conductance-based synaptic dynamics in a hierarchical address-event architecture. Within this architecture, we encode each synaptic event with parameters that govern synaptic connectivity, synaptic strength, and axonal delay with additional global configurable parameters that govern neural and synaptic temporal dynamics. Spike-based coincidence detection is observed and analyzed in measurements on a log-domain analog VLSI implementation of the integrate-and-fire neuron and conductance-based synapse dynamics.**

I. Introduction

Recent research efforts at the intersection between computational neuroscience and neuromorphic engineering are pursuing very large-scale spike-based cortical neural systems in silicon as a means to studying synchronous neural and synaptic dynamics underlying neural information processing [1]–[4]. One approach [5] uses spike rate-based algorithms to perform various computations. This approach relies upon the readily accessible spike rate statistics as a measure of spike activity. Another approach [6] seeks to exploit the efficiency of spike-based computation. This approach emphasizes that each individual spike carries information that either creates, corroborates or corrects previous information. Some implementations of spike-based computation perform spike-timing dependent plasticity (STDP) [7], [8] to utilize the relative spike timing between associated presynaptic and postsynaptic events to determine the change in the synaptic connection strength. STDP is used to describe how the synaptic connections in a network of spiking neurons evolve over time. Another implementation of spike-based computation recognizes that the coincidence of two or more synaptic events upon the postsynaptic membrane results in the activation of a subsequent neural event [9]. Through a multilayered and interwoven construction of neurons computing this coincidence detection of incoming synaptic events, the neural network can implement an arbitrary function dependent upon the synaptic connectivity, synaptic strength, and axonal delay between neuron elements.

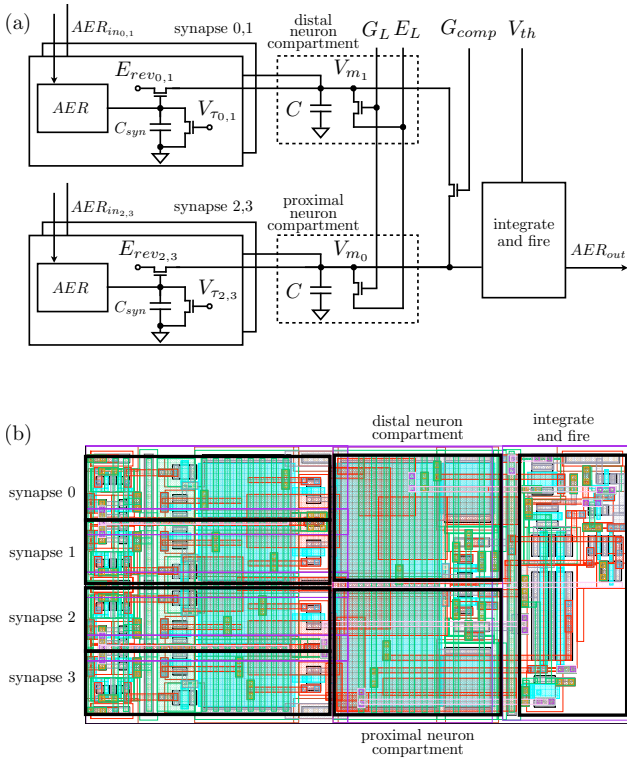

Fig. 1. (a) Detailed system block diagram of an individual neuron cell with neural spike generation and spike registration circuits [13], [14], address-event routing (AER) translinear synaptic activation circuits [12], and synaptic, leakage, and compartment coupling translinear conductances [18]. (b) VLSI layout showing labelled block components.

Here we present a spike event-based neuromorphic architecture for synchrony in neural computation by coincidence detection of synchronously converging presynaptic action potentials. To this end, we have developed the hierarchical address-event routing integrate-and-fire transceiver (HiAER-IFAT) system as described and introduced in [10] for scaleable, generalized, neural spike-based computation. We present results of synchronous neural detection illustrating the configurability of neural and synaptic dynamics for one neuron in the analog integrate-and-fire array transceiver

This work was supported by NIH/NIA, DARPA NeoVision2, Evolved Machines, and Qualcomm, and Texas Instruments

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(IFAT). Specifically, we show measurement results illustrating neural event coincidence detection through variation of parameters governing synapse type, synapse strength, and axonal delay. The presented measurements for a single addressed neuron can be extended to all 2^{16} neurons on the chip in a scalable and low-power architecture for synchrony detection and temporal coding based applications.

II. System Architecture

We have developed the HiAER-IFAT communication architecture for routing neural events in a scaleable reconfigurable large-scale neuromorphic system. The scaleable hierarchy allows for large-scale neural system implementation while minimizing queue occupancy [11]. The neural events are routed in real-time through synaptic connections with configurable parameters governing connectivity, synaptic strength, and axonal delay. Each analog chip is partitioned into two halves, each with individually controlled dynamics governing four types of synapse input activation dynamics and synapse reversal potential in addition to global parameters for membrane threshold values, etc.

All 2^{16} neurons on the chip are individually addressable. And the spike events that they generate are served sequentially through arbitration for transmission of address-events over two communication buses. Here we experimentally characterize a single addressed neuron in the HiAER-IFAT architecture, complete with two membrane compartments and with neural and synaptic activation circuits, as described in Figure 1. Each synapse implements time-multiplexed conductance-based dynamics in the log-domain with a compact three transistor circuit [12]. Each neuron implements two-compartment leaky integrate-and-fire (IFAT) dynamics [10], [13], [14].

III. Biophysical Models

A. Time-multiplexed conductance-based synapse dynamics

Coincidence detection of postsynaptic events upon the neuron membrane occurs when two or more events arrive in a short time window "coincidentally" to trigger a neural event. In order to ensure that only coincident postsynaptic events integrate together upon the neural member, the conductance (G) -capacitance (C) integration time constant must be short and comparable to the synapse activation time constant. In addition to triggering a coincident neural event through the mapping of several synaptic connections to a single neuron, we incorporate axonal delays through the synaptic connectivity in our system by HiAER routing [10]. These axonal delays allow the coincidence detection to become very input specific through temporal coding [15]–[17].

The postsynaptic current contribution for a single conductance-based synapse can be expressed by a conductance G modulated by the potential difference between reversal potential E_{rev} and membrane potential V:

$$I_{syn} = G(E_{rev} - V) \tag{1}$$

where the conductance G can be further expressed as:

$$G = G_0(t) * f(t) \tag{2}$$

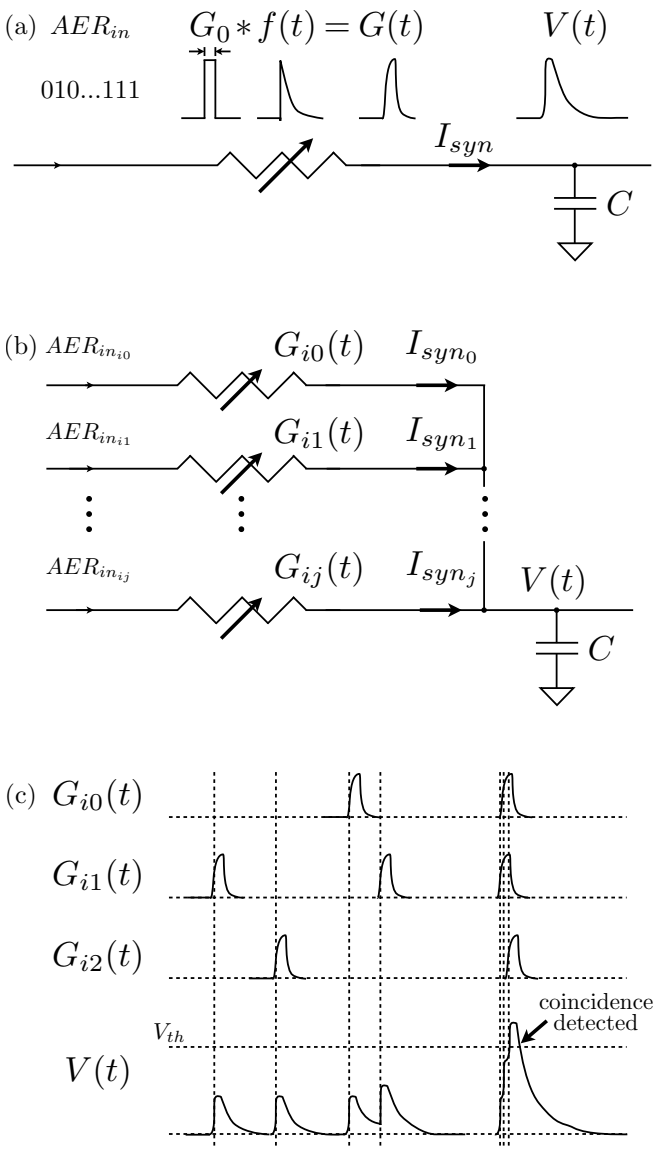

Fig. 2. (a) Block diagram showing the conductance-capacitance relationship for a single synaptic conductance connecting to the membrane capacitance C, where the conductance strength G_0 is modulated by the $f(t)$ function resulting in $G(t)$ and through integration upon C, $V(t)$. (b) Block diagram showing the conductance-capacitance relationship for multiple conductance synapses. (c) Time-varying $G(t)$ from multiple conductance-synapses showing coincidence detection when multiple input spike events coincide and are net excitatory.

where $*$ denotes convolution in time, $G_0(t)$ denotes the pulse-width modulated synaptic conductance strength, $f(t)$ denotes the synaptic input event activation dynamics, which we model with an instantaneous rise time and finite exponential decay fall time such that

$$f(t) = e^{-t/\tau} \tag{3}$$

and as illustrated in Fig. 2. The coincidence of several postsynaptic events is illustrated in Fig. 2(c).

We implement these dynamics in time-multiplexed conductance-based synapses [12] where each synapse is

composed of three parameters. The nominal conductance G_0 is digitally controllable in graded fashion while the other two parameters governing reversal potential E_{rev} and activation time constant V_τ are digitally selectable and globally configurable as one of four synapse types unique for each half of the chip.

B. Neural membrane dynamics

Neurons are implemented as two-compartment leaky integrate-and-fire neurons with two synaptic inputs per compartment and dynamics,

$$C_1 \frac{dV_{i_1}}{dt} = \sum_j I_{ij_1} + g_L(E_L - V_{i_1}) + g_{comp}(V_{i_0} - V_{i_1}) \quad (4)$$

$$C_0 \frac{dV_{i_0}}{dt} = f(V_{i_0}) + \sum_j I_{ij_0} + g_L(E_L - V_{i_0}) + g_{comp}(V_{i_1} - V_{i_0}) \quad (5)$$

where C_n denotes the membrane capacitance for neuron compartment n, $f(V_{i_n})$ denotes the nonlinear positive feedback dynamics, I_{ij_n} denotes the synaptic current contributions, g_L denotes the leak conductance, E_L denotes the leak reversal potential, and g_{comp} denotes the conductance between compartments.

We implement the positive feedback dynamics $f(V_{i_0})$ through a single transistor operating in subthreshold resulting in exponential nonlinear term in the feedback current. We fix the configurable global parameter, threshold voltage V_{th}, which provides the threshold-initiated regeneration amplification in this circuit [13], [14].

IV. Log-domain mapping

We model the linear conductor for each synapse and neuron with a single transistor operating in subthreshold by virtue of the log transform of its node voltages [18]. The subthreshold drain current can be expressed as

$$i = I_0 \frac{W}{L} e^{\kappa V_g}(e^{-V_s} - e^{-V_d}) \quad (6)$$

where V_g is the gate node voltage, V_s is the source node voltage, and V_d is the drain node voltage with each expressed in terms of V_T. Transformed to the "log-domain" or "pseudo-voltage domain", each "pseudo-parameter" describes the associated signal in log-domain [19], [20]

$$i = G^*(E^*_{rev} - V^*_m) \quad (7)$$

with pseudo-parameters conductance $G^* = I_0 \frac{W}{L} e^{\kappa V_g}$, membrane voltage $V^*_m = -e^{-V_s}$, and reverse potential $E^*_{rev} = -e^{-V_d}$.

Thus we can express the postsynaptic current contribution from synapses of type (θ) to be:

$$\sum_j I_{syn_j} = \sum_j \sum_k g^{(\theta)}_{ij}(t^k_j) e^{-(t-t^k_j)/\tau^{(\theta)}}(E^{(\theta)}_{ij} - V_i) \quad (8)$$

where i denotes the post-synaptic neuron, j denotes the pre-synaptic neuron, k indicates the spiking event number, g_{ij} is the conductance strength between neuron i and neuron j for synapse type (θ), τ indicates the decaying exponentials in the conductance dynamics profile for synapse type (θ), E_{ij} is the reversal potential between neuron i and neuron j, and V_i is the membrane voltage of post-synaptic neuron i.

The decaying exponential synaptic input activation dynamics (3) is implemented in the log domain as a linear decay by constant current draining the synapse gate capacitance [12]. The current circuit realization does not implement transcapacitance [18], but instead uses constant capacitance in the log domain leading to nonlinear membrane dynamics in the current domain, with faster onset and slower decay times.

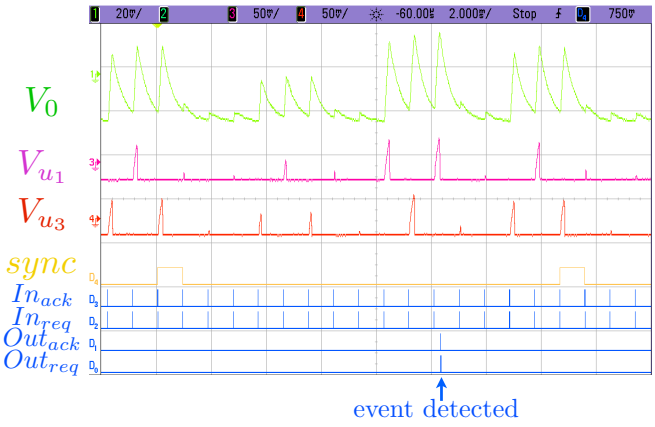

Fig. 3. Oscilloscope traces showing periodic synaptic input train of excitatory synaptic events with constant delay between events and varying synapse conductance strength amplitude resulting in neural event activation.

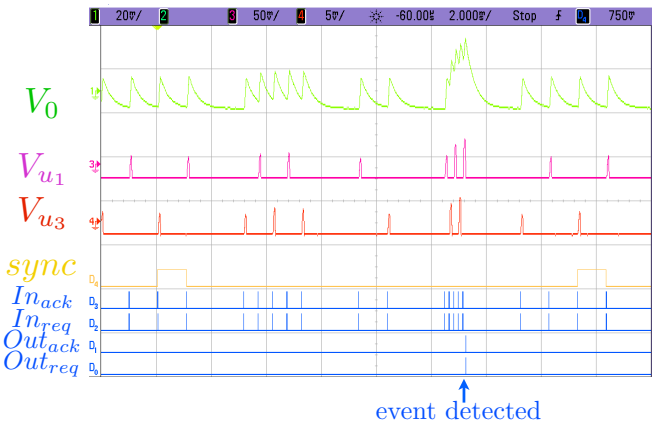

Fig. 4. Oscilloscope traces showing periodic synaptic input train of excitatory synaptic events with constant synaptic conductance strength amplitude and varying delay between events resulting in neural event activation.

V. Results

We test three scenarios to verify integration of neural events and coincidence detection. First we input a periodic stream of regularly spaced excitatory synaptic events into alternating neural compartments with varying synapse strength G_0 as seen in Fig. 3. We observe that only the sequences of synaptic events with sufficient synapse strength such that

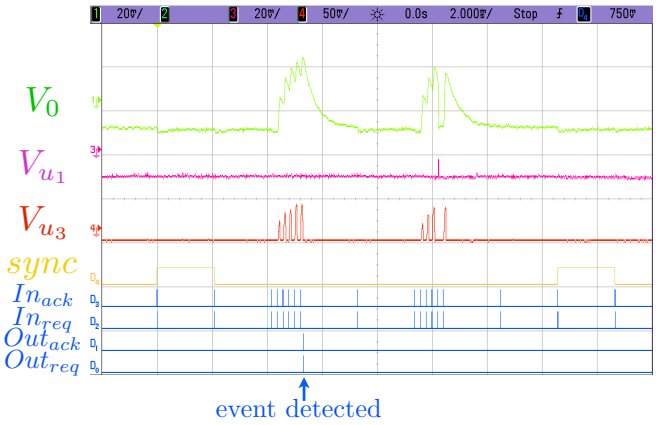

Fig. 5. Oscilloscope traces showing periodic synaptic input train of excitatory and inhibitory synaptic events resulting in neural event activation with additional inhibitory synaptic events resulting in removal of neural event activation.

the time of decay is greater than the time between pulses results in integration of events upon the neural membrane and subsequent event activation. Next we input a periodic stream of excitatory synaptic events with equal strength into alternating neural compartments with varying delay between events as seen in Fig. 4. We observe that only the sequences of synaptic events that occur with delay small enough to allow for integration of events upon the neural membrane results in subsequent event activation. Finally, we input a periodic stream of synaptic events with two packets of events with short delay inbetween as seen in Fig. 5. The first packet is comprised of five excitatory events and the second is the same except the fourth event is inhibitory. We observe that a single inhibitory event is sufficient to prevent integration of events upon the neural membrane resulting in subsequent event activation.

VI. Conclusion

We have presented and analyzed coincidence detection of convergent presynaptic action potentials and its effect on synchronous postsynaptic action potential firing. To this end we have described the architecture of a two-compartment conductance-based integrate-and-fire transceiver array (IFAT) for scaleable neural dynamics, and presented experimental results characterizing two-compartment membrane voltage and synaptic conductance dynamics for a single addressed neuron in the architecture. We outline the biophysical models of the synapse and neural dynamics that results in integration of events and coincidence detection. Robust postsynaptic output spike events were observed under varying presynaptic conductance, spike timing, and multiplicity, while synchronous inhibition was effective in eliminating postsynaptic firing.

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