A Superposable Silicon Synapse with Programmable Reversal Potential

Ben V. Benjamin¹, John V. Arthur², Peiran Gao¹, Paul Merolla², and Kwabena Boahen¹

Abstract— We present a novel log-domain silicon synapse designed for subthreshold analog operation that emulates common synaptic interactions found in biology. Our circuit models the dynamic gating of ion-channel conductances by emulating the processes of neurotransmitter release–reuptake and receptor binding–unbinding in a *superposable* fashion: Only a single circuit is required to model the entire population of synapses (of a given type) that a biological neuron receives. Unlike previous designs, which are strictly excitatory or inhibitory, our silicon synapse implements—for the first time in the log-domain—a programmable reversal potential (i.e., driving force). To demonstrate our design's scalability, we fabricated in 180nm CMOS an array of 64K silicon neurons, each with four independent superposable synapse circuits occupying 11.0 × 21.5 μ m² apiece. After verifying that these synapses have the predicted effect on the neurons' spike rate, we explored a recurrent network where the synapses' reversal potentials are set near the neurons' threshold, acting as shunts. These shunting synapses synchronized neuronal spiking more robustly than nonshunting synapses, confirming that reversal potentials can have important network-level implications.

I. LOG-DOMAIN NEURONS AND SYNAPSES

Neuromorphic engineering aims to emulate computations carried out in the nervous system by mimicking neurons and their interconnectivity in VLSI hardware [1]. Having succeeded in morphing visual and auditory sensory systems into mixed-analog-digital circuits, engineers are entering the arena of cortical modeling [2], [3], [4]; an arena in which neuromorphic systems' parallel operation and low energy consumption give them distinct advantages over software simulation. The neuron model of choice for large-scale cortical simulations [5], the quadratic integrate-and-fire (QIF) neuron, has been implemented successfully with log-domain circuits [6], [7], [8], [9]. The corresponding synapse model, a conductance tied to a programmable reversal potential, is however yet to be fully implemented in the log-domain.

Existing log-domain conductance-based silicon synapse designs are either purely excitatory or purely inhibitory [6], [10], [11]. In contrast, biological synapses behave like a conductance that drives the membrane toward a fixed voltage the reversal potential—that can be excitatory (much higher), inhibitory (much lower), or shunting (near the membrane's spike threshold). Shunting synapses have been shown to synchronize a heterogeneous population of neurons more

Fig. 1. Superposable silicon synapse, together with biasing and neuron circuitry (gray). The *cleft* (M_{C1-2}) models spike-triggered neurotransmitter release and reuptake: M_{C1} discharges C_C to ground (release) and M_{C2} charges $C_{\rm C}$ back up to $V_{\rm DD}$ (reuptake). The *receptor* (M_{R1-4}) models receptor binding and unbinding: M_{R1} discharges C_R to a limit set by M_{R2} (binding) and M_{R3} charges it back up to V_{DD} (unbinding). The $diffusor$ (M_{G1-4}) models spatial decay: M_{R4}'s current, mirrored by M_{A1-2}, spreads through M_{G1-3} into a hexagonal grid. The *reverser* (M_{E1-5}) models a conductance and its reversal potential: M_{G4} sets M_{E4} 's & M_{E5} 's currents (conductance) and M_{E3} sets how much the former's current is scaled (reversal potential). These currents drive the neuron's capacitor (C_m) , together with a leakage current (M_{S7}) , to produce an output current (M_{S1}) .

robustly by slowing down those that spike too fast and speeding up those that fire too slowly [12].

To remedy the deficiency in existing log-domain silicon synapse designs, we developed a new silicon synapse by adding a reversal-potential subcircuit to our previous design [6]. In this paper, we present the synapse's design and test results (Section II), theoretically predict and verify its effect on the QIF neuron's spike rate (Section III), and confirm that the highest degree of synchrony is achieved when the synapse is shunting (Section IV). The paper concludes with a brief summary.

II. SYNAPSE CIRCUIT

The effect a population of synapses with total conductance g_{syn} and a common reversal potential e_{rev} has on the neuron's membrane potential v_m is described by

$$
\tau_{\rm m}\dot{v}_{\rm m} = -v_{\rm m} + g_{\rm syn}(e_{\rm rev} - v_{\rm m})\tag{1}
$$

where $\tau_{\rm m}$ is the membrane time-constant. The linear term, $-v_{\rm m}$, models a leakage conductance (normalized to one) with its reversal potential set to zero (voltage reference). $v_{\rm m}$ is normalized by the threshold voltage and g_{syn} is normalized by the leakage conductance. Notice that the synaptic input consists of a current source $(g_{syn}e_{rev})$ and a conductance to

Supported by a NIH Director's Pioneer Award (DPI-OD000965) and the Samsung Advanced Institute of Technology GRO Program.

¹B. Benjamin is with Electrical Engineering and P. Gao and K. Boahen are with Bioengineering, Stanford University, Stanford CA, U.S.A. {benvb,prgao,boahen}@stanford.edu

² J. Arthur and P. Merolla were with Bioengineering, Stanford University, Stanford CA, U.S.A. {arthurjo,pameroll}@us.ibm.com

ground $(g_{\rm syn})$, similar to excitatory and inhibitory synapses, respectively. In the log-domain, these circuit elements are realized by tying a transistor's source or drain, respectively, to the silicon neuron's membrane capacitor [6].

The dynamic gating of synaptic conductances is modeled by emulating neurotransmitter release from axonal terminals and binding to postsynaptic receptors as was done previously [14], [6]. Spikes are fed into a pulse-extender that models how long neurotransmitter remains in the synaptic cleft by producing t_{rise} -wide unit-amplitude pulses, $p_{\text{rise}}(t)$ (Fig 1, *cleft*). These pulses feed a lowpass filter that models receptor binding–unbinding by decaying at a rate, $1/\tau_{\rm syn}$, proportional to the unbinding rate (Fig 1, *receptor*). Thus

$$
\tau_{\rm syn} \dot{g}_{\rm syn} = -g_{\rm syn} + g_{\rm sat} \min(\sum_i p_{\rm rise} (t-t_i), 1)
$$

where t_i are spike times and g_{sat} is the saturation value attained when all the synapses' postsynaptic ion-channels are open—each synapse is assumed to contribute equally. Overlapping pulses do not sum—they yield an elongated unit-amplitude pulse that starts with the first and ends with the last. Hence, $g_{syn} = (1 - \exp(-t_{rise} f_{tot})) g_{sat}$ in steadystate for Poisson spike trains with total rate f_{tot} . This output feeds the reversal-potential subcircuit (Fig 1, *reverser*).

Analysis confirms that the reversal-potential subcircuit behaves as described by Eq 1—and yields the mapping parameters needed to convert neuronal parameters into bias currents. The membrane capacitor's current is

$$
C_{\rm m}\dot{V}_{\rm m} = I_{\rm E5} - I_{\rm E4} + I_{\rm S7}
$$

=
$$
\frac{\alpha_{\rm E5}}{\alpha_{\rm E1}}I_{\rm G4} - \frac{\alpha_{\rm E4}\alpha_{\rm S1}}{\alpha_{\rm E2}\alpha_{\rm E1}}\frac{I_{\rm E2}I_{\rm E1}}{I_{\rm S1}} + \alpha_{\rm S7}I_{\rm lk}
$$

where I_n and α_n are transistor M_n 's current and sizing ratio, normalized by the biasing transistors' sizing ratio (e.g., $I_{\rm{S7}}/\alpha_{\rm{S7}} = I_{\rm{lk}}$). $I_{\rm{E4}}$ was obtained by applying the translinear principle: $(I_{\text{E2}}/\alpha_{\text{E2}})(I_{\text{E1}}/\alpha_{\text{E1}}) = (I_{\text{E4}}/\alpha_{\text{E4}})(I_{\text{S1}}/\alpha_{\text{S1}})$. With $\alpha_{E1} = \alpha_{E5}$, $I_{E2} = I_{E3} = \alpha_{E3}I_{e_{rev}}$, $I_{E1} = I_{G4}$ and $\dot{V}_{\text{m}} = -U_T \dot{I}_{S1}/(\kappa I_{S1})$, where U_T is the thermal voltage and κ is the subthreshold slope-coefficient, we obtain

$$
\frac{C_{\rm m}U_T}{\kappa \alpha_{\rm S7}I_{\rm lk}}\dot{I}_{\rm S1} = \frac{I_{\rm G4}}{\alpha_{\rm S7}I_{\rm lk}} \left(\frac{\alpha_{\rm E4} \alpha_{\rm S1} \alpha_{\rm E3}}{\alpha_{\rm E2} \alpha_{\rm E1}} I_{\rm e_{\rm rev}} - I_{\rm S1} \right) - I_{\rm S1}
$$

Setting $v_{\rm m} = I_{\rm S1}/(\gamma I_{\rm lk})$, where γ is a normalization factor (derived in [13]), yields

$$
\frac{p_{\tau_{\rm m}}}{I_{\rm lk}}\dot{v}_{\rm m} = -v_{\rm m} + p_{\rm g_{syn}} \frac{I_{\rm G4}}{I_{\rm lk}} \left(p_{\rm e_{rev}} \frac{I_{\rm e_{rev}}}{I_{\rm lk}} - v_{\rm m} \right)
$$
 (2)

with mapping parameters

$$
p_{e_{rev}} = \alpha_{E4} \alpha_{S1} \alpha_{E3} / (\gamma \alpha_{E2} \alpha_{E1})
$$
 and $p_{g_{syn}} = 1 / \alpha_{S7}$

Their values are determined either from the device dimensions or through a calibration procedure (similar to [13]); the latter yields more accurate results. Equating Eq 1's neuronal parameters to Eq 2's coefficients yields

$$
I_{\text{e}_{\text{rev}}} = e_{\text{rev}} I_{\text{lk}} / p_{\text{e}_{\text{rev}}}
$$
 and $I_{\text{G4}} = g_{\text{syn}} I_{\text{lk}} / p_{\text{g}_{\text{syn}}}$

This model-circuit mapping enables us to program the bias currents appropriately.

Fig. 2. Synapse circuit's measured waveforms. a. Increasing the rise time (t_{rise}) makes the conductance peak later—and increases its peak value $(\tau_{syn} = 25 \text{ms})$. **b**. Increasing the saturation value (g_{sat}) rescales the entire waveform (τ_{syn} = 25ms, t_{rise} = 5ms). c. Increasing the time constant (τ_{syn}) slows down the rise as well as the fall ($t_{rise} = 50$ ms). **d**. Increasing the reversal potential (e_{rev}) cause's the conductance's effect on the membrane potential to reverse when $e_{\text{rev}} = v_{\text{m}} = 0.1$ ($\tau_{\text{syn}} =$ $50\text{ms}, t_{\text{rise}} = 100\text{ms}, \tau_{\text{m}} = 25\text{ms}.$

The synapse circuit's conductance and membrane potential waveforms varied as expected when we programmed various values for its model parameters (Fig 2). Their mapping parameters were used to set $M_{\rm C2}$'s, $M_{\rm R2}$'s, $M_{\rm R3}$'s, and M_{E3} 's gate voltages through biasing transistors driven by an on-chip DAC (see Fig 1). Four sets of DACs program each of a silicon neuron's four superposable synapse circuits independently, but these biases are shared by all synapse circuits on that chip. I_{G4} and I_{S1} were mirrored by transistors (in parallel with $M_{E1,5}$ and M_{S1}) connected to an on-chip ADC through a scanner. For $t_{\text{rise}} \ll \tau_{\text{syn}}$, the conductance peaks at $g_{\text{sat}}t_{\text{rise}}/\tau_{\text{syn}}$ (Fig 2a,b). For $t_{\text{rise}} \gg \tau_{\text{syn}}$, it plateaus at g_{sat} (Fig 2c). Its effect can be excitatory ($e_{\text{rev}} > v_{\text{m}}$), inhibitory ($e_{\text{rev}} < v_{\text{m}}$), or shunting ($e_{\text{rev}} \sim v_{\text{m}}$) (Fig 2d).

III. QIF NEURON'S CONDUCTANCE-FREQUENCY CURVE

When we drive a QIF neuron with a synaptic population it obeys the differential equation

$$
\tau_{\rm m} \dot{v}_{\rm m} = -v_{\rm m} + v_{\rm m}^2/2 + i_{\rm in} + g_{\rm syn}(e_{\rm rev} - v_{\rm m}) \tag{3}
$$

 $v_{\rm m}^2/2$ models positive feedback provided by sodium channels; i_{in} is an input current (normalized by the threshold voltage times the leak conductance) that we set to zero. This model is a 1D dynamical system with bifurcation parameter g_{syn} (i.e., it determines the number of fixed points) (Fig 3a).

To find the the conditions under which the neuron spikes, we determine the values for g_{syn} at which bifurcations occur. They occur when the minimum point of the neuron's phase

Fig. 3. Conductance-driven QIF neuron's phase $(\dot{v}(v))$ and spike-rate $(f(g_{syn}))$ curves. **a**. As g_{syn} increases, the phase curve's minimum point follows an inverted parabola (dashed line) centered at $v = e_{\text{rev}}$, causing the fixed points (circles) to disappear and reappear. **b**. As e_{rev} increases, the spike rate reaches a higher plateau that occurs at a higher $g_{\rm syn}$ value and the upper bifurcation point moves rightward.

curve $(v_{\text{min}}, \tau_{\text{m}}\dot{v}_{\text{min}})$ touches the x-axis. This minimum point is obtained by equating $\frac{dv_{\text{m}}}{dv_{\text{m}}}$ to 0 and substituting the result into Eq 3

$$
v_{\rm min} = 1 + g_{\rm syn}, \ \tau_{\rm m} \dot{v}_{\rm min} = g_{\rm syn} e_{\rm rev} - (1 + g_{\rm syn})^2 / 2
$$

It touches the x-axis (i.e., $\tau_m \dot{v}_{\text{min}} = 0$) when g_{syn} 's value is

$$
g_{\rm syn}^{*\pm} = (e_{\rm rev} - 1) \pm \sqrt{(e_{\rm rev} - 1)^2 - 1} \text{ for } e_{\rm rev} > 2
$$

For $g_{syn} < g_{syn}^{*-}$, two fixed points exist: an upper unstable one and a lower stable one, at which the neuron rests. For $g_{\text{syn}}^* < g_{\text{syn}} < g_{\text{syn}}^*$, these fixed points disappear, and the neuron spikes. For $g_{syn} > g_{syn}^{*+}$, the fixed points reappear and spiking ceases. When $e_{\text{rev}} < 2$, $\tau_{\text{m}} \dot{v}_{\text{min}}$'s maximum value, $e_{\rm rev}(e_{\rm rev}/2 - 1)$, is less than zero. Hence the fixed points never disappear and the neuron never spikes.

To calculate the interspike interval T , we integrate Eq 3

$$
\int_{t_{\text{ref}}}^{T} dt = \tau_{\text{m}} \int_{0}^{\infty} \frac{1}{v_{\text{m}}^{2} / 2 + g_{\text{syn}}(e_{\text{rev}} - v_{\text{m}}) - v_{\text{m}}} dv_{\text{m}}
$$

$$
\Leftrightarrow T - t_{\text{ref}} = \tau_{\text{m}} h(g_{\text{syn}})
$$

where t_{ref} is the refractory period and

$$
h(g_{\rm syn}) = \frac{\pi + 2 \arccot(\sqrt{2e_{\rm rev}g_{\rm syn}/(1+g_{\rm syn})^2 - 1})}{(1+g_{\rm syn})\sqrt{2e_{\rm rev}g_{\rm syn}/(1+g_{\rm syn})^2 - 1}}
$$

Inverting T yields the conductance-driven spike rate

$$
f(g_{\rm syn}) = 1/(\tau_{\rm m} h(g_{\rm syn}) + t_{\rm ref})
$$
 for $g_{\rm syn}^* < g_{\rm syn} < g_{\rm syn}^*$ (4)

The rate rises sharply from zero as g_{syn} increases beyond g_{syn}^* , peaks when g_{syn} is a little less than $e_{\text{rev}}-1$, g_{syn} 's value when $\tau_{\rm m} \dot{v}_{\rm min}$ is maximum, and drops precipitiously to zero

Fig. 4. Synapse circuit's measured rate-conductance curve. An excellent match is obtained between theory (lines) and experiment (dots). And, as expected, the neuron did not spike for $e_{rev} = 1$ or 2. The model's parameter values were $\tau_{\rm m} = 15$ ms and $t_{\rm ref} = 5$ ms; the fitted values were 0.96 $\tau_{\rm m}$, $1.00t_{\rm ref}$, $0.96e_{\rm rev}$, and $1.00g_{\rm syn} + 0.3$.

when g_{syn} approaches g_{syn}^{*+} (Fig 3b). The peak occurs earlier than expected because the phase curve's rightward movement makes $v_{\rm m}$ travel further and further away from zero (reset). For $e_{\text{rev}} \gg 1$, spiking starts at $g_{\text{syn}}^{*-} \approx 1/(e_{\text{rev}} - 1)/2$ and stops at $g_{syn}^{*+} \approx 2(e_{rev} - 1)$. Quadratic positive-feedback is unable to overcome conductances larger than this. They shunt the membrane potential to e_{rev} strongly enough to prevent spiking—even when $e_{\text{rev}} \gg 1$ —a counterintuitive result.

We compared these theoretically predicted $f(g_{syn})$ curves with measurements made by varying M_{R2} 's gate voltage and recording the silicon neuron's spikes (Fig 4). M_{R1} was kept on continuously by inputing spikes at intervals shorter than t_{rise} (set to 30ms), thereby pinning g_{syn} to g_{sat} . The spike rate varied as expected, with lower and upper bifurcation points, steep onset and offset, and peak spike rate all closely matching the theory. These results also validated the calibration procedure: The fitted parameter values were within 4% of the programmed ones.

IV. SYNCHRONY

The $f(g_{syn})$ -curves' extended plateau makes the neuron's spike rate relatively independent of the amount of synaptic input, which should promote synchrony in a heterogeneous population by homogenizing spike rates. Indeed, this has been demonstrated in a recurrent network model of gammaband (30-80Hz) synchronization: Coherence (normalized pairwise cross-correlation) was highest when synapses were shunting [12]. Shunting also rescued neurons silenced by inhibition, increasing the number of active neurons by 100%.

We confirmed that synchrony is more robust when synapses are shunting (Fig 5). A recurrent neural network model with circularly symmetric local arbors was implemented in a 256×256 -array of silicon neurons on a single chip. Point-to-point connections were realized by multiplexing spikes using the address-event representation and arbors were realized by relaying analog currents from neuron to neuron with a programmable decay factor $\lambda = 0.8$ (Fig 1,

Fig. 5. Spike rasters from a recurrent network of 65,536 silicon neurons. Synchrony improves as e_{rev} changes from inhibitory (0.1) to shunting (1.0). The rhythm's frequency and the number of active neurons increase as well. Neurons firing faster than twice the mean rate were excluded ($\tau_{\rm m} = 15$ ms, $t_{\text{ref}} = 1 \text{ms}, i_{\text{in}} = 0.6, g_{\text{sat}} = 40, \tau_{\text{syn}} = 10 \text{ms}, \tau_{\text{rise}} = 5 \text{ms}.$

diffusor), both as described previously [6].

The model's parameters were mapped onto the chip's single set of circuit biases using its silicon neurons' and synapses' median mapping parameters. This approach resulted in a heterogenous implementation of the model whose median parameter values matched the specified values but whose variance was determined by device mismatch [13]. For instance, all neurons received a lognormally distributed tonic current with median $i_{\text{in}} = 0.6$ and $CV = 22.5\%$ (standard deviation/mean) [13]. This degree of heterogeneity is significantly higher than the previous study's, whose tonic current was normally distributed with $CV = 10\%$ [12].

We varied e_{rev} from inhibitory (0.1 to 0.5), to shunting (0.5 to 1.0), to excitatory (1.0 to 3.0) and found coherence to be highest in the shunting region (Fig 6). For $i_{\rm in} > 0.5$, the theory predicts that the $f(g_{syn})$ curve starts with a nonzero spike rate (at $g_{syn} = 0$) that can either decrease or increase as g_{syn} increases, depending on e_{rev} . The slope is flat near $g_{syn} = 0$ when $e_{rev} \approx 1$, because the $f(g_{syn})$ curve still peaks near $g_{syn} = e_{rev} - 1$ when $i_{in} \neq 0$. Hence, we expect the spike rates to be maximally homogenized when $e_{\text{rev}} \approx 1$, enabling the neurons to synchronize with maximal coherence. Indeed, coherence peaked when e_{rev} was 0.9. As e_{rev} increased from 0.3 to 0.9, the rhythm's frequency increased from 15Hz to 70Hz and the number of active neurons increased from 3,789 to 9,671.¹

V. SUMMARY

We presented the first log-domain silicon synapse with a programmable reversal-potential, realized with just five transistors. Our's is a pure log-domain design, unlike a recent proposal, which requires a resistor [15]. In addition to reversing its effect when the membrane potential crosses the reversal potential, our superposable synapse circuit captures a synaptic population's dynamic behavior through its programmable rise time, decay constant, and saturation value. We proved analytically that the QIF neuron's $f(g_{syn})$ curve is nonmonotonic—unlike its $f(i)$ curve [9], [13]—and confirmed that silicon neurons driven by our new silicon synapse

Fig. 6. Coherence (squares) peaked at $e_{rev} = 0.9$ whereas the number of active neurons (discs) increased monotonically with e_{rev} .

displayed this behavior. Finally, we demonstrated that the silicon synapse synchronizes silicon neurons most robustly when it is shunting, confirming that reversal potentials can have important implications at the network-level.

ACKNOWLEDGEMENTS

The authors would like to thank Julie Dethier and Patrick Ye for collecting and analyzing the synchrony data.

REFERENCES

- [1] C. Mead, *Analog VLSI and Neural Systems*. Reading, MA: Addison-Wesley, 1989.
- [2] R. J. Vogelstein, U. Mallik, E. Culurciello, G. Cauwenberghs, and R. Etienne-Cummings, "A multichip neuromorphic system for spikebased visual information processing," *Neural Computation*, vol. 19, pp. 2281–300, 2007.
- [3] J. Schemmel, D. Brandderle, A. Grandbl, M. Hock, K. Meier, and S. Millner, "A wafer-scale neuromorphic hardware system for largescale neural modeling," in *Proc. ISCAS*, pp. 1947–50, 2010.
- [4] T. Y. Choi, P. A. Merolla, J. V. Arthur, K. A. Boahen, and B. E. Shi, "Neuromorphic implementation of orientation hypercolumns," *IEEE Trans. Circuits Syst. I*, vol. 52, pp. 1049–60, 2005.
- [5] E. M. Izhikevich and G. M. Edelman, "Large-scale model of mammalian thalamocortical systems," *PNAS*, vol. 105, pp. 3593–98, 2008.
- [6] J. V. Arthur and K. A. Boahen, "Synchrony in silicon: The gamma rhythm," *IEEE Trans. Neural Netw.*, vol. 18, pp. 1815–25, 2007.
- [7] V. Rangan, A. Ghosh, V. Aparin, and G. Cauwenberghs, "A subthreshold aVLSI implementation of the Izhikevich simple neuron model," in *Proc. EMBS*, pp. 4164–67, 2010.
- [8] A. van Schaik, C. Jin, A. McEwan, and T. J. Hamilton, "A log-domain implementation of the Izhikevich neuron model," in *Proc. ISCAS*, pp. 4253–56, 2010.
- [9] J. V. Arthur and K. Boahen, "Silicon-neuron design: A dynamical systems approach," *IEEE Trans. Circuits Syst. I*, vol. 58, pp. 1034– 1043, 2011.
- [10] C. Bartolozzi and G. Indiveri, "Synaptic dynamics in analog VLSI," *Neural Computation*, vol. 19, pp. 2581–603, 2007.
- [11] R. Z. Shi and T. Horiuchi, "A summating, exponentially-decaying CMOS synapse for spiking neural systems,", *NIPS 16*, S. Thrun et al., eds, pp. 1003–10, MIT Press, Cambridge MA, 2004.
- [12] I. Vida, M. Bartos, and P. Jonas, "Shunting Inhibition Improves Robustness of Gamma Oscillations in Hippocampal Interneuron Networks by Homogenizing Firing Rates", *Neuron*, vol. 49, no. 1, pp. 107–17, 2006.
- [13] P. Gao, B. V. Benjamin and K. Boahen, "Dynamical system guided mapping of quantitative neuronal models onto neuromorphic hardware," *IEEE Trans. Circuits Syst.* In press.
- [14] A. Destexhe, Z. F. Mainen, and T. J. Sejnowski, "Synthesis of models for excitable membranes, synaptic transmission and neuromodulation using a common kinetic formalism," *J. Comp. Neuro.*, vol. 1, pp. 195– 230, 1994.
- [15] T. Yu, S. Joshi, V. Rangan, and G. Cauwenberghs, "Subthreshold MOS dynamic translinear neural and synaptic conductance," *Int. IEEE/EMBS Conf. Neural Eng.*, pp. 68-71, 2011.

¹Only a small fraction were active because the highly excited neurons suppressed their neighbors. The chip's kill bits, which can be set to disable neurons, were not utilized in this study.