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FPGA-Based Recurrent Wavelet Neural Network Control System for Linear Ultrasonic Motor

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Abstract

A field-programmable gate array (FPGA)-based recurrent wavelet neural network (RWNN) control system is proposed to control the mover position of a linear ultrasonic motor (LUSM) in this study. First, the structure and operating principles of the LUSM are introduced. Since the dynamic characteristics and motor parameters of the LUSM are nonlinear and time-varying, an RWNN controller is designed to improve the control performance for the precision tracking of various reference trajectories. The network structure and its on-line learning algorithm using delta adaptation law of the RWNN are described in detail. Moreover, an FPGA chip is adopted to implement the developed control algorithm for possible low-cost and high-performance industrial applications. Finally, the effectiveness of the proposed control system is verified by some experimental results.

1. Introduction

LUSMs are one of the new kinds of ultrasonic motors (USMs) which are driven by the ultrasonic vibration force of piezoelectric ceramic elements and the mechanical friction effect [1], [2]. Different constructions and driving principles of LUSMs have been reported [2], [3]. They permit high precision, fast control dynamics and large driving force in small dimensions. Thus, some precision motion control stages using LUSMs, which are small, light and high-precise positioning, have been developed for industrial applications [4], [5]. However, the control accuracy of the LUSMs is much influenced by the existence of uncertainties, which usually comprises parameter variations, external disturbances and high-order dynamics, etc. Moreover, the mathematical models of LUSMs are complex and the motor parameters are time-varying due to increasing in temperature and changing in motor drive operating conditions. Therefore, the intelligent control approaches are good candidates to control the motion control stage using LUSM for high performance applications due to their ability of to approximate nonlinear system without using the mathematical models of the controlled system.

Since the neural networks can approximate a wide range of nonlinear functions to any desired degree of accuracy under certain conditions [6], [7], the amount of research for neural networks control has been much increased in the past decade. Moreover, the connective weights of the neural networks can be tuned using the learning process to export ideal control signals for the mapping of the nonlinearity. Furthermore, the neural networks have parallel-processing and generalization capabilities, and their structures are robust for noise data and uncertainties. On the other hand, wavelets are well suited to depict functions with local nonlinearities and variations due to their intrinsic properties of finite support and self-similarity [8], [9]. With these specific features, much research has been done on the applications of wavelet neural networks (WNNs), which combine the capability of neural networks in learning from processes and the capability of wavelet decomposition [10].

FPGA incorporates the architecture of gate arrays and the programmability of a programmable logic device (PLD). It consists of thousands of logic gates, some of which are combined together to form a configurable logic block (CLB) thereby simplifying high-level circuit design. Moreover, concurrent operation, simplicity, programmability, a comparatively low cost and rapid prototyping make it the favorite choice for prototyping an application specific integrated circuit (ASIC) [11]. Furthermore, the circuits and algorithms can be developed in the VHSIC hardware description language (VHDL) [11]. This method is as flexible as any software solution. Another important advantage of VHDL is that it is technology independent. However, the major

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disadvantage of an FPGA-based system for hardware implementation is the limited capacity of available cells. In this study, the FPGA chip is adopted to implement the proposed RWNN controller in order to allow possible low-cost and high-performance industrial applications. The proposed control algorithms are realized on a 24MHz FPGA (XC2V1000) with 1 million gate counts and 10240 flip-flops from Xilinx, Inc using VHDL with the Q-format arithmetic representation. The design and implementation of the FPGA-based control system will be described in detail. Compared with a PC-based control system, the merits of the FPGA-based control system are parallel processing and small size in addition to low-cost. In addition, the developed VHDL code can be easily modified and implemented to control any type of motors as well.

2. Linear ultrasonic motor motion control stage

The motion control stage can be divided into two parts: the LUSM servo drive and a single-axis stage. The AB1A-SP-E1 drive manufactured by Nanomotion Corp. is adopted for the servo drive. Moreover, the motion control stage comprises one SP series LUSM, the SP1-02 LUSM, which is also manufactured by the Nanomotion Corp. The travel of the moving table of the motion control stage is linear. The moving table is directly driven using the spacer of the LUSM. Furthermore, the output of the RWNN is the command voltage (control effort) of the LUSM servo drive. The command voltage with ± 10 V is applied to the drive AB1A-SP-E1. The drive generates a fixed frequency (39.6kHz) sine wave voltage whose amplitude (0-280Vrms) is a function of the applied command voltage (0-10V). The generated sine wave voltage drives the LUSM, and then generates thrust force and velocity to rotate the moving table to reach the desired position. Detailed structure and operating principle of LUSM can be referred to the references [2]-[4].

3. Proposed control system

3.1. Recurrent wavelet neural network

The architecture of the RWNN including input layer (layer 1), membership layer (layer 2), rule layer (layer 3) and output layer (layer 4) with two inputs and one output is shown in Fig. 1. Furthermore, the signal propagation and the basic function of each layer are introduced in the following:

Layer 1 - Input Layer: In the input layer, the node input and the node output are represented as

$$u_i^{(1)}(k) = x_i^{(1)}(k) + O_i^{(1)}(k-1), \quad i = 1, 2 \tag{1}$$

$$O_i^{(1)}(k) = u_i^{(1)}(k) \tag{2}$$

where $u_i^{(1)}$ and $O_i^{(1)}$ are the input and output of the ith node in this layer, respectively; k represents the kth iteration; $x_1^{(1)}$ and $x_2^{(1)}$ are the tracking error e and its derivative $\dot{e}$, respectively.

Layer 2 – Membership Layer: A family of wavelets is constructed by translations and dilations performed on a single fixed function called mother wavelet. In this study, the first derivative of a Gaussian function $h(\cdot)$ has been chosen as the mother wavelet. Moreover, the first derivative of the Gaussian function may be regarded as a similar version of the Haar mother wavelet, just as the sigmoid function is a similar version of a step function. By properly choosing the parameters in the first derivative of the Gaussian function, it possesses the universal approximation property [12]. Furthermore, in order to reduce the computational requirements and facilitate the hardware implementation using FPGA, a triangular function is selected to approximate the first derivative of a Gaussian function. In membership layer, each node performs a wavelet from its mother wavelet and the node input and the node output are represented as:

$$u_{ij}^{(2)} = \frac{O_i^{(1)} - a_{ij}}{b_{ij}} \tag{3}$$

$$O_{ij}^{(2)} = \begin{cases} h(u_{ij}^{(2)}) & \text{if } u_{ij}^{(2)} < 0 \\ -h(u_{ij}^{(2)}) & \text{if } u_{ij}^{(2)} > 0 \end{cases}, \quad j = 1, 2, \cdots, 5 \tag{4}$$

$$h(x) = \begin{cases} 0 & \text{if} \quad x \geq m_1 + \sigma_1,\ x \leq m_1 - \sigma_1 \\ \dfrac{x - m_1 + \sigma_1}{\sigma_1} & \text{if} \quad m_1 - \sigma_1 < x \leq m_1 \\ \dfrac{-x + m_1 + \sigma_1}{\sigma_1} & \text{if} \quad m_1 < x \leq m_1 + \sigma_1 \end{cases} \tag{5}$$

where $u_{ij}^{(2)}$ and $O_{ij}^{(2)}$ are the input and output of the jth node of the ith input variable; a_{ij} and b_{ij} are the associated translation and dilation parameters of the wavelet membership function; m_1 is the center of the triangle; σ_1 is the center's width of the triangle.

Layer 3 - Rule Layer: In rule layer, two feedbacks including rule layer feedback and output layer feedback are considered. Moreover, a piecewise continuous function is selected to approximate the sigmoid function $f(x)$. In rule layer feedback, the node input and the node output are represented as:

$$u_j^f(k) = O_j^{(3)}(k-1) \tag{6}$$

$$O_j^f(k) = f(u_j^f(k)) \tag{7}$$

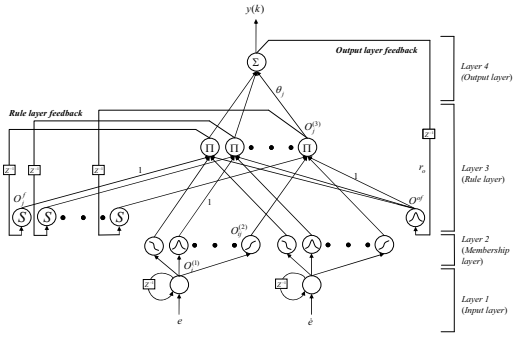

Figure 1. Network structure of RWNN

$$f(x)=\begin{cases} 1 & if \quad x > 0.5/a \\ 0 & if \quad x < -0.5/a \\ a\times x+0.5 & otherwise \end{cases} \tag{8}$$

where $u_j^f(k)$ and $O_j^f(k)$ are the input and output of the jth node in rule layer feedback, respectively; a is the slope of the piecewise continuous function. On the other hand, in the proposed RWNN, the feedback of output layer is taken into account with an active function $\exp(-x^2)$ to obtain better learning efficiency. A triangular function is selected to approximate this exponential function. The node input and the node output of output layer feedback are represented as:

$$u^{of}(k)=r_o\cdot y(k-1) \tag{9}$$

$$O^{of}(k)=\begin{cases} 0 & if \quad u^{of}(k)\ge m_2+\sigma_2,\ u^{of}(k)\le m_2-\sigma_2 \\ \dfrac{u^{of}(k)-m_2+\sigma_2}{\sigma_2} & if \quad m_2-\sigma_2<u^{of}(k)\le m_2 \\ \dfrac{-u^{of}(k)+m_2+\sigma_2}{\sigma_2} & if \quad m_2<u^{of}(k)\le m_2+\sigma_2 \end{cases} \tag{10}$$

where $u^{of}(k)$ and $O^{of}(k)$ are the input and output of the node in output layer feedback, respectively; r_o is the nonadjustable output recurrent weight; m_2 is the center of the triangle and σ_2 is the center's width of the triangle. Finally, the node input and the node output of rule layer are represented as:

$$u_j^{(3)}=O^{of}\cdot O_j^f\cdot O_{1j}^{(2)}\cdot O_{2j}^{(2)} \tag{11}$$

$$O_j^{(3)}=u_j^{(3)} \tag{12}$$

where $u_j^{(3)}$ and $O_j^{(3)}$ are the input and output of the jth node in rule layer respectively.

Layer 4 – Output Layer: In output layer, the node input and the node output are represented as:

$$u^{(4)}=\sum_{j=1}^{5}\theta_j\cdot O_j^{(3)} \tag{13}$$

$$V=y(k)=O^{(4)}=u^{(4)} \tag{14}$$

where $u^{(4)}$ and $O^{(4)}$ are the input and output of the node in output layer, respectively; θ_j is the connective weight between rule layer and output layer; $V=y(k)$ is the output of the RWNN and also is the control effort of the LUSM drive system. The control block diagram of the proposed RWNN control system is shown in Fig. 2, where d_m and d represent the reference trajectory and mover position of the LUSM, respectively.

3.2. On-line learning algorithm using delta adaptation law

To describe the on-line learning algorithm of the RWNN using supervised gradient decent method, first the energy function E is defined as:

$$E=\frac{1}{2}(d_m-d)^2=\frac{1}{2}e^2 \tag{15}$$

Then the learning algorithm is described as follows. The weights are updated by the amount

$$\Delta\theta_j=-\eta_\theta\frac{\partial E}{\partial\theta_j}=-\eta_\theta\frac{\partial E}{\partial y(k)}\frac{\partial y(k)}{\partial u^{(4)}}\frac{\partial u^{(4)}}{\partial\theta_j}=\eta_\theta\delta^{(4)}O_j^{(3)} \tag{16}$$

$$\theta_j(k+1)=\theta_j(k)+\Delta\theta_j \tag{17}$$

where $\delta^{(4)}=-\partial E/\partial y(k)=-\partial E/\partial d\times\partial d/\partial y(k)$, and the factor η_θ is the learning rate. The update laws of translation and dilation are

$$\Delta a_{ij}=-\eta_a\frac{\partial E}{\partial a_{ij}}=-\eta_a\frac{\partial E}{\partial O_{ij}^{(2)}}\frac{\partial O_{ij}^{(2)}}{\partial u_{ij}^{(2)}}\frac{\partial u_{ij}^{(2)}}{\partial a_{ij}} \tag{18}$$

$$=\eta_a\delta^{(4)}\theta_j(k)O^{of}O_j^fO_{ij}^{(2)}\frac{1}{b_{ij}}\frac{1}{\sigma_1}$$

$$a_{ij}(k+1)=a_{ij}(k)+\Delta a_{ij} \tag{19}$$

$$\Delta b_{ij}=-\eta_b\frac{\partial E}{\partial b_{ij}}=-\eta_b\frac{\partial E}{\partial O_{ij}^{(2)}}\frac{\partial O_{ij}^{(2)}}{\partial u_{ij}^{(2)}}\frac{\partial u_{ij}^{(2)}}{\partial b_{ij}} \tag{20}$$

$$=\eta_b\delta^{(4)}\theta_j(k)O^{of}O_j^fO_{ij}^{(2)}\frac{1}{b_{ij}}u_{ij}^{(2)}\frac{1}{\sigma_1}$$

$$b_{ij}(k+1)=b_{ij}(k)+\Delta b_{ij} \tag{21}$$

where the factors η_a and η_b are the learning rates.

The exact calculation of the Jacobian of the system, $\partial d/\partial y(k)$, is difficult to be determined due to the unknown dynamics of the LUSM drive system. To overcome this problem, a delta adaptation law is

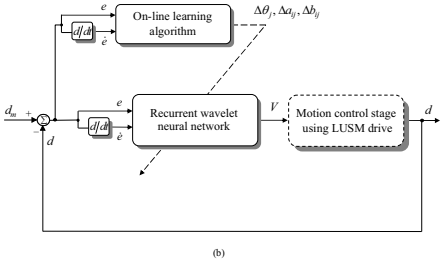

Figure 2. Block diagram of RWNN control system.

adopted as follows:

$$\delta^{(4)} \cong (d_m - d) + (\dot{d}_m - \dot{d}) = e + \dot{e} \quad (22)$$

where $\dot{d}_m$ and $\dot{d}$ represent the first derivatives of the reference trajectory and the mover position of the LUSM, respectively.

4. Circuits design on FPGA chip

FPGA-based control system for a motion control stage is shown in Fig. 3. A linear scale with resolution 1 μm is adopted to detect the position of the moving table. To implement the RWNN control system, the timing control module, encoder interface module, and the RWNN control module are realized on the FPGA chip, respectively. The sampling interval, i.e. the execution interval, of the control algorithm is 1.366ms (732Hz). Two D/A converters are utilized to display the reference trajectory d_m, the mover position d, the control effort V and the tracking error e alternately on the oscilloscope. The entire I/O port for this chip includes 2 pins for the input ports and 36 pins for the output port. Moreover, 6076 out of 10240 flip-flops (59%) have been used in the FPGA chip. Furthermore, the circuits and control algorithm in the FPGA are developed using VHDL by a personal computer as the development system. In the development of the VHDL codes for a 12-bits FPGA processor, by using fractional numbers between –1 and 1 with the Q-format representation, the results of multiplication can be easily handled since the product of two numbers is always in the same range. Besides, all the sine, multiplier and divider are implemented using available intellectual properties (IPs).

4.1. Encoder interface module

The block diagram of encoder interface module is shown in Fig. 4(a), which consists of timing control, two digital filters, a decoder, an up-down counter, a register, a command generator and one adder. The function of the encoder interface is to obtain the position and speed values of the mover. The position signal d can be obtained using the PLS and DIR signals through up-down counter. Moreover, the command generator includes periodical sinusoidal IP and periodical trapezoidal IP in order to generate the reference trajectory d_m. Furthermore, the resolution of the encoder is 1mm = 1000 digital value at the sampling frequency 732Hz.

4.2. RWNN control module

To implement the control law effectively, the

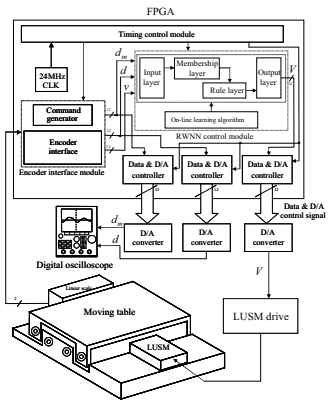

Figure 3. FPGA-based control system for motion control stage using LUSM drive.

RWNN control module is divided into five parts which are shown in Figs. 4(b) to 4(f): 1) Figure 4(b) shows the block diagram of the input layer, using d_m, d, $O_1^{(1)}(k-1)$ and $O_2^{(1)}(k-1)$ to obtain e, $\dot{e}$, $O_1^{(1)}(k)$ and $O_2^{(1)}(k)$; 2) Figure 4(c) shows the block diagram of the membership layer based on (3)-(5). 3) Figure 4(d) shows the block diagram of rule layer based on (6)-(12). 4) Figure 4(e) shows the block diagram of the output layer based on (13) and (14). 5) Figure 4(f) shows the block diagram of the on-line learning algorithm utilized to achieve the update laws of the connective weights between the rule layer and the output layer based on (16), (17), the translations in the membership layer based on (18), (19) and the dilations in the membership layer based on (20), (21).

5. Experimental results

The control objective is to control the mover of the LUSM to move periodically according to the reference trajectories including sinusoidal and trapezoidal commands using the RWNN controller. Moreover, two test conditions are provided in the experimentation, which are the nominal condition and the parameter variation condition. The parameter variation condition is the addition of one iron disk with the mass 3.66kg on the moving table.

The control objective is to control the mover to move ±1 mm periodically for sinusoidal reference trajectory and 1mm periodically for trapezoidal reference trajectory. Figures 5 to 8 depict the experimental results of the command tracking due to the periodical sinusoidal and trapezoidal reference trajectories of the proposed RWNN control system at nominal condition and parameter variation condition, respectively. From the experimental results, good

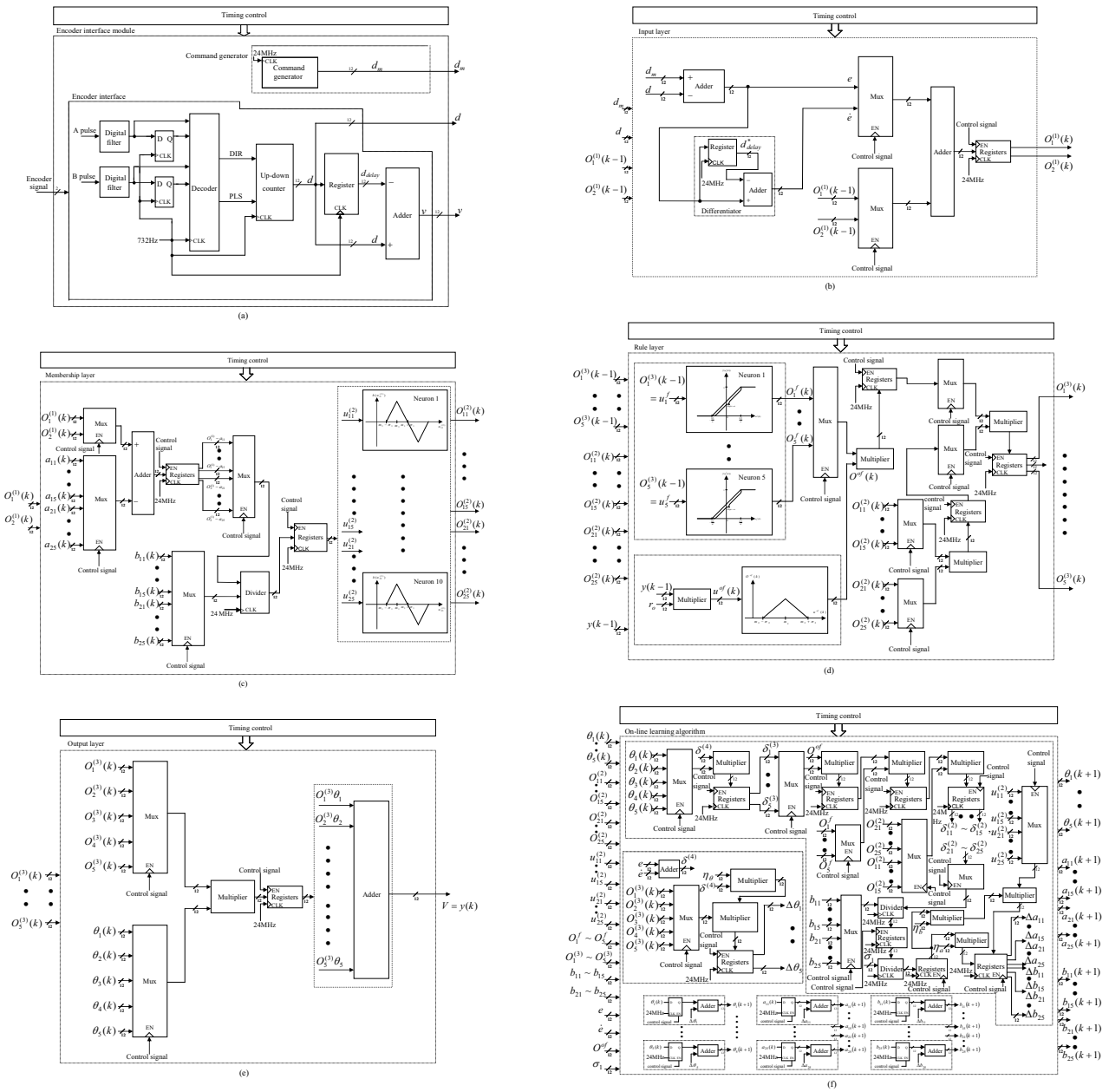

Figure 4. Circuits design on FPGA: (a) encoder interface module; (b) input layer in RWNN control module; (c) membership layer in RWNN control module; (d) rule layer in RWNN control module; (e) output layer in RWNN control module; (f) on-line learning algorithm in RWNN control module.

tracking responses of the mover can be obtained at both the nominal and the parameter variation conditions for the proposed RWNN controller as shown in Figs. 5(a), 6(a), 7(a) and 8(a). It also depicts that the proposed FPGA-based RWNN control system has effective hardware on-line learning ability of the network parameters and is robust with regard to the parameter variation.

6. Conclusions

Since the dynamic characteristics of the LUSM are non-linear and time-varying and the precise dynamic model is difficult to obtain, an FPGA-based RWNN control system has been proposed to control the mover position of the LUSM to achieve high-accuracy position control in this study. First, the LUSM drive system was introduced. Then, the proposed RWNN were described in detail. Moreover, according to the

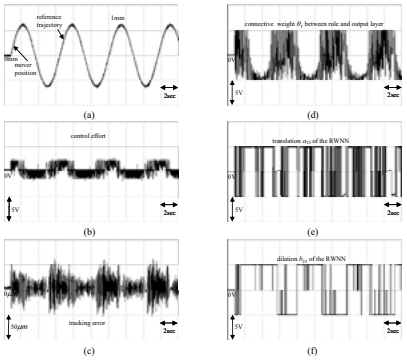

Figure 5. Experimental results of RWNN control system for periodical sinusoidal reference trajectory at nominal condition: (a) tracking response; (b) control effort; (c) tracking error; (d) connected weight θ_3 ; (e) translation a_{23} ; (f) dilation b_{23} .

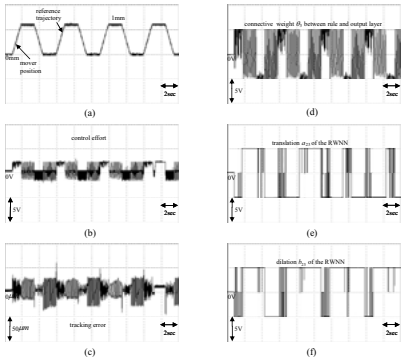

Figure 6. Experimental results of RWNN control system for periodical trapezoidal reference trajectory at nominal condition: (a) tracking response; (b) control effort; (c) tracking error; (d) connected weight θ_3 ; (e) translation a_{23} ; (f) dilation b_{23} .

on-line learning algorithm, the connective weights, translations and dilations of the RWNN are trained on-line to obtain the control effort using FPGA-based hardware circuits. Finally, the effectiveness of the proposed low-cost high-performance FPGA-based LUSM drive has been confirmed by some experimental results.

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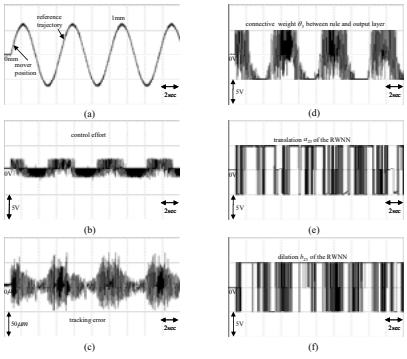

Figure 7. Experimental results of RWNN control system for periodical sinusoidal reference trajectory at parameter variation condition: (a) tracking response; (b) control effort; (c) tracking error; (d) connected weight θ_3 ; (e) translation a_{23} ; (f) dilation b_{23} .

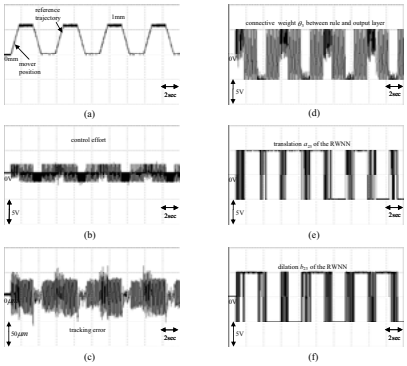

Figure 8. Experimental results of RWNN control system for periodical trapezoidal reference trajectory at parameter variation condition: (a) tracking response; (b) control effort; (c) tracking error; (d) connected weight θ_3 ; (e) translation a_{23} ; (f) dilation b_{23} .