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# Neural Recording Front-End Designs for Fully Implantable Neuroscience Applications and Neural Prosthetic Microsystems

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*Abstract*—**An implantable neural recording front-end has been designed in two versions. The first is a multi-channel signal-conditioning ASIC for use with any neural recording probe technology. This ASIC was implemented in a commercial 0.5µm CMOS process, includes 16 parallel amplifier channels, and measures 2.3mm$^2$. The amplifiers have a gain of 59.5dB, a high cutoff frequency at 9.1kHz and consume 75µW per channel. The low cutoff frequency is independently tunable on each channel to accept or reject field potentials. This chip is small enough to be chronically packaged for experiments in awake behaving animals or it can be integrated into a fully implantable neural recording microsystem. The second version of the front-end is a neural recording probe with integrated signal conditioning circuitry on the back-end implemented in a 3µm CMOS process. This version dissipates 142µW and includes 64 to 8 site selection, 8 per-channel amplifiers each having a gain of 50.2dB, a tunable low cutoff frequency, and a 7kHz upper cutoff frequency. Real-time site impedance and circuit testing has been integrated in this design.**

*Keywords*—**Neural recording amplifiers, neural probes, neural prosthetics, microsystems**

## I. INTRODUCTION

Neural interfaces in the form of implantable microsystems are emerging as one of the most important and rapidly growing technologies for neuroscience and neural prosthetics. State-of-the-art applications include prosthetics aimed at suppressing the debilitating effects of Parkinson's disease and epilepsy, motor control of prosthetic limbs, improving cochlear implants to achieve higher frequency resolution, providing localized drug delivery, and replacing damaged retinas. The chronic functionality of these systems requires advances in robust system design, integration, packaging, and biocompatibility.

In particular, implantable neural recording front-ends are key to these microsystems and to neuroscience experiments involving awake behaving subjects. A schematic of a neural recording system is shown in Fig. 1. The front-end includes recording electrodes and signal conditioning circuitry (site-selection, amplification and filtering). A number of electrode technologies are currently available [1-4] but *implantable* signal conditioning circuitry is still in development and only large external signal conditioning technologies are currently offered (e.g., from Plexon Inc. and Tucker Davis Technologies). These large front-ends are not feasible for implantable devices and

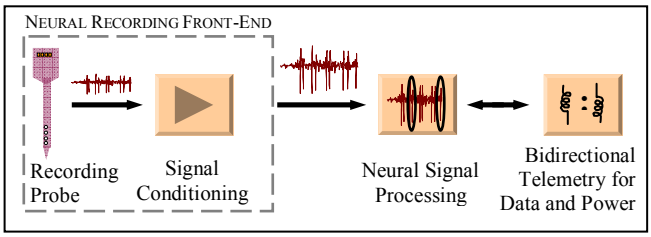



Fig. 1: Diagram of a neural recording system.

furthermore their use is limited in experiments involving freely moving subjects. State-of-the-art implantable front-end designs include signal conditioning ASICs (Application Specific Integrated Circuits) [5-7] and recording arrays with integrated circuitry [8-9]. The ASICs can be used with any electrode technology but this approach requires hybrid packaging of the ASIC with the electrode array. Integrating the circuitry onto the backend of the probe (referred to as an active probe) not only eliminates the hybrid packaging and suppresses sensitivity to interconnect (cable) leakage but also improves signal quality since externally coupled noise is significantly reduced. In addition, active probes can offer real-time testing of site impedance and circuit operation during in-vivo experiments. However, active probe availability is still very limited.

This work presents band-tunable neural recording amplifiers designed in a commercial process and integrated onto a small multipurpose chip having parallel recording channels. The amplifier designed in this work has the largest gain at comparable power levels and smallest per-channel die area ever reported for monolithic neural recording amplifiers [5-9]. A neural recording probe is also presented having integrated signal conditioning circuitry along with real-time site and circuit testing capability.

## II. DESIGN

The application specific integrated circuit (ASIC) chip includes 16 parallel neural recording amplifier channels designed in a commercial 0.5µm CMOS technology. The active probe design features 64-to-8 site selection, followed by 8 parallel amplifier channels. Self-testing capability is included on the active probe so that there are three modes of operation. In the normal operation mode the recorded signal from the selected site is amplified. The other two modes of operation are used for testing purposes where the amplifiers

can be bypassed to measure the selected site impedances or a test signal can be sent to simultaneously characterize all amplifier channels allowing the user to set the tuning voltage and compensate for random offsets.

The neural recording amplifiers, both on the ASIC and on the active probe, are based on a two-stage architecture with a differential input pair and a gain stage [10] as shown in the open-loop configuration in Fig. 2. The input stage is designed using PMOS transistors since the dominant noise source in the bandwidth of interest (flicker noise) is lower for PMOS devices compared to NMOS devices. The Miller compensation technique is used with a nulling series resistance implemented using NMOS and PMOS transistors for stable operation in feedback mode. Since the NMOS device has a lower overdrive voltage, an NMOS source follower is used in the gain stage to achieve maximum output swing. The recorded signals are capacitively-coupled to the input of the amplifier to reject the dc polarization of the electrode. Therefore, a capacitor ratio is used to set the gain in a negative feedback loop. The low-frequency cutoff is tunable using a voltage to control the impedance in the feedback loop, allowing the selection/rejection of slow wave potentials.

The closed-loop configuration of an amplifier on the ASIC is shown in Fig. 3 and the circuit block diagram of the active probe is shown in Fig. 4. The active probe amplifiers are cascaded to achieve a large gain but the disadvantage with this approach is that each stage has random offsets due to process variations. Since the gain is fixed, the random offsets can cause the output to be saturated. Attempting to null the offset of each stage using the non-inverting input can be challenging since the random offsets of each amplifier can be in opposite directions. To overcome this challenge the ASIC amplifiers were designed to achieve the required gain in a single block. Eliminating the cascading of

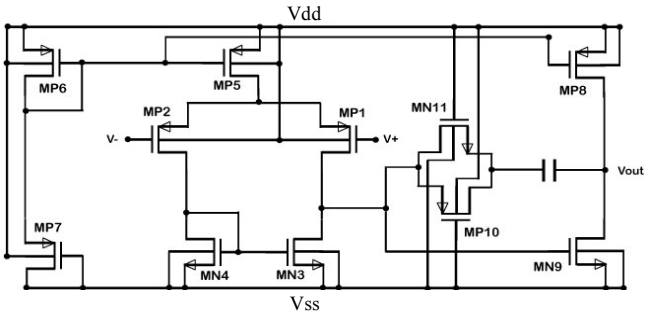



Fig. 2: Neural recording amplifier architecture in open-loop configuration.

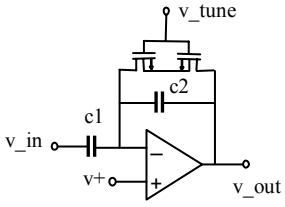



Fig. 3: ASIC closed loop amplifier configuration with band-tunability and DC rejection.

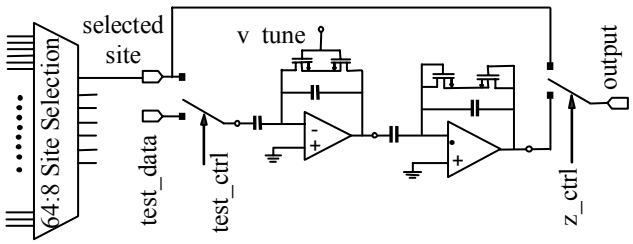
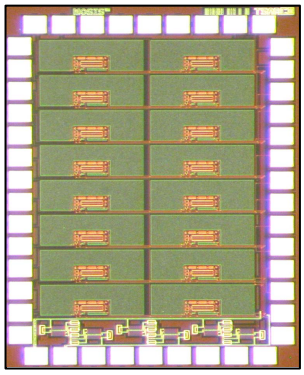



Fig. 4: Block diagram showing closed loop amplifier configuration and the testing capability included on the active probe front-end design.

two amplifier blocks not only helps with the random offset but also results in almost half the power consumption per channel.

## III. Results

A picture of the amplifier ASIC having 16 channels along with the per-channel performance summary is shown in Fig. 5. The measured transfer curves for an ASIC amplifier showing the gain and the low-frequency tuning capability are given in Fig. 6 as the tuning voltage is varied. The gain of each channel was measured to be 59.5dB while the low cutoff frequency is tunable to below 10Hz with a resolution of 5mV. The measured low cutoff frequency as a function of the tuning voltage swept over a 70mV range is shown in Fig. 7. The high cutoff frequency was measured to be 9.1kHz. Each channel consumes 75µW operating at ±1.5V. Other features of the ASIC include laser trimmable links integrated on the chip to set the operating tuning voltage and to compensate for dc offsets. This allows circuit operation without the need for off-chip components or external control, which is a requirement for a fully implantable device in addition to low-power and small size. The total area consumed by the chip is 2.3mm$^2$. As seen in Fig. 5, most of the die area is taken by the large feedback capacitor used to set the gain. The in-vitro testing results for this amplifier using a pre-recorded neural input signal are shown in Fig. 8. The inset shows a close-up of the input signal and amplified output signal (inverted). As seen in this figure the spike shape and latency are well preserved;



| | |
|---|---|
| Gain | 59.5 |
| Low frequency cutoff | <10Hz |
| Low frequency tunability | yes |
| High frequency cutoff | 9.1kHz |
| Input referred noise (10Hz-10kHz) | 8µVrms |
| Power | 75µW |
| Supply voltage | ±1.5V |

Fig. 5: Neural recording amplifier ASIC with 16 channels (chip area: 2.3mm$^2$) and measured performance summary per channel.

furthermore, it is apparent that the high-frequency noise on the spike input is filtered from the output signal.

The circuitry on the active probe was designed in the University of Michigan 3µm CMOS process and integrated with the dissolved-wafer probe process [11]. A picture of the fabricated probe having 64 recording sites (8 on each shank) is shown in Fig. 9, including a close-up of the back-end circuitry. The site-selection pattern includes a selection of 8 channels, either vertically on the shank, horizontally across the 8 shanks, or a block of 4x2 (4 laterally and 2 vertically) adjacent sites. The recorded signals from each of the 8 selected sites are amplified with a measured gain of 50.2 dB and filtered from a tunable low-frequency cutoff to 7kHz. Each amplifier on the active probe consumes 142µW and operates at ±1.5V. To demonstrate the self-testing capability included on the active probe, a 500µVp-p square wave and sine wave at 1kHz were applied to the "test_data" and "selected site" nodes of Fig. 4, respectively. There are three modes of operation, as shown in Fig. 10. To test the amplifier operation, "Test_ctrl" and "Z_ctrl" are set to the high state and a test signal can be sent through the amplifier to the output pad. The second mode of operation allows the user to measure the site impedance when "Z_ctrl" is set to the low state. The normal mode of operation, i.e., amplify the recorded signal from the site, is selected by setting "Test_ctrl" and "Z_ctrl" to the low and high states, respectively.

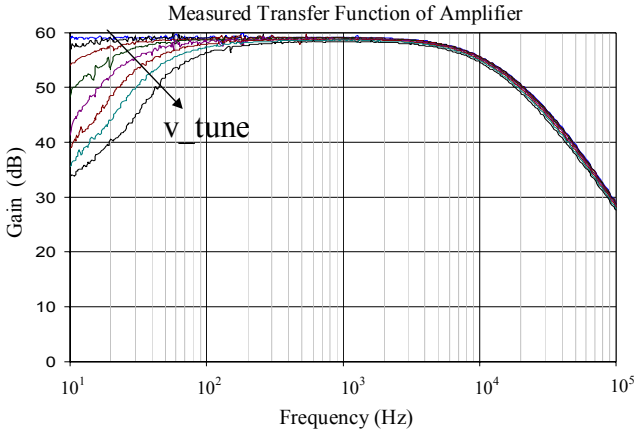



Fig. 6: Measured transfer curves for an amplifier on the ASIC as the tuning voltage is swept over 70mV range. The midband gain is 59.7dB and the high cutoff frequency is 9.5kHz.

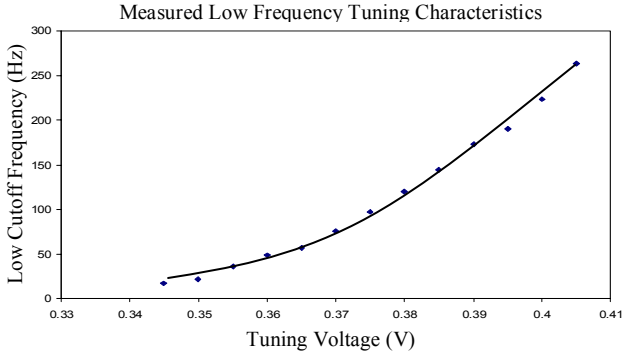



Fig. 7: Measured low frequency cutoff frequency as a function of the tuning voltage.

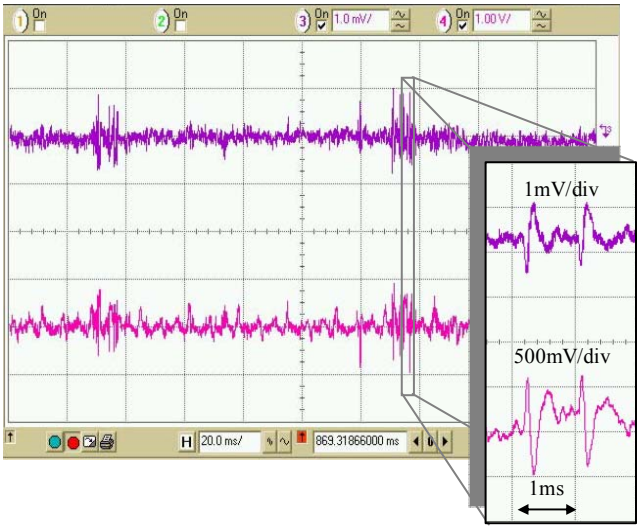



Fig. 8: Test results for an amplifier on the ASIC chip using pre-recorded neural data.

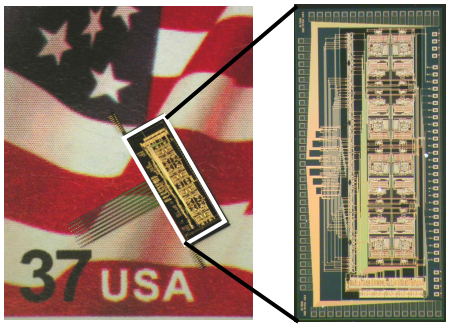



Fig. 9: An active probe with monolithically integrated circuitry capable of site-selection, amplification/filtering and real-time site-impedance testing capability.

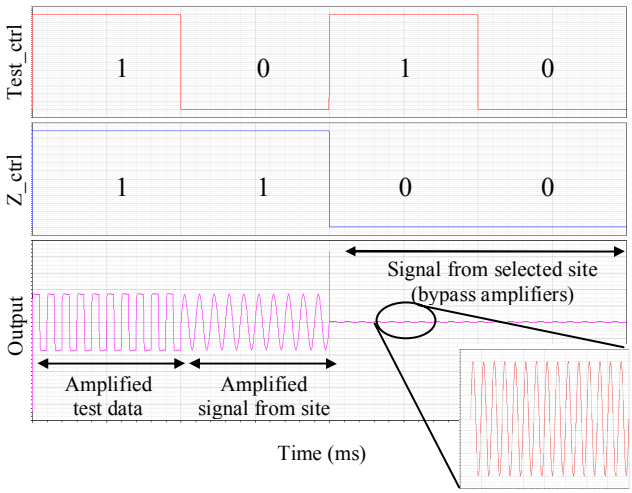



Fig. 10: Self-testing capability included on the active probe.

Table 1: A comparison of monolithically integrated neural recording amplifiers designed in CMOS

| | Harrison [5] (2003) | Olsson [9] (2003) | Horiuchi [6] (2004) | Mohseni [7] (2004) | This work |
|---|---|---|---|---|---|
| Gain | 39.5 dB (94x) | 38.9 dB (88x) | 42.5 dB (133x) | 39.3 dB (92x) | 59.5dB (950x) |
| Low freq. cuttoff | 0.025Hz | < 1Hz | 22 Hz | dc | < 10Hz |
| Tunable low frequency | yes | yes | yes | yes | yes |
| High freq. cuttoff | 7.2 kHz | 9.9 kHz | 6.7 kHz | 9.1 kHz | 9.1kHz |
| Input Referred Noise Voltage | 2.2μVrms | 9.2μVrms (100Hz -10kHz) | 20.6μVrms (10Hz -10kHz) | 7.8μVrms (0.1-10kHz) | 8μVrms (10-10kHz) |
| Input Offset Voltage | N/A | -511μV | N/A | 811μV | 1mV |
| Supply Voltage | ±2.5V | ±1.5V | 1.5V | 3V | ±1.5V |
| Power Consumption | 80μW | 68μW | 0.8μW | 115μW | 75μW |
| Die area per channel | 0.160mm$^2$ | 0.177mm$^2$ | N/A | 0.107mm$^2$ | 0.072mm$^2$ |
| Process | 1.5μm CMOS | 3μm CMOS | 1.5μm CMOS | 1.5μm CMOS | 0.5μm CMOS |

## IV. Discussion

The currently available commercial neural recording systems are considered *macrosystems*. For prosthetic applications and many other experiments with freely behaving subjects, it is necessary to develop *microsystems*. Neural recording front-end performance can be a bottleneck in microsystems design. The challenge here is to develop robust probe structures and recording amplifiers. While probe structures are widely available by now, work on implantable neural recording amplifiers is still relatively limited. Table 1 compares the performance of neural recording amplifiers based on fully-integrated designs (i.e., using no off-chip components). All of the amplifiers compared in Table 1 are designed in CMOS and consume only microwatts of power per channel. The design in this work provides the largest overall gain at comparable power levels and consumes the smallest area per channel. The small feature size used to design this ASIC is advantageous when integrating the entire microsystem circuitry onto a single chip. This will greatly simplify system integration and validation as well as resulting in a very compact system.

## VI. Conclusion

In this work we have designed two versions of an implantable neural recording front-end. These front-end designs have a high gain, filter the signals in signal bandwidth, and consume very little power. The two designs presented here provide a variety of options for neurophysiological studies. Depending on the complexity of the experiments, they can be used simply as front-ends or can be integrated into a compact low-profile microsystem.


### ACKNOWLEDGMENT

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