Proceedings of the 28th IEEE
EMBS Annual International Conference
New York City, USA, Aug 30-Sept 3, 2006

The Design and Testing of an Epi-Retinal Vision Prosthesis Neurostimulator Capable of Concurrent Parallel Stimulation

N. Dommel, *Student Member, IEEE*, Y.T. Wong, *Student Member, IEEE*, P.J. Preston,
T. Lehmann, *Member, IEEE,* N.H. Lovell, *Senior Member, IEEE* and G.J. Suaning *Member, IEEE*

Abstract— **An application specific integrated circuit (ASIC) neurostimulator capable of stimulating multiple electrodes in unison has been designed and tested. The ASIC utilizes multiple matched current sinks and sources to provide localized stimulation and is designed to drive electrodes organized in a hexagonal mosaic. This organization allows each stimulating electrode to be surrounded by up to six return electrodes, effectively isolating each stimulation site. The ASIC was manufactured using a high-voltage complementary metal-oxide-semiconductor process, which allows up to 20V to be applied across the circuitry. This provides the greatest versatility for testing with electrodes and tissues of varying impedances *in-situ* and allows the device to be used in other neurostimulation applications such as functional electrical stimulation. The design has been thoroughly tested and meets all the design specifications.**

I. Introduction

MACULAR degeneration and retinitis pigmentosa are two of the leading causes of blindness in the western world. These diseases destroy the light transducing elements of the eye (the photoreceptors), but can leave the retinal ganglion cells and afferent nerve fibers intact [1-3]. In these situations, due to the death of the photoreceptors, no signals are conveyed from the retina to the visual cortex even if the neural pathways are still able to conduct signals. A vision prosthesis can intervene with electrical stimulation at any location proximal to the damaged tissue. In recent years efforts have been focused on three intervention sites: the visual cortex, the optic nerve, and the retina.

Brindley and Lewin stimulated the visual cortex, with patients reporting sensations of light (phosphenes) [4]. Further research in this area has been conducted by Dobelle [5], [6] and Troyk [7]. The main drawbacks of intervening at the visual cortex is the relatively unknown spatial mapping of the visual cortex to the visual field [8], and the difficulty of long-term electrode implantation in the cortex. Veraart *et al.* have stimulated the optic nerve with success in a recent patient [9]. Similar to the visual cortex approach, there is relative uncertainty between the mapping of the optic nerve fibers to the visual field. To address the problem of mapping cortical or optic nerve stimulation events to the visual field, techniques are employed where elicited phosphene positions on the visual field are mapped to given stimulation events and parameters.

The third intervention site, the retina, is the target of the neurostimulator described in this paper. Several groups [10-12], have focused their research efforts on electrically stimulating surviving ganglion cells from the previously mentioned diseases. While results from human and animal trials [12], [13] have been successful, Marc and Jones [14], [15] have shown that over time neural "re-wiring" occurs amongst the inner retinal neurons, after outer retinal neural cell death. This "re-wiring" can hinder the elicitation of electrically evoked responses. The main advantage of the retinal stimulation approach is the known spatial mapping of the retina to the visual field [16], although surgical implantation and fixation is likely to prove more difficult. For further reading on the various approaches of vision prostheses, the reader is directed to [17].

From the above-mentioned work, it can be roughly estimated that for each additional electrode that a neurostimulator can provide, an additional phosphene will be elicited in a subject. Phosphene numbers, and hence electrode numbers, are critical to the success of a vision prosthesis in restoring useful vision. In addition, the effective refresh or frame rate of the neurostimulator has been shown to be important for good perceptual results.

To investigate how phosphene numbers affect visual perception, several groups have simulated prosthetic vision on normal sighted subjects. Hallum *et al.* have found that by increasing phosphene numbers from 100 to 400, the number of faces recognized by subjects improved from 63.8±11.5% to 90.7±6.8% when only the size of the phosphenes are modulated, and from 64.1±16.7% to 87.8±7.4% when only the intensity of the phosphenes are modulated [18]. Simulations by Cha *et al.*, where an array of 25 x 25 phosphenes occupied 1.7˚ of the foveal visual field, showed that reading rates of 100 words/min were achievable [19], [20]. Further studies by Chen *et al.* have found that when phosphenes are arranged in a hexagonal mosaic, there is an advantage in the detection of the orientation of a Landolt C

N. Dommel, Y.T. Wong, P.J. Preston, G. J. Suaning, and N.H. Lovell are with the Graduate School of Biomedical Engineering, University of New South Wales, Sydney NSW 2052, Australia. N.H. Lovell is also with National Information and Communications Technology Australia (NICTA), Eveleigh, NSW 1308, Australia. G. J. Suaning is also with the School of Engineering, University of Newcastle, Callaghan, NSW 2444 Australia. T. Lehmann is with the School of Electrical Engineering and Telecommunications, University of New South Wales, Sydney, NSW 2052 Australia. This research was supported by funding from the Australian Federal Government (Department of Education, Science, and Training and the Australian Research Council), Retina Australia, the Clive and Vera Ramaciotti Foundation and the Government of Canada (Natural Sciences and Engineering Research Council of Canada).

optotype over rectangular arrays of phosphenes [21].

To ensure that the images conveyed by a prosthesis are continuous (i.e. do not flicker), the stimulations used to convey phosphenes need to occur above a threshold frequency, commonly referred to as the critical flicker fusion (CFF) frequency. For a normal sighted person this frequency at normal luminance has been reported to vary from 20-40Hz [22]. For a subject where vision is conveyed solely through stimulation of the retinal neurons, this frequency has been reported to be higher than that of the normal observer at 40-50Hz [16]. An epi-retinal prosthesis should therefore be designed to be able to stimulate at frequencies above 50Hz.

Just as there are different intervention sites, the neurostimulators used to generate the electrical stimulation also vary. The majority of neurostimulators interleave a single current source or sink across multiple electrodes. This is the case in cochlear implants, where the Continuous Interleaved Sampling (CIS) and Spectral Peak (SPEAK) speech processing strategies utilize such a serial stimulation mode [23]. The interleaving of a single stimulator works well for the cochlear implant where there are small electrode numbers (below 30 [24]). In vision prostheses, the electrode numbers required to provide useful vision (over 500 [19]) are too high to be able to interleave a single stimulator at an acceptable frequency. For example, if a single stimulation event lasts 1ms (as reported in [13]) then 200 electrodes can be stimulated at a maximum rate of 5Hz. To overcome this problem, multiple stimulators used simultaneously will increase the stimulation rate.

The main drawback of activating multiple electrode sites in unison is electrical cross-talk. In conventional bipolar stimulation, with one stimulating (active) electrode and one return (indifferent) electrode, charge has only one electrode to enter via and one electrode to return through. By increasing the number of stimulating and return electrode pairs operating simultaneously, the current that enters through one electrode may now return through any of the return electrodes and not necessarily through its paired electrode as desired. This reduces the ability to inject localized current into tissue due to current diversion between separate stimulation sites. Investigations by Lovell *et al.* have shown that significant current diversion or cross-talk occurs when multiple stimulation sites are active and injecting different amounts of current [25]. This cross-talk can also result in charge imbalance at the end of a stimulation sequence that could, if not dissipated, damage neural tissue.

To reduce the effects of cross-talk during simultaneous stimulation, the neurostimulator described in this paper uses a unique arrangement of electrodes and both a current source and sink during stimulations. This neurostimulator forms part of an electric circuit between the stimulus power supply ($V_{stimulus}$) and circuit ground (V_{ss} – the lowest circuit potential in the neurostimulator). The circuit includes the current source and sink, the electrode/tissue interface impedance ($Z_{E/T}$) and the tissue impedance (Z_T). The current source requires a minimum voltage between its output and $V_{stimulus}$ for it to operate (V_{source}). Similarly, the current sink requires a minimum voltage between its output and V_{ss} to operate (V_{sink}). As illustrated in Fig. 1, the voltage compliance (V_{comp}) of a current source is defined as the difference between $V_{stimulus}$ and V_{source}. If the voltage at the output of the current source were to increase above this V_{comp}, the current source would cease to operate (it is out of compliance). Similarly, for the current sink, it's V_{comp} is defined as the voltage difference between $V_{stimulus}$ and V_{sink}. For the current sink to operate, the voltage at its output must remain above V_{sink}.

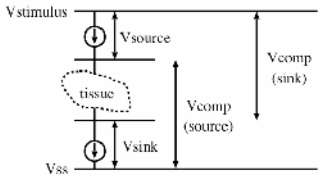

Fig. 1. Compliance voltage of a current source and sink.

$Z_{E/T}$ is dependent upon: electrode geometry; stimulation frequency; factors affecting the electrochemical process such as ion concentrations and surface properties of the electrodes, and tissue surrounding the electrodes [26]. Z_T is dependent upon the patient's anatomy and the tissue conductivity coefficients [26]. Studies on cochlear implant patients have shown that $Z_{E/T}$ significantly increased in the first month of implantation, likely due to fibrous tissue encapsulating the electrode increasing the resistive component [27]. Therefore, the values of $Z_{E/T}$ and Z_T are not necessarily known prior to device implantation, and will change during implantation life due to biological processes at the electrode-tissue interface. V_{comp} is dependent upon the current source and sink design. The designer chooses $V_{stimulus}$; its value is limited to the maximum voltage allowed across the circuit components used to implement the neurostimulator.

Two parameters are under direct control of the designer and can be chosen to provide the greatest flexibility of the neurostimulator *in-situ*: $V_{stimulus}$ can be increased and V_{comp} can be increased. The neurostimulator described herein allows for a $V_{stimulus}$ of up to 20V, and was designed with a large V_{comp}. 20V is classified as a high-voltage (HV) in complementary metal-oxide-semiconductor (CMOS) design and manufacturing processes. Although the CMOS process allowed for a $V_{stimulus}$ of up to 20V, a higher $V_{stimulus}$ increases the power consumption; therefore, careful design is required to limit the circuit components connected to $V_{stimulus}$.

The drive to build this neurostimulator was to provide a research tool to allow investigations into the effects of simultaneous stimulations on neural tissue. The neurostimulator is targeted primarily for epi-retinal stimulation. A HV CMOS process was used to implement the ASIC neurostimulator, to provide the greatest versatility in choice of electrode sizes and geometries (i.e. potentially large range of $Z_{E/T}$ and Z_T) during animal studies.

This paper presents the design specifications, ASIC functionality, design considerations and implementation details, and simulation and measured results for an epi-retinal prosthesis neurostimulator. This neurostimulator is the first design which allows concurrent parallel stimulation with hexagonally organized guard electrodes.

II. Methods

A. Specifications

The ASIC neurostimulator was designed to meet the following specifications:

- Capable of exciting retinal ganglion cells in animal models and humans, and to be flexible enough to operate in other functional electrical stimulation (FES) applications
- Capable of being controlled and powered through a radio-frequency (RF) link
- Inherently safe and able to handle corrupt data instructions or partial data streams
- Able to provide multiple stimulations simultaneously
- Small enough to implant in an eye (maximum dimensions of 6mm by 6mm)
- Easily scalable using a bus architecture to cater for a larger number of electrodes
- Low cost
- Able to withstand up to 20V across the output driver circuitry, to allow for stimulation with electrodes of various geometries and sizes and varying impedances at the electrode-tissue interface

B. Functionality

The following functionality has been included in this neurostimulator design to allow it to operate as the stimulator for an epi-retinal prosthesis, and to allow testing of simultaneous stimulations in neural tissue.

1) Push-Pull Stimulation

The primary stimulation mode involves connecting the stimulating electrodes to a current sink and the return electrodes to a current source (as shown in Fig. 2). This is opposed to conventional stimulation techniques where either a current sink is connected to the stimulating electrode and the return electrodes are connected to $V_{stimulus}$, or where the stimulating electrode is connected to V_{ss} and a current source is connected to the return electrode. The use of a current source and sink together has been chosen as the default mode of stimulation as it allows for better localized current injection and charge balancing during simultaneous stimulation [28]. The neurostimulator is also capable of providing stimuli using either a current sink only or a current source only, as described above; these modes are chosen through the RF data stream used to program the ASIC.

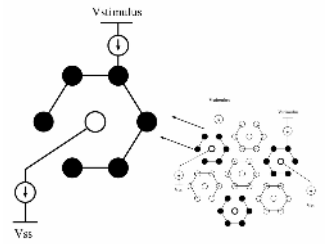

Fig. 2. Electrodes organized in a hexagonal arrangement with simultaneous stimulations driven by the dual use of current sources and sinks.

2) Hexagonal Electrode Arrangements

Conventional bipolar stimulation utilizes a pair of electrodes with one electrode acting as the stimulating electrode and the second electrode acting as the return electrode. This is illustrated in the left panel of Fig. 3 with current entering one electrode and recovered from the other. To reduce the effect of electrical cross-talk that can occur when multiple electrodes are active in unison, the return electrodes are connected together to form a guard ring of electrodes, surrounding each stimulating electrode. This effectively isolates each stimulating electrode from the others (right panel Fig. 3). The electrodes are laid out in a hexagonal shape, as this provides the densest packing and allows for seamless expansion of electrode numbers. The neurostimulator designed in this paper allows the stimulating electrode to be centered on any one of the seven unique electrode positions.

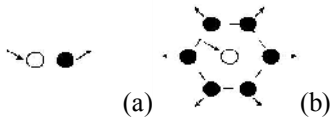

Fig. 3. Stimulating electrode organizations. (Left panel) Conventional paired electrodes with current entering the white electrode and returning through the black electrode. (Right panel) Hexagonally arranged electrodes with current entering the centre white electrode and returning through the black surrounding electrodes (all connected together). By surrounding the centre electrode with the connected guard return electrodes, the injected charge is kept to a localized region.

Models developed by Dokos *et al.* have showed that the secondary activations that can occasionally occur during the second phase of stimulation (anodic phase) when a single return electrode is used are significantly reduced when the current is returned through multiple electrodes [29]. The second phase of stimulation is intended to recover the charge injected in the first phase (cathodic phase), so it is desired to eliminate these unwanted activations. A technique that is commonly used to remove secondary activations is that of anodic scaling (described in further detail in sub-section 4). This can, however, increase stimulation durations significantly, reducing effective stimulation rates. By utilizing six electrodes for each stimulation site, the chance of secondary activations are significantly reduced.

3) Stimulation Current Levels

The neurostimulator has been designed primarily for vision prosthesis purposes, but a high current range (130μA – 4.03mA) has been implemented to allow the neurostimulator to be used for other FES purposes. For

vision prosthesis applications, two current ranges, 20μA – 620μA and 40μA – 1.24mA (default), have been implemented to allow the versatility of experimentation with different animal models and electrode sizes and geometries. To safeguard the accidental selection of the high current range for vision prosthesis applications, and hence risking tissue damage, this range can only be enabled through connection of a specific neurostimulator pin to the logic high voltage (V_{dd} – 3.3V).

4) Anodic Scaling

A balanced biphasic stimulation waveform is typically used in the electrical stimulation of neural tissue as it minimizes the chance that charge will accumulate over time in the excited tissue [30]. In such a waveform, an equal amount of charge is injected in the cathodic phase (to elicit an action potential) as is recovered in the anodic phase. By recovering the charge injected in the anodic phase at a lower current setting for a longer time period, the probability of eliciting an undesired secondary activation is reduced significantly [31]. This is accomplished by left-shifting the digital-to-analog converter (DAC) current setting bits for each current source and sink by a certain number of bits, and extending the stimulation time by the same ratio at the end of the cathodic phase. This allows the DAC a longer time to settle on the new current level before the onset of the anodic stimulation phase.

5) Monopolar Stimulation

The development of this neurostimulator is primarily as a research tool. While this neurostimulator is designed to operate multiple stimulating electrodes surrounded by rings of return electrodes, a monopolar stimulation mode has been included to allow for comparisons of physiological and psychophysical events using both bipolar and monopolar stimulation. In monopolar stimulation, multiple electrodes are active simultaneously, but only one return electrode sinks or sources the total charge, depending on the stimulation phase.

6) Serial Mode Stimulation

The authors have highlighted that simultaneous stimulations will increase the effective stimulation rate over serial mode stimulation. Serial mode stimulation is where one electrode site is active sequentially followed by another. The neurostimulator has the ability to stimulate in both parallel and serial modes, to allow for comparisons between the perceptual outcomes using each mode. Serial mode stimulation is enabled through the RF data programming commands.

7) Scan Chain Test Logic

Once the ASIC has been manufactured, no internal controllability or visibility into the circuit is possible. Sequential logic circuit blocks are particularly difficult to test, as obtaining a desired output value at a particular flip-flop could require thousands of state changes. To allow for greater visibility and controllability in our design, key flip-flop circuit blocks were replaced with scan equivalent versions. The scan flip-flop allows for a regular or scan test clock to control the clock input to the flip-flop. In addition, the scan flip-flop allows for a regular or scan-specific data input to be used. The purpose for using scan flip-flops is to allow a particular data stream to be loaded at the input of each scan flip-flop. In addition, the value at a particular scan flip-flop output can be scanned out after a specific clock signal to facilitate testing of the ASIC logic [32].

8) Electrode Shorting

At the end of each stimulation sequence (cathodic and anodic phases), the electrodes can be shorted together and to a common potential, setting the pre-stimulus implant-tissue potential. This ensures the greatest voltage swing for the current sources and sinks to operate in (i.e. ensure that they are in compliance at the onset of the next stimulation event). As the neurostimulator can be configured to operate in a current sink only, current source only, or combined current source and sink mode, the electrodes need to be shorted to different potentials based on the stimulation mode. For current sink mode stimulation, the electrodes are shorted to $V_{stimulus}$. For current source mode stimulation, the electrodes are shorted to V_{ss}. For combined current source and sink mode stimulation, the electrodes are shorted to a potential set halfway between $V_{stimulus}$ and V_{ss}. In addition to setting the implant-tissue potential, the electrode shorting also allows any charge remaining in the tissue from the stimulation event to be removed.

9) RF Data Decoding and On-Chip State

The ASIC is powered and controlled by an RF data link. A simple pulse counting technique where $n = 8(n + 1)$ RF cycles is used to set up all the internal registers for a single stimulation event. While this communication protocol exhibits significant redundancies, it is more than adequate to control the number of electrodes in this system. For future neurostimulators with larger electrode numbers this protocol will become a bottleneck and will need to be altered to a more efficient schema.

To ensure that the neurostimulator ASIC will not inadvertently send stimuli to an implantee when corrupted or rogue data is sent via the RF link, a fixed protocol beginning with a unique synchronization sequence is used (Fig. 4). In addition to this, minimal state is kept across two simultaneous stimulation sequences. A reset occurs at the end of every stimulation sequence, clearing all state elements inside the ASIC with the exception of a single flip-flop that allows shorting to occur during the inter-stimulus gap.

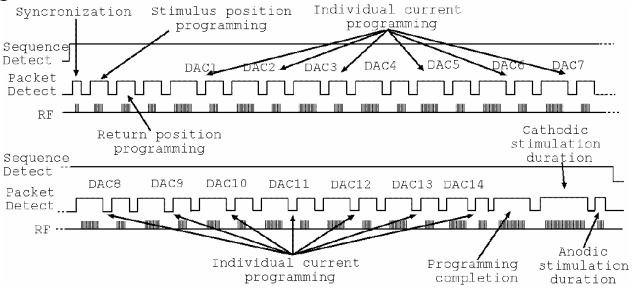

Fig. 4. RF data communication protocol.

C. Design Considerations and Implementation Details

The following section outlines the technology and tools used to design, test, and fabricate the ASIC. Methods used to reduce the size of the die and steps taken to implement the HV circuitry are provided.

1) High Voltage Circuitry

HV transistor use was limited to areas where absolutely required, as they have layout areas orders of magnitude larger than equivalent-sized low voltage (LV) transistors, and reduced transconductance compared with LV transistors [33]. HV transistors were required when the gate, drain, or source was connected to a voltage higher than V_{dd}. LV transistors were used where possible, in particular for the current mirror circuit, for the following reasons: layout area orders of magnitude smaller than equivalent HV devices; better matching for key transistors in the current mirrors [33]; lower threshold voltage (V_{th}) resulting in a higher V_{comp} [34].

The use of LV transistors in a HV environment led to considerable space savings, especially when transistor matching layout techniques were used (e.g. split common-centroid). However, during start up conditions there is a possibility that the drain-source voltage of the LV transistors could exceed their rated values, affecting device reliability or leading to device failure. To ensure all LV transistors did not exceed their rated values, several diode-connected, LV protection transistors were connected between the drain and source of the LV transistors operating in a HV environment (except those LV transistors which were already diode-connected). The protection transistors were designed such that they do not turn on during normal operation; their combined V_{th} is less than the maximum expected drain-source voltage of the LV transistor they are protecting during normal operation. If this voltage is exceeded, the protection devices are enabled.

Fig. 5 illustrates the selective use of HV transistors in the output stage of the current source and sink circuit, including the placement of LV diode-connected protection transistors.

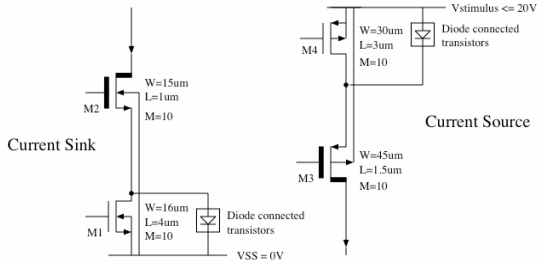

Fig. 5. Output stage of the current source and sink circuit. Transistors used: LV NMOS (M1), asymmetrical HV NMOS (M2), asymmetrical HV PMOS (M3), isolated LV PMOS (M4). Diode-connected transistors were used to protect the drain node of LV transistors in a HV environment (M1 and M4).

The layout of AMS HV transistors required additional process layers, such as HV shallow and deep *n*-wells and *p*-wells, thick gate-oxides, and isolation channels to contain substrate leakage currents. Due to the added complexity of these layouts, attempts were made to minimize the number of different HV transistor types and dimensions used.

2) Bus Structure

The ASIC utilizes a bus structure, where it can operate as a bus master or a bus slave. The bus structure and configurable master and slave modes were utilized to save considerable layout space and therefore manufacturing costs (at least 12,000 Euro). The initial circuit design consisted of a single control unit (decodes the incoming RF data) and 14 electrode clusters connected to it through an internal bus. An electrode cluster consists of a group of seven hexagonally packed electrodes, and a current source and sink.

When an ASIC is fabricated multiple copies (in this case 45) of the same design are provided from the foundry. As multiple copies were to be manufactured, the layout was reduced by removing twelve of the electrode clusters and instead, routing the bus signals to bi-directional pads. These pads are configured to be outputs in the master mode and inputs in the slave mode. The twelve electrode clusters that were removed are instead connected through these bi-directional pads using additional ASIC's. Fig. 6 illustrates how three ASIC's are connected together to control 42 electrodes. The full system consists of seven ASIC's connected through the bus driving 100 electrodes (98 electrodes in the hexagonal mosaic and two monopolar electrodes).

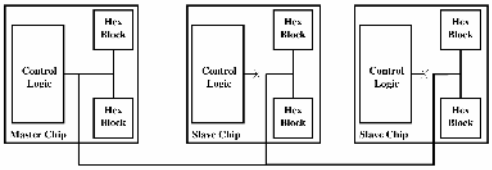

Fig. 6. Three separate ASICs connected through a bus. The ASIC on the left hand side is the bus master, the two others are slaves. This structure would allow up to 42 electrodes to be driven.

3) Technology Used

The AMS H35B4D3 4M 2P process (Austriamicrosystems AG, Schloss Premstatten, Austria) was used, with foundry access provided through Europractice IC Services (IMEC, Leuven, Belgium). The process supports multiple gate-oxide thicknesses and extended drain transistors, and allows for both LV and HV transistors on the same die. Die size of the ASIC is 2.8mm x 4.6mm, well within the dimensions of our implantable vision prosthesis device (Fig. 7). The total transistor count was over 30000.

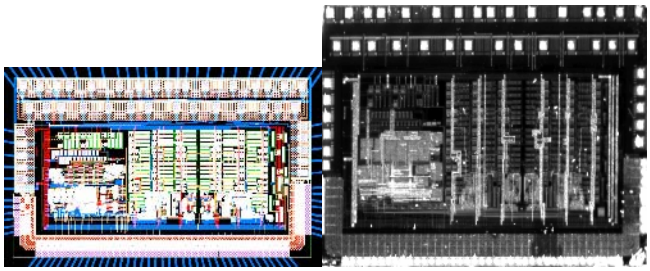

Fig. 7. Images of the neurostimulator die. (Right panel) A photograph of the die, (left panel) the layout plot of the die. Die size is 4.6mm x 2.8mm. The input/output (I/O) pads surround the perimeter of the die; high-voltage I/O on the top half (including the staggered I/O rows on the top), low voltage I/O on the bottom half.

4) Staggered Input/Output Pad Placement

There are several pad placement techniques one can use when making an ASIC. The most common is inline pad placement, where the Input/Output (I/O) pad cells are placed around the perimeter of the ASIC. Due to the larger layout size of the HV I/O pad cells compared with the LV I/O pad cells (1.8 times as wide), a staggered I/O placement technique was used for the majority of the HV I/O (top side of the ASIC, Fig. 7). In staggered I/O pad cell placement, two stacked rows of I/O pad cells are placed at the perimeter of the ASIC, with spacer cells between certain I/O pad cells to provide space for bonding wires to reach the inner pad cell row. The use of staggered I/O pad placement reduced the overall ASIC layout area, creating a smaller device for encapsulation and reducing the manufacturing costs. Despite the increased design complexity, the use of the staggered I/O pad cell placement technique proved successful, with no problems encountered during packaging or bonding to the bare die.

5) Transistor Design and Layout Matching Techniques

Transistor current and V_{th} matching in certain areas of the ASIC was very important (e.g. current source and sink matching). Circuit design and layout techniques utilized to best achieve matching are highlighted in Table I and Table II, respectively [33], [35].

TABLE I: TRANSISTOR CURRENT AND THRESHOLD VOLTAGE (V_{TH}) CIRCUIT DESIGN MATCHING TECHNIQUES USED

TECHNIQUE	REASON
Same drain-source voltage	Reduce effects of channel-length modulation
Large gate area	Reduce V_{th} mismatch, which varies inversely with the square root of the gate area
Use of thin gate-oxide (LV) vs. thick gate-oxide (HV) transistors	Reduce V_{th} mismatch due to reduced backgate doping in thin gate-oxide transistors
Equal gate lengths	Reduce effects of channel-length modulation

TABLE II: TRANSISTOR CURRENT AND THRESHOLD VOLTAGE (V_{TH}) CIRCUIT LAYOUT MATCHING TECHNIQUES USED

TECHNIQUE	REASON
Same drain-source orientation in x-y axis	Reduce transconductance mismatch due to reduced orientation-dependent carrier mobility stress sensitivity
Super-imposable asymmetrical HV transistor layout	Transistors affected equally during any photolithography shifts of the gate area
Common-centroid layout (same effective centre)	Reduce oxide thickness mismatch, stress induced gradients, and temperature gradients
Compact layout	Minimize effects of gradients
Use of dummy gates	Reduce impact of polysilicon etch rate variations
No routing or metal over active gate area	Reduce stress gradients
No contacts over active gate area	Reduce V_{th} variations

6) Design Flow

The design and simulation of the ASIC was performed using computer-aided design tools (Mentor Graphics, Wilsonville, OR, USA). The ASIC was designed and implemented in a hierarchical manner. Fig. 8 illustrates the top level design flow used to create the final ASIC layout. Fig. 9 and Fig. 10 illustrate the design flow used to implement the digital logic and analog blocks, respectively. The design flow used to implement the digital logic gate standard cells was similar to the analog block design flow. The logic gates were implemented using standard CMOS design techniques in a full-custom design approach [36].

Digital logic gate level simulations, and analog block simulations, were performed using the Eldo SPICE (Simulation Program with Integrated Circuits Emphasis) simulator provided by Mentor Graphics. Digital logic block level simulations were performed using the ModelSim VHDL simulator provided by Mentor Graphics.

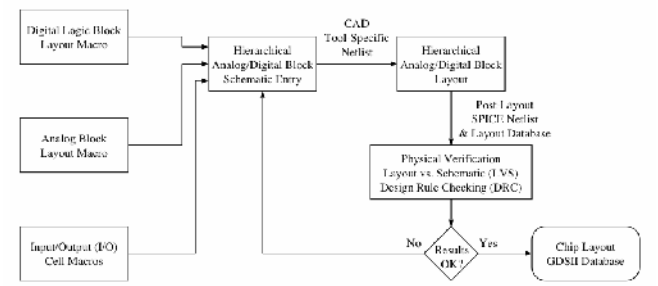

Fig. 8. Top level device design flow chart.

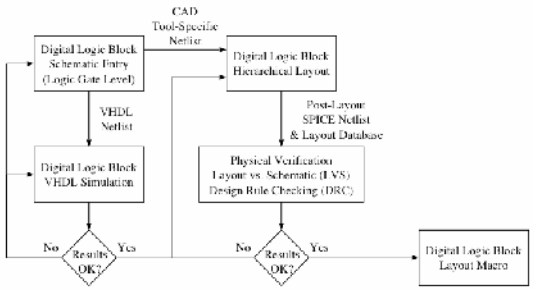

Fig. 9. Digital logic block design flow chart.

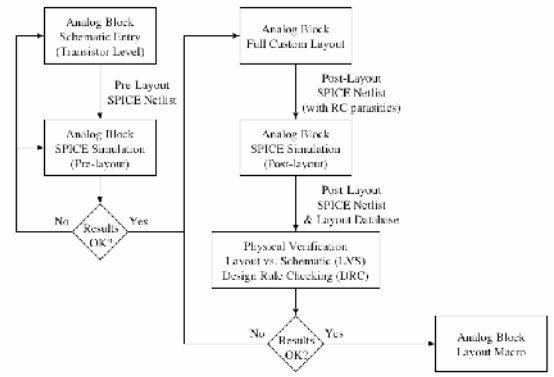

Fig. 10. Analog block design flow chart.

III. Results

Fig. 11 is the VHDL simulation waveforms for three of the digital logic circuit blocks: clock generation circuit, stimulation position decoding, and anodic scaling. Fig. 12 is an oscilloscope screen shot of a biphasic charge-balanced waveform using the push-pull mode of stimulation.

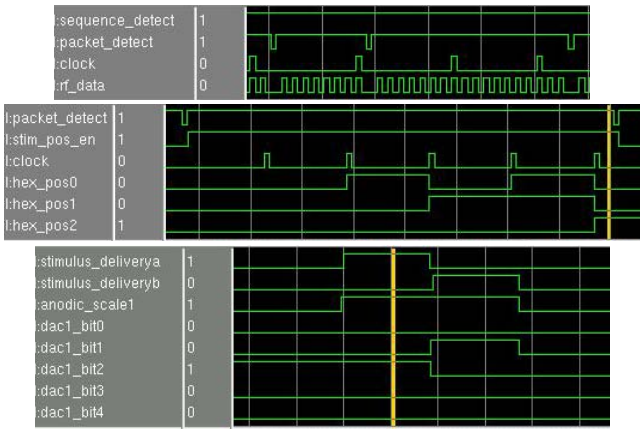

Fig. 11. Digital logic VHDL simulation waveforms for the following circuit blocks: (top panel) clock generation circuit; (middle panel) stimulation position decoding; (bottom panel) anodic scaling. (Top panel) A clock is generated for every eight cycles of RF, (middle panel) the decoded clock signals set the stimulation position, (bottom panel) the DAC programming bits are left-shifted by one at the end of the first phase of stimulation.

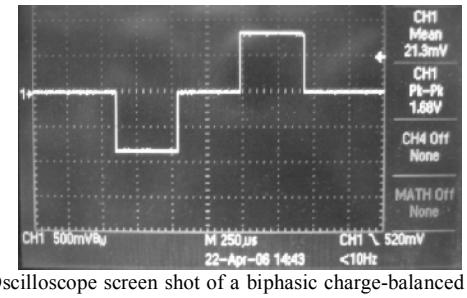

Fig. 12. Oscilloscope screen shot of a biphasic charge-balanced stimulation event using the push-pull mode of stimulation.

The two most important specifications of a DAC are the integral non-linearity (INL) and differential non-linearity (DNL) errors [37]. The resolution of the DAC is specified by the DNL; how much each DAC increment deviates from one LSB. If the DNL error is greater than one LSB, the DAC is not monotonic. The use of a thermometer-coded DAC, as implemented in this ASIC, provides the best architecture for achieving low DNL errors [35]. The accuracy of the DAC is measured by the offset error, the gain error, and the INL. Offset error is the difference between the ideal and actual DAC output, when the DAC input code is all 0's (i.e. the DAC is off); the gain error is the difference between the ideal and actual DAC output, when the DAC input code is all 1's (i.e. the DAC is at its full scale value). Ideally, both the offset and gain errors should be zero. The INL is a measure of how much each DAC bit deviates from its ideal value, expressed as a fraction of the LSB.

The INL and DNL of the current source and sink were measured by incrementing the DAC through all possible input codes (for each current range), and recording the current at each step using a digital ammeter (Fluke 189, Fluke Corp., Everett, WA, USA) connected between the current source and V_{ss}, or the current sink and $V_{stimulus}$. Both the INL and DNL were obtained after the gain and offset errors were removed.

Fig. 13 illustrates the measured current source and sink outputs, for all possible DAC input codes, using the mid current range (40µA to 1.24mA). The current source was connected through a 1kΩ resistor to V_{ss} and the current sink was connected through a 1kΩ resistor to $V_{stimulus}$. For the same current range, the worst case (WC) INL for the current source and sink were 0.24±0.04 LSB and 0.23±0.04 LSB (measured ± accuracy), respectively. The WC DNL for the current source and sink were 0.10±0.09 LSB and 0.08±0.03 LSB (measured ± accuracy), respectively.

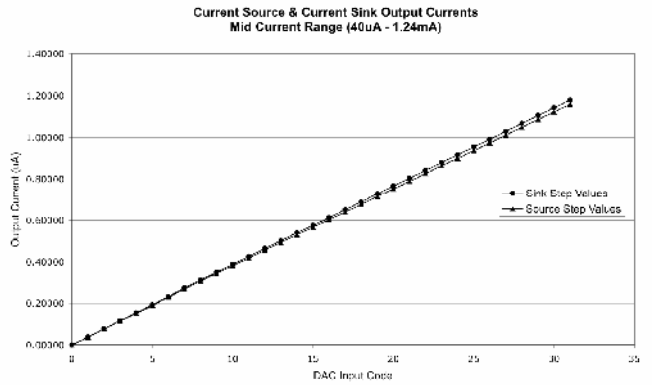

Fig. 13. Measured current source and sink outputs, for all possible DAC input codes, using the mid current range (40µA to 1.24mA). The current source was connected through a 1kΩ resistor to V_{ss} and the current sink was connected through a 1kΩ resistor to $V_{stimulus}$.

The output impedance and voltage compliance of the current source and sink were measured by connecting the current source and sink through a digital ammeter to a variable voltage source with reference to V_{ss}. As the variable voltage source was varied from $V_{stimulus}$ (11.7V) to V_{ss}, the current source and sink output current, and the voltage of the variable voltage source, were measured. The voltage at the voltage source was measured using a digital multimeter (Digitech QM1535). The voltage at which the output current was reduced by 1% from its highest value was also measured and used to calculate V_{comp} for the current source

and sink. The output impedance is the inverse of the slope of the current-voltage curve when the current source or current sink are operating in the linear region.

Fig. 14 illustrates the measured output current from the current source and sink, while varying the power supply. The measurements were taken using the highest DAC input code (DAC=31) for the mid current range (40µA to 1.24mA). The current source and sink output impedances were 850kΩ±8.9kΩ and 820kΩ±11kΩ (measured ± accuracy), respectively. The current source voltage compliance, with respect to $V_{stimulus}$ = 11.7V, was 10.3V±0.05V (measured ± accuracy). The current sink voltage compliance, with respect to V_{ss}, was 10.7V±0.01V (measured ± accuracy).

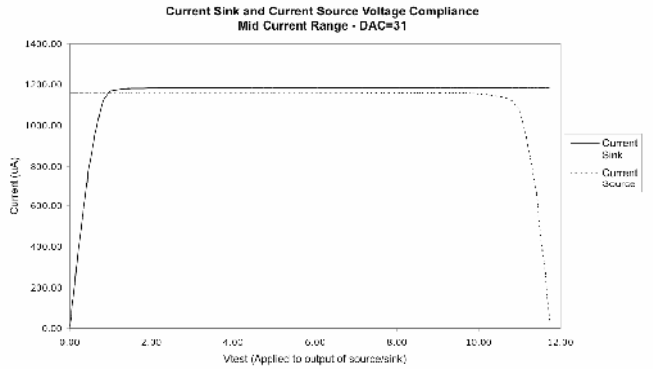

Fig. 14. Measured current source and sink voltage compliance using the highest DAC input code (DAC=31) for the mid current range (40µA to 1.24mA).

A test circuit board was constructed using bidirectional light emitting diodes (LEDs) arranged in the hexagonal pattern; each LED represents an electrode. The use of bidirectional LEDs allowed for the current direction to be visualized, while testing the movement of the stimulating and return (guard) electrode positions. The test setup confirmed that the ASIC could be configured for all possible electrode switch positions. A similar test circuit board using 1kΩ resistors was constructed to measure the current sharing between the hexagonal groups of electrodes. One end of the resistor was connected to an electrode pin on the ASIC, with the other end connected to a common potential on the board (shared with all other resistors). This common potential is a simplified model of the retinal tissue (0Ω resistance). The resistor test board was used to ensure that current was switched and shared correctly between the current sources and sinks of adjacent electrode clusters. Fig. 15 is a photograph of three ASICs connected to the LED test board (left panel) and the resistor board (right panel). Fig. 16 is a photograph of the LED test board illuminated using the push-pull stimulation mode, with the centre electrode configured as the stimulating electrode and the six surrounding electrodes configured as the return electrodes. Fig. 17 is a photograph of three ASICs connected through a bus.

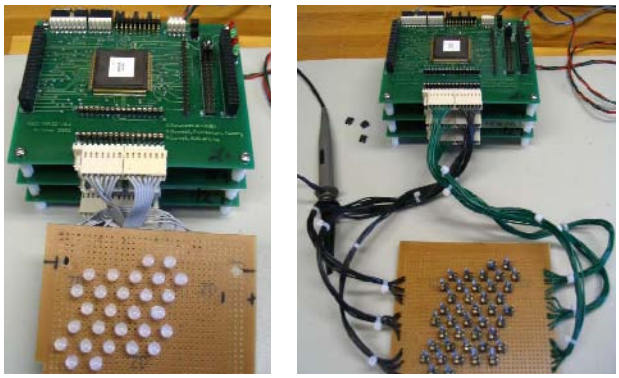

Fig. 15. (Left Panel) Bidirectional light emitting diode (LED) test circuit board used to verify that the ASIC switching logic functioned correctly. (Right Panel) 1kΩ resistor test circuit board used to verify that current was switched and shared correctly between the current sources and sinks of adjacent electrode clusters.

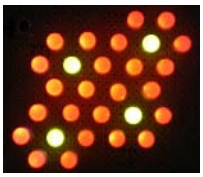

Fig. 16. Bidirectional light emitting diode (LED) test circuit board illuminated using the push-pull stimulation mode, with the centre electrode configured as the stimulating electrode and the six surrounding electrodes configured as the return (guard) electrodes.

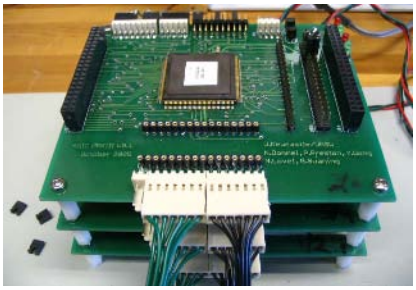

Fig. 17. Three ASICs in packaged parts connected together through printed circuit boards. The top board is acting as a master with the bottom boards acting as slaves. The bus connection is on the left side of the board and is common to each board. 14 electrodes are at the front of each board, and the incoming RF data and settings bits are at the back of each board.

IV. Discussion

The simulated and measured results confirm that the ASIC operates according to the design specifications. For the analog circuit blocks, SPICE Monte Carlo simulations (30 runs) were used to randomly vary individual transistor parameters, to obtain a statistical distribution of the expected circuit performance. The results lay within three standard deviations of the mean of the Monte Carlo simulation results, inline with industry standard control limits [38]. Correct switching of current sources and sinks was verified using the LED and resistor test boards.

The current source and sink WC INL and WC DNL results indicate a highly linear operation, with each DAC increment increasing the output current value close to the desired value. The output impedance of the current source and sink were acceptable, at least 10 times the expected value of $Z_{E/T}$ and Z_T combined (less than 100kΩ, based on

results reported by Mahadevappa et al. [13]), ensuring that neither the current source nor sink operation will be affected when connected to the electrodes. As the output impedance was measured at the highest current setting for vision prosthesis applications for the ASIC (DAC=31 in the mid current range), the output impedance values at all other currents will be higher than the values reported in the results. Lastly, the V_{comp} values are high and within specifications. If $V_{stimulus}$ is set at 12V, the current source and sink combined use 2.4V of the supply when delivering 1.24mA, which leaves 9.6V to appear across $Z_{E/T}$ and Z_T. The current source and sink voltages are maximums that will be used for the vision prosthesis current range.

The measured results compare well with results published for other vision prosthesis neurostimulator designs. For example, Sivaprakasam et al. recently presented results from a LV CMOS vision prosthesis neurostimulator with an anodic/cathodic current matching of 1.7%, a WC INL of 0.2 LSB, and a WC DNL of 0.15 LSB [39]. This compares well with the current source and sink current matching of 2.6%, WC INL of 0.24 LSB, and WC DNL of 1.0 LSB on this ASIC. The current sources and sinks used in this ASIC, and the ones reported on by Sivaprakasam et al. [39], were designed using current mirror circuits, which rely on V_{th} matching between transistors to achieve current matching [35]. As LV CMOS transistors provide better V_{th} matching than HV transistors [33], the results from our ASIC demonstrate that HV CMOS design in a neurostimulator does not necessarily hinder performance. Transistor matching is an important aspect of achieving low INL and DNL measurements.

Ghovanloo and Najafi designed a novel programmable current source in a LV CMOS process, with the goal of achieving a very high V_{comp} [40]. In the AMS H35B4D3 4M 2P process, LV transistors have a much lower V_{th} than equivalent HV transistors [34]. The V_{th} of the transistors may affect the design of the current source and sink, if a cascode current mirror structure is used (as in our ASIC) [35]. Ghovanloo and Najafi removed the effect of transistor V_{th} on V_{comp} in their design, resulting in a larger V_{comp}. Comparing the results from this current source circuit and the one described in this paper indicates that even without novel circuit design techniques, and using HV transistors, a large V_{comp} can be achieved.

The above results indicate that the use of a HV CMOS process and transistors in a vision prosthesis neurostimulator compare well with other neurostimulators implemented using a LV CMOS processes and transistors in this field. Despite this, the use of a HV CMOS process and transistors could be disputed due to the increased design complexity and increased cost. The primary reason for using a HV process is to allow for the greatest flexibility for the neurostimulator *in-situ*, due to the largely unknown and possibly changing $Z_{E/T}$ and Z_T. Mahadevappa et al. reported on the measured current thresholds required for visual perception using a 0.975ms cathodic/anodic biphasic stimulus, and the $Z_{E/T}$ and Z_T values at a stimulating frequency of 1kHz while delivering 10µA of current, for three human subjects implanted with a vision prosthesis for 18, 15, and seven months [13]. The results of this study indicated a large range in current required to elicit a visual percept (24 to 702µA), and a large range in $Z_{E/T}$ and Z_T measurements (up to 60kΩ). The author's noted an initial increase in $Z_{E/T}$ and Z_T in the first few weeks post-implantation, followed by a gradual decrease over the next few months. Electrode diameters used in the test were 500µm and 250µm.

Based on these results, it is not possible to predict the exact $Z_{E/T}$ and Z_T for each patient. In addition, electrode diameters are likely to decrease as greater electrode numbers are incorporated into the same area, resulting in an increased $Z_{E/T}$. Allowing for potentially large stimulating currents and $Z_{E/T}$ and Z_T, provides the greatest flexibility for the neurostimulator. If $Z_{E/T}$ and Z_T were as large as 20kΩ for a patient requiring a stimulation current of 500µA to elicit a visual percept, the neurostimulator circuit would require a minimum of 10V.

V. Conclusions

The ASIC neurostimulator was built to the stated specifications and has been tested to operate well within them. The use of a HV CMOS process to implement the neurostimulator ASIC allowed for the greatest flexibility; despite the increased design complexity, the ASIC operated as well, if not better, than comparative devices implemented using LV CMOS processes. The novel use of a bus structure allowed not only for a scalable design, but a significantly reduced layout space and hence cost. The ASIC will be used as a research tool to investigate the effects of simultaneous stimulation on neural tissue.

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