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Microelectronic Retinal Prosthesis: II. Use of High-Voltage CMOS in Retinal Neurostimulators

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***Abstract*— This paper presents the design, implementation, and simulated and measured results of a complementary metal-oxide-semiconductor neurostimulator implemented in a 0.35 μm high-voltage process. To allow for a high stimulation voltage, and hence the greatest versatility of the neurostimulator *in situ*, a high-voltage CMOS process was used. The neurostimulator utilized current sources and sinks to simultaneously deliver and recover charge. It has the ability to deliver stimulus in three output current ranges using a current sink only, current source only, or both a current source and sink combined to provide focused stimulation. The worst case integral non-linearity and differential non-linearity errors were 0.2 LSB and 0.1 LSB respectively, and the current source and sink turn-on times were under 500 ns, providing fast switching time in response to stimuli instructions. The total die area was under 13 mm^2, well within the area constraints of our implantable vision prosthesis device.**

***Index Terms*— digital-to-analog converter (DAC), high-voltage CMOS, parallel neural stimulation, vision prosthesis.**

I. Introduction

NEUROSTIMULATORS are used to excite neurons, eliciting action potentials leading to events such as motor movements and sensory perception. Current-mode neurostimulators operate by transferring charge over time from electronic circuitry to the neural tissue through electrodes, changing the extra-cellular potential field surrounding neurons and, once sufficiently changed, creating action potentials. Implantable current-mode neurostimulators, as used in vision prosthesis, are implemented as application specific integrated circuits (ASICs) using complementary metal-oxide-semiconductor (CMOS) circuitry.

The neurostimulator ASIC forms part of an electric circuit between the stimulus power supply (V_{stimulus}) and circuit ground (V_{SS}, the lowest potential in the neurostimulator circuit). The circuit includes the voltage across the current source (V_{source}), the electrode/tissue interface impedance ($Z_{\mathrm{e/t}}$), the tissue impedance (Z_{t}), and the voltage across the current sink (V_{sink}). Both V_{source} and V_{sink} must be large enough to ensure that the current source and sink are operational, yet low enough to maintain a large voltage compliance (V_{comp}) for each. V_{comp} of the current source and sink is the difference between V_{stimulus} and V_{source}, or V_{stimulus} and V_{sink}, respectively.

The values of $Z_{\mathrm{e/t}}$ and Z_{t} are not necessarily known prior to device implantation, and may change during its use [1], [2]. V_{comp} is dependent upon the stimulator circuit design, the current source and sink specifically. V_{stimulus} is externally chosen, but is limited to the maximum voltage allowed across the circuit components used to implement the ASIC. The ASIC described herein allows for a V_{stimulus} of up to 20 V, a high-voltage (HV) for CMOS technology, and was designed for a high V_{comp} (low V_{source} and V_{sink}). The high-level architecture of the ASIC was based on previous work done by this research group [3], [4]. This paper presents an overview of the architecture used on the ASIC, methods used to ensure the neurostimulator will function *in vivo*, key design and implementation issues, and the simulated and measured results from the fabricated ASIC.

II. Methods

A. Methods for Ensuring Stimulator Operation

Vision prosthesis neurostimulator ASICs have traditionally been implemented using standard low voltage (LV) CMOS processes [5], [6], [7]. The LV refers to the process supply voltage, generally below 5 V. One of the trends in LV CMOS design and manufacturing is to lower the supply voltage to below 1 V.

Maximizing V_{comp} of the current source and sink in the neurostimulator will increase the current output range of the neurostimulator. The use of wide-swing cascode current mirrors in the current source and sink will increase V_{comp} by one threshold voltage (V_{th}) compared with standard cascode current mirrors [8]. Ghovanloo and Najafi designed a neurostimulator using CMOS transistors in the triode region specifically to increase V_{comp} of a current source [5]. While both these techniques are effective, they only increase V_{comp} by a few hundred mV, which is not a significant increase when stimulating currents of up to 700 μA are used [9].

A second method for increasing the ability of the neurostimulator to function properly is increasing V_{stimulus}. The maximum voltage allowed by the CMOS process used to design the ASIC determines the maximum allowable V_{stimulus}. To increase V_{stimulus} beyond what the process can

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support, a HV CMOS process was chosen to implement the present ASIC. The process allowed for a V_{stimulus} of up to 20 V, providing greater versatility for the neurostimulator. As V_{stimulus} is increased, the power consumption increases, therefore careful design is required to limit the circuit components connected to V_{stimulus}.

The use of a HV CMOS process has design implications and increases the circuit complexity. Liu et al. proposed three reasons for avoiding a HV process and its associated HV transistors in a neurostimulator: poor transistor matching, large transistor sizes and hence increased layout area, and large drain resistance [6]. These issues are all valid, however using careful design techniques, as highlighted in this paper, excellent transistor matching was achieved and the use of HV transistors with large layout areas was minimized. Further, the use of a lightly doped fringe area (drift region) surrounding the heavily doped drain area (extrinsic drain) in the process used minimized the drain resistance [10].

B. Technology Information

The AMS H35B4D3 4M 2P process (Austriamicrosystems AG, Schloss Premstatten, Austria) was used, with foundry access provided through Europractice IC Services (IMEC, Leuven, Belgium). The process supports multiple gate-oxide thicknesses and extended drain transistors, and allows for both LV and HV transistors on the same die. The size of the ASIC die is 2.8 mm x 4.6 mm, well within the dimensions of our implantable vision prosthesis device.

C. ASIC Architecture

The ASIC receives programming commands via radio frequency (RF) telemetry. These commands program the electrode switches for the cathodic and anodic stimulation phases, and configure two separate current drivers. Each current driver is comprised of its own digital to analog converter (DAC), current source, and current sink. Electrode switches connect the current source and sink to the stimulating and guard electrodes. The switch connections are set based on the desired stimulating and guard electrode positions, and the phase of stimulation (cathodic or anodic) [3]. After both the cathodic and anodic stimulation phases, shorting of all electrodes together and to a common potential is required to recover any residual charge accumulation on the tissue to prevent tissue damage [11]. A shorting potential mid-way between V_{stimulus} and V_{SS} was chosen, as this ensures that neither the current source nor sink is out of compliance at the onset of the next stimulation event; in other words, ensuring that the current source and sink are operational.

The desired output current is generated via a five-bit DAC. Additionally, the DAC output can be scaled based on the desired operating range (20 μA - 620 μA, 40 μA - 1.24 mA, 130 μA - 4.03 mA) and is delivered to the electrodes via the current sources and sinks. The highest current range (130 μA - 4.03 mA) was designed for use in motor unit recruitment (FES) and can only be accessed by way of a hard-set connection to the ASIC, thereby removing its unintended use in a vision prosthesis. The DAC was designed using a thermometer-coded DAC architecture with wide-swing cascode current mirrors [8].

D. Transistor Selection

Table I lists the different HV and LV transistor types used, the features of each, and where in the design they were used.

TABLE I

TRANSISTOR TYPES USED, THEIR FEATURES, AND WHERE THEY WERE USED. V_{DS} IS THE DRAIN-SOURCE VOLTAGE, V_{Bpsub} IS THE BULK-$\mathrm{P}_{\mathrm{substrate}}$ VOLTAGE, AND V_{GS} IS THE GATE-SOURCE VOLTAGE.

Transistor Type	Features	Where Used
HV Asymmetrical NMOS/PMOS	HV V_{DS} LV V_{Bpsub} HV V_{GS}	Current sink and source cascode transistors
HV Symmetrical NMOS/PMOS	HV V_{DS} HV V_{Bpsub} HV V_{GS}	Electrode switches
LV Isolated PMOS	LV V_{DS} HV V_{Bpsub} LV V_{GS}	Current source non-cascode transistors

E. Selective HV or LV Transistor Placement

The use of HV transistors was limited to areas where absolutely required, as they have reduced transconductance compared with LV transistors, and layout areas orders of magnitude larger than equivalent-sized LV transistors [10]. HV transistors were required when either the gate, drain, or source was connected to a voltage higher than V_{DD} (3.3 V).

Fig. 1 illustrates the selective use of HV and LV transistors in the current source and sink circuit. LV transistors were used where possible, in particular for the current mirror circuit, for the following reasons: layout area orders of magnitude smaller than equivalent HV devices; better matching for key transistors in the current mirrors [10]; lower V_{th} resulting in a higher V_{comp} [12].

F. LV DAC and Current Source and Sink Design

The current source and sink currents were scaled in the LV DAC. Scaling at the HV output stage, by switching in additional transistors, would have reduced the current range seen by the individual HV output transistors, resulting in a lower effective gate voltage. This would have increased V_{comp} of the current source and sink. However, this would have more than doubled the layout area of the current source and sink which, in turn, would have increased the gate-source capacitance of the output driver transistors (as seen by the LV DAC) increasing the switching time of the current source and sink. Each current source and sink must be ready to deliver and recover charge at the onset of stimulation (i.e. they must have a fast switching time). To further decrease the switching time of the current source and sink, a small bias current of approximately 100 nA was used to keep the gate capacitance of all transistors charged.

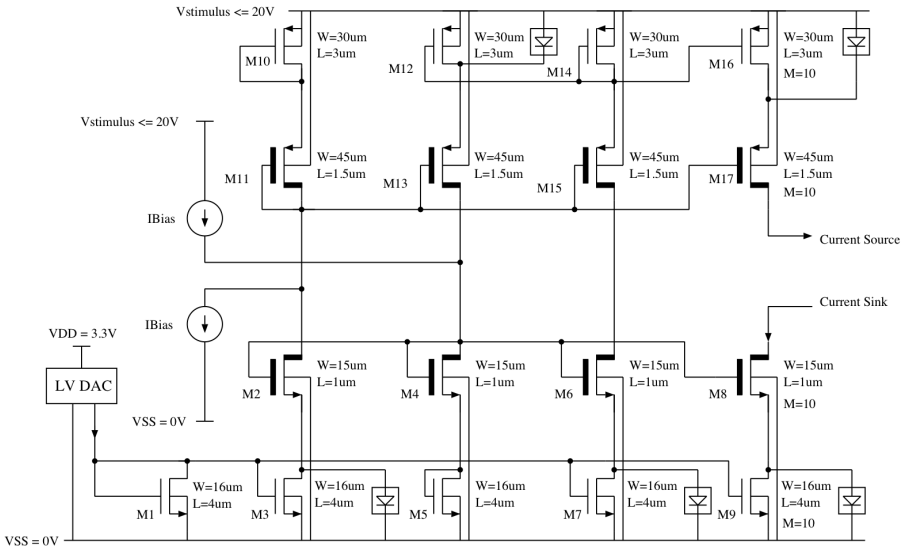

Fig. 1. Schematic diagram of the current source and sink. The circuit uses the following transistors: LV NMOS (M1, M3, M5, M7, M9); HV asymmetrical NMOS (M2, M4, M6, M8); HV asymmetrical PMOS (M11, M13, M15, M17); isolated LV PMOS (M10, M12, M14, M16). A small bias current (IBias) of approximately 100 nA was used to keep the gate capacitance of all transistors charged, to ensure fast switching times. Diode-connected LV protection transistors were connected between the drain and source of LV transistors M3, M7, M9, M12, and M16 (LV transistors that were not already diode-connected). The protection transistors were designed such that they do not turn on during normal operation; their combined threshold voltage is less than the maximum expected drain-source voltage (during normal operation) of the LV transistor they are protecting. If this voltage is exceeded, the protection devices are enabled.

G. Electrode Switch Design

The electrodes are connected to the current source and sink through electrode switches. Fig. 2 illustrates an electrode switch to a current sink. The drain-source resistance in a CMOS transistor is proportional to the transistor's length to width ratio [8]. A low switch on-resistance is desired, therefore the minimum length permitted by the process was used for the HV NMOS and PMOS switch transistors (M7 in Fig. 2). Wide transistors provide low on-resistance but much larger layout area, therefore the width was chosen to provide a reasonable on-resistance and layout area. Each electrode switch was controlled by LV logic circuitry. For this reason, an LV to HV logic level shifter/inverter circuit was required.

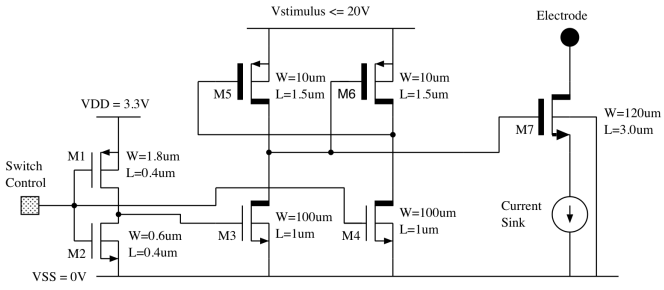

Fig. 2. Current sink switch (symmetrical HV NMOS transistor M7) controlled by a LV to HV logic level shifter (M1 through M6), which converts V_{SS} to V_{SS} (logic 0) and V_{DD} to V_{stimulus} (logic 1).

H. Layout Techniques

Transistor matching in certain areas of the ASIC was very important (e.g. current source/sink matching), therefore the following layout techniques were employed: drain-source orientations in the same direction; use of dummy transistors, no minimum dimension transistors, and equal gate lengths for all transistors; compact layout; no routing, contacts, or vias over matched transistors; split common-centroid layouts [10].

III. Results

Table II lists measured and SPICE (Simulation Program with Integrated Circuits Emphasis) simulation results, with the ASIC configured to deliver stimuli in the mid current range (40 μA - 1.24 mA). Measured results were from one part. Monte Carlo analysis (30 runs) was used for the SPICE simulations, to randomly vary individual transistor parameters to obtain a statistical distribution of the expected circuit performance. Results that are dependent upon the DAC input setting were listed for the highest setting (DAC=31), as this represents the upper possible limit for the specified measured value.

IV. Discussion

All aspects of the ASIC performed to specifications. Both the worst case (WC) differential non-linearity (DNL) and integral non-linearity (INL) errors for the current source and sink were very low, indicating a highly linear, monotonic DAC, with each step size close to the expected value, and each step size increasing in magnitude by a factor close to one LSB. V_{comp} at full-scale output current (DAC=31) was high – over 85 % of the available power supply for both the current source and sink (V_{source} was 1.4 V, V_{sink} was 1.0 V). The use of the bias current in the current source and sink substantially reduced their switching time to under 1 μs

TABLE II

ASIC DEVICE MEASUREMENT AND SPICE MONTE CARLO (MC) SIMULATION RESULTS (N=30) FOR CURRENT RANGE (40 μA - 1.24 MA). ACCURACY OF MEASURED VALUES REPRESENTS INSTRUMENT ACCURACY AND THEIR AFFECT ON THE MEASURED RESULTS.

	Measured Value $\pm$ Accuracy	SPICE MC Mean ($\bar{X}$) and Std. Dev. (σ)
Current Source & Sink Worst Case INL	0.24 LSB $\pm$ 0.04 LSB	$\bar{X}$ = 0.12 LSB σ = 0.04 LSB
Current Source & Sink Worst Case DNL	0.10 LSB $\pm$ 0.09 LSB	$\bar{X}$ = 0.07 LSB σ = 0.02 LSB
Current Matching of Current Source to Sink	2.6 % $\pm$ 0.5 %	$\bar{X}$ = 1.18 % σ = 0.84 %
Current Source Voltage Compliance @ DAC=31 (w.r.t. V_{stimulus} = 11.7 V)	10.3 V $\pm$ 0.052 V	$\bar{X}$ = 10.79 V σ = 0.14 V
Current Sink Voltage Compliance @ DAC=31 (w.r.t. V_{stimulus} = 11.7 V)	10.7 V $\pm$ 0.005 V	$\bar{X}$ = 10.77 V σ = 0.09 V
Current Source Turn-On Time @ DAC=31	316 ns $\pm$ 80 ns	$\bar{X}$ = 650.6 ns σ = 64.5 ns
Current Sink Turn-On Time @ DAC=31	282 ns$\pm$ 60 ns	$\bar{X}$ = 655.4 ns σ = 62.9 ns
Current Source Switch Resistance	438 Ω $\pm$ 104 Ω	$\bar{X}$ = 496.9 Ω σ = 15.6 Ω
Current Sink Switch Resistance	360 Ω $\pm$ 56.4 Ω	$\bar{X}$ = 395.2 Ω σ = 10.8 Ω

from over 25 μs (if no bias current was used), ensuring that the current source and sink are programmed well in advance of the onset of a stimulation event several μs later (based on the communication data frame rate).

A standard control limit used for qualifying integrated circuits is that the measured results lie within three standard deviations (3σ) of the mean ($\bar{X}$) of the Monte Carlo simulation results [13]. For all of the measured results, except the current source and sink turn-on time, this was the case. The measured current source and sink turn-on times were much faster than the simulated results. This may be due to slightly inaccurate circuit layout parasitic elements extracted for simulation purposes. The current mismatch (2.6 %) is largely due to mismatch in device parameters (V_{th}, gain factor, mobility reduction, and drift resistance), and matches the values extracted in test structures at the foundry [14]. The difference between the measured and simulated WC INL and current mismatch could be due to the inability of the SPICE models to accurately model device mismatch parameters.

Sivaprakasam et al. recently presented data from a LV vision prosthesis neurostimulator which had an anodic/cathodic current matching of 1.7 % [7]. The LV neurostimulator presented by Ghovanloo and Najafi had a V_{comp} of 4.25 V with respect to a 5 V power supply (85 % of the supply voltage); in other words, a V_{source} of 0.75 V [5]. The 2.6 % current sink and source matching, V_{source} of 1.4 V, and V_{sink} of 1.0 V measured on the ASIC reported in this paper, compare favorably with the devices reported on by Sivaprakasam et al. and Ghovanloo and Najafi.

To reduce the power consumption of a HV CMOS neurostimulator, it is important to ensure that a minimum number of transistors operate at the higher voltage, and that V_{stimulus} is not increased beyond what is needed for the neurostimulator to operate *in-situ*.

V. CONCLUSION

The use of a HV CMOS process in a vision prosthesis neurostimulator allows the stimulation voltage to be set much higher than an equivalent LV process, thereby providing the greatest versatility of the device *in-situ* given the uncertain electrode/tissue interface and tissue impedance. If careful consideration is given to the design, and HV transistors are used carefully and sparingly, results comparable or superior to other vision prosthesis neurostimulators can be achieved.

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