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A Neural Signal Processor for an Implantable Multi-Channel Cortical Recording Microsystem

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***Abstract*- A 64-channel neural processor has been developed for use in an implantable neural recording microsystem. In the Scan Mode, the processor is capable of detecting positive, negative, and biphasic spikes with programmable thresholds. It collects action potential information from the input channels, tags the activities with the associated channel address, compresses and finally packs the activity information in a serial digital bit stream to be sent to an external host. In the Monitor Mode, two channels can be selected and viewed at high resolution for studies where the entire signal is of interest.**

I. Introduction

Direct recording of action potentials from different regions in the brain is of interest to neurophysiologists to enable them to better understand the behavior of the brain and to treat a variety of neural disorders. Passive recording microprobes (without electronic circuitry) hardwired to the external world [1] are widely used for such studies. To permit chronic recording from a hundred or more sites, such systems will need to be equipped with a neural processor to organize the collected data and a bidirectional telemetry link through which to receive power and command signals from the outside world and transmit the recorded activity. The first such neural processor [2] handles 32 neural channels with positive spike thresholding using digitally-computed channel offsets. A second processor [3] has also been reported that will handle up to 100 channels, thresholding on positive spikes. The processor reported here can be set for positive, negative, or biphasic spike detection and is programmable to handle a wide number of recording situations. It is compatible with both passive and active recording probes.

II. The System and Its Operation

The neural processor described in this paper is the heart of a wireless implantable microsystem capable of recording single-unit activity on up to 64 simultaneous channels from areas such as motor cortex. The system is powered and controlled over an inductive bidirectional wireless link, and also transmits the processed neural activity to the outside world. Fig. 1 illustrates the general architecture of the microsystem.

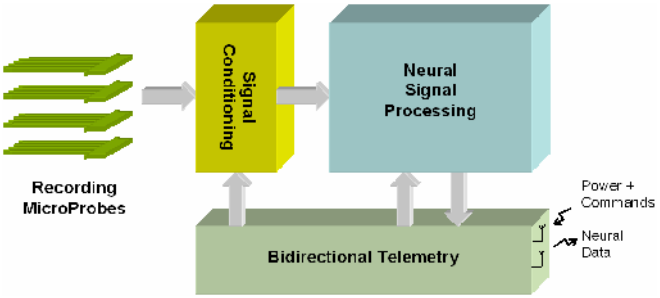

Fig. 1: System block diagram

Two 32-site passive silicon recording microprobes are used to sense single-unit activity from the cortex. The sensed signals are transferred to a hermetically sealed electronics package over ribbon cables. The signal conditioning front-end consists of four 16-channel chips, pre-amplifying and band-pass filtering the signals sensed by the microprobes. The bidirectional telemetry module (BTM) interfaces with the outside world. It retrieves the clock and data carried by the RF signal received through the forward telemetry link, and uses the energy received through the same link to generate regulated power for the implanted system. The reverse telemetry back-end on the BTM encodes, modulates, and transmits the processed neural information to the outside world. There is also an application-specific controller on the BTM that gets, checks, and interprets the received data packets. The control and timing signals required for the system are generated by the controller and in response to the commands conveyed by the data packets. The neural processing unit (NPU) is the processing heart of the system and is described in detail in this paper.

III. The Neural Processing Unit

The NPU is designed to support the *operational modes* defined for the system:

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- In the *Scan Mode*, all 64 channels are searched for the occurrence of neural spikes. The addresses of the active channels, i.e., the channels with neural activity, are sorted, packed, and sent to the outside world through the reverse telemetry link. In this mode, each channel can be individually set to detect positive, negative, or biphasic spikes. Also, the spike detection thresholds can be adjusted for each of the channels individually.

- In the *Monitor Mode,* one of the 64 neural channels is selected, sampled at high resolution, and transmitted to the outside world. The selected channel can be sent out either directly in analog form or after quantization to 8 bits.

Additionally, there is a third mode supporting the spike detection settings for the Scan Mode, called the *Spike Detection Setting (SDS) Mode*. In this mode, the desired spike polarity (positive, negative, or biphasic) and the threshold value for each individual channel can be set.

Designed with a fully-modular architecture, the 64-channel NPU (NPU-64) consists of two 32-channel NPUs (NPU-32) communicating with each other in a master-slave fashion. Like ping-pong, the Master takes care of its 32-channels in 32 clock cycles, and then activates the Slave for the next 32 clock cycles. At the end of its chip cycle, the Slave sends a pulse to the Master so that it can resume its operation. In addition to taking care of its own 32 channels, the Master obtains the neural information received from the Slave and sends the information collected (in Scan Mode) from or selected from among (in Monitor Mode) the 64 channels to the BTM to be transmitted out.

The NPU-32 chip is designed to be configured either as the Master or as the Slave. It is worth noting that being operated in its basic functional mode, a single NPU-32 chip can also be used as a stand-alone 32-channel NPU. As illustrated in Fig. 2, each NPU-32 consists of four 8-channel modules (SD-8) and a data fusion core, which is responsible for organizing the information that the four SD-8s provide.

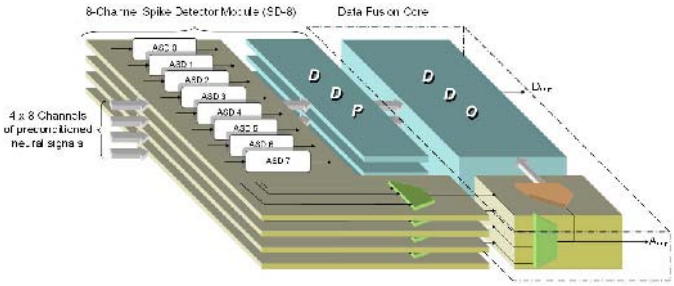


Fig. 2: Block diagram of the NPU-32

Each SD-8 comprises eight programmable analog spike detectors (ASDs), a small digital data Processor (DDP) that tags the neural activity with the associated channel addresses and stores them in a local memory for the Scan Mode, and an analog channel selector for the Monitor Mode. The Data Fusion Core consists of a Digital Data Organizer (DDO) to organize the data provided by the four SD-8 modules in the Scan Mode and an analog channel selector to pick one of the channels provided by the four SD-8s in the Monitor Mode. The selected channel can be either directly sent out or converted to digital using an external 8-bit A/D converter and delivered to the DDO in order to be packed in the same fashion as the Scan-Mode data are.

In the Scan Mode, after all the eight channels on the four SD-8s are scanned in parallel, a read operation is performed on the four local memories at the same time. As a result, four 4-bit digital words are fetched, each of which indicates the address of an active channel on the associated SD-8 module plus a validation bit (A_{i0}–A_{i3} & VB_i, i=0,1,2,3). Then, an even parity bit is generated for each two 4-bit words (P_0, P_1). The outgoing data packet in the Scan Mode begins with a Start Pulse, which stays high for four clock cycles. Then, a Chip Address Bit (CAB) follows, which indicates whether the packet is generated by the Master or by the Slave. After that, the above-mentioned 16 bits of neural activity information plus two parity bits will come, as illustrated in Fig. 3

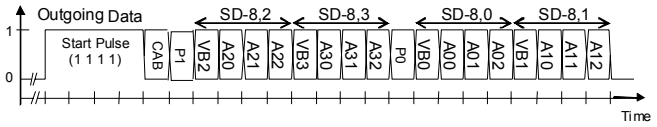


Fig. 3: Outgoing data packet in the Scan Mode

In the Monitor Mode, if the selected channel is to be sent out in digital format, an even parity bit is generated for each 8-bit amplitude sample, and every two consecutive samples accompanied by the associated party bits are carried by a data packet, as illustrated in Fig. 4. As seen, the data packet structure in the monitor mode is much similar to the one generated in the scan mode.

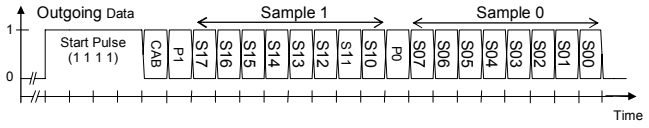


Fig. 4: Outgoing data packet in the Monitor Mode

It is worth noting that the Master NPU interleaves the data packets prepared by itself and the ones it receives from the Slave NPU. This enables the NPU-64 in the Monitor Mode to monitor one channel within the range of the Master and a second channel within the Slave area at the same time (interleaved).

It was mentioned earlier that each individual ASD can be programmed to detect positive, negative, or biphasic spikes, as shown in Fig. 5. As illustrated in Fig. 6, using a 5-bit threshold word (THR) the positive and negative thresholds, $V_{TH,P}$ and $V_{TH,N}$, are symmetrically set around the threshold offset (THR Offset), which itself can be set at three different levels. This setting approach covers wide ranges for both positive and negative thresholds.

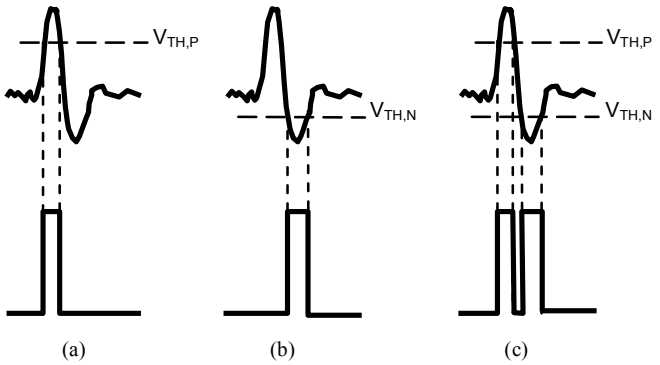


Fig. 5: Spike detection modes supported by the NPU (a) Positive (b) Negative (c) Biphasic

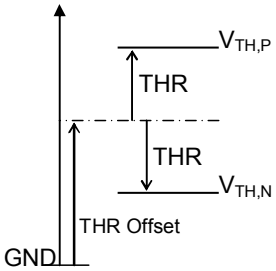


Fig. 6: Defining positive and negative thresholds using a threshold value (THR) and an Offset (THR Offset)

IV. Experimental Results

The NPU-32 chip was fabricated in the AMI 0.5µm 3M2P standard N-well CMOS process, and occupies 3.5mmx2.7mm of silicon area. A photo of the fabricated chip is shown in Fig. 7.

The tunability of both positive and negative thresholds dictated by the digital information received from the external system through the forward telemetry link is first tested. Fig. 8 demonstrates the threshold-setting function by changing the threshold value (THR), while Fig. 9 shows how the threshold offset (THR Offset) is changed.

Fig. 10 demonstrates positive, negative, and biphasic spike detection performed by an ASD. Shown in Fig. 11 is the generated data packet in the Scan Mode. In this test, channels 0, 13, 23, and 26 are active. Channel addressing/switching in the Monitor Mode is shown in Fig. 12. To better demonstrate Monitor Mode operation, a square wave is applied to channel 00, a sine wave is fed into channel 26, and a pre-recorded neural signal is applied as input to Channel 19. First, the NPU is reset and as a result, channel 00 is the default channel selected for monitoring. Then, using the control and timing signals ASDA and AClk, channels 26 and 19 are selected to be monitored. Specifications of the neural processor are summarized in Table 1.

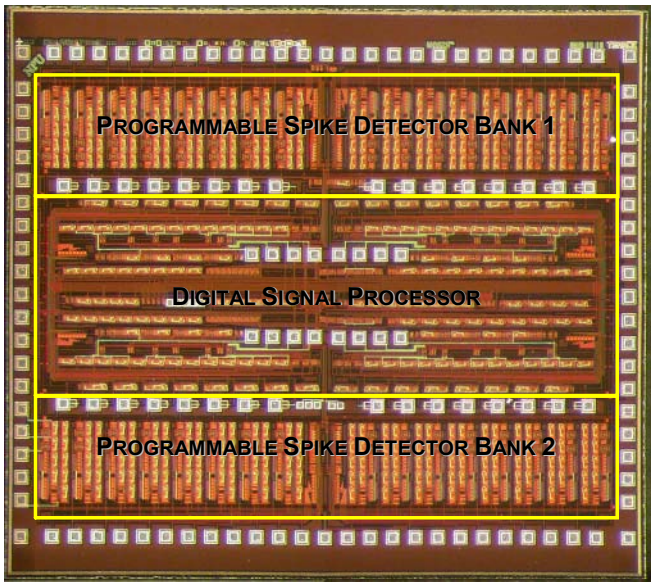


Fig. 7: NPU-32 die photo

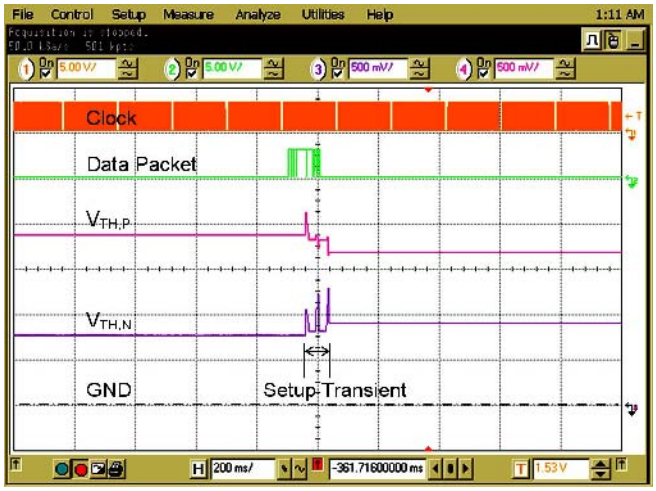


Fig. 8: Setting the threshold value

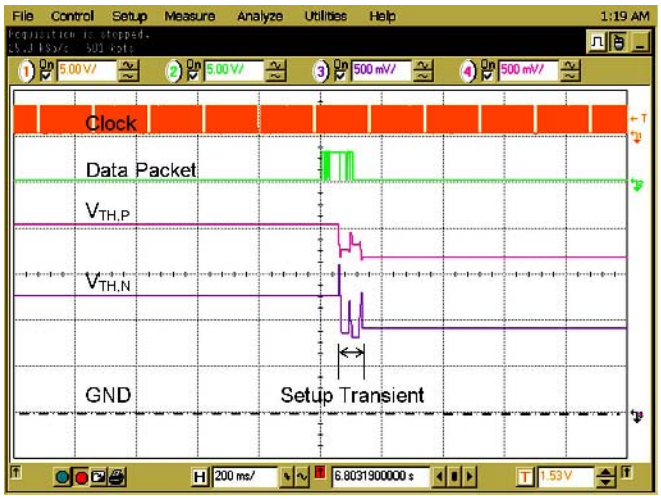
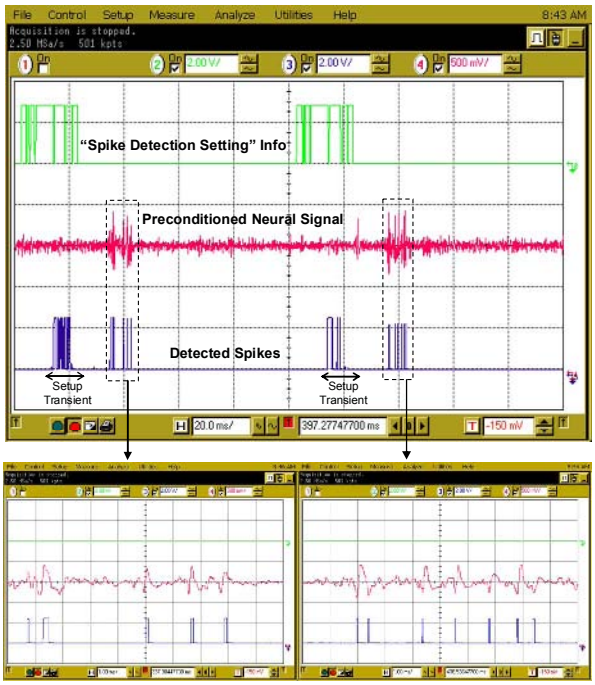
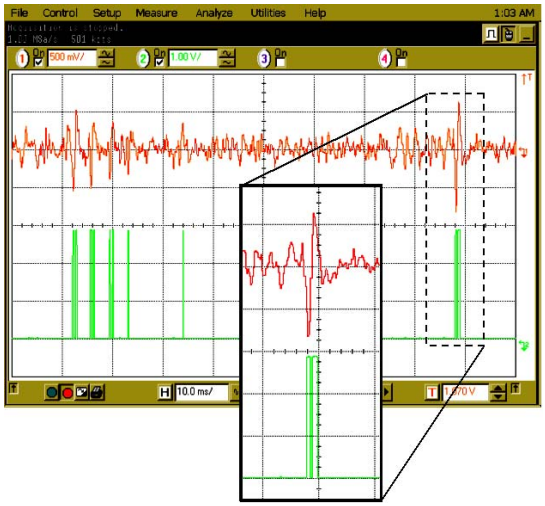


Fig. 9: Setting the threshold offset



(a)



(b)

Fig. 10: Different modes of spike detection (a) Changing the spike detection method from positive to negative in real time (b) Biphasic spike detection

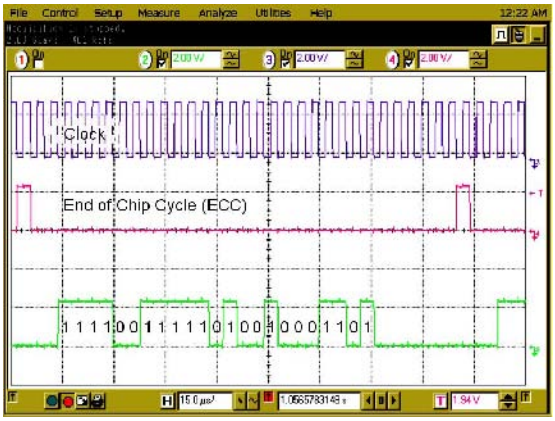


Fig. 11: Data packing in the Scan Mode

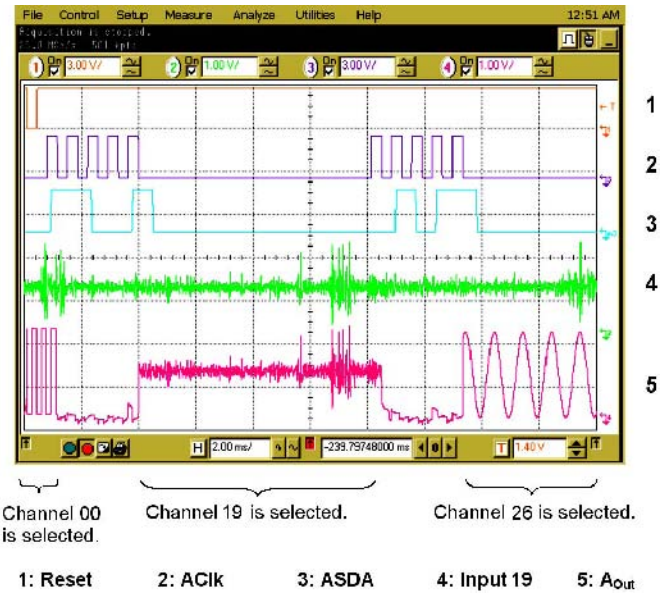


Fig. 12: Channel switching in the Monitor Mode

Table 1: Specifications of the Neural Processor

Specification		Value
No. of input channels		64
No. of channels for simultaneous spike detection		64
No. of channels for simultaneous high-resolution monitoring		2
Threshold setting range:	$V_{TH,P}$	850 mV
	$V_{TH,N}$	1000 mV
Clock frequency		2 MHz
Channel scan rate		64kSample/sec.
Output bit rate		2Mbps
Outgoing channel data rate w/o compression		64kSpike/sec.
Average outgoing ch. data rate w/ compression		8kSpike/sec.
Data compression		8:1
Fabrication process		0.5µm CMOS
Die size (NPU-32)		3.5mmx2.7mm

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REFERENCES

[1] J. Csicsvari, et al, "Massively parallel recording of unit and local field potentials with silicon based electrodes," *J. Neurophys*., vol. 90, no. 2, pp. 1323–1341, 2003.

[2] R. Olsson III, K. Wise, "A Three-Dimensional Neural Recording Microsystem with Implantable Data Compression Circuitry," *IEEE J. Solid-State Circuits., 40*, No. 12, Dec. 2005.

[3] R. Harrison, et al, "A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural Recording System," *Digest IEEE Int. Solid-State Circuits Conf*., pp. 554-555, February 2006.