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Parallel Multiplexing – a Solution of Large Scale Stimulation Needed by the Retinal Prostheses to Maintain the Persistence of Vision

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Abstract– **So far a retinal prosthesis has been able to stimulate a limited number of neurons (around 100) by the biphasic current stimulus to reproduce an image spatially by multiplexing technique. For functional restoration of sight (visual acuity 20/80) we are to stimulate at least 2500 neurons/mm^2. We are far behind that target. The time required by biphasic stimulus, and sequential stimulation by multiplexing technique limits our ability to stimulate a large number of neurons, and maintain the persistence of vision. We have designed a stimulus circuit applying parallel multiplexing technique, which is capable of simultaneous stimulation of a large number of cells. This paper presents an implantable CMOS-based 5x5 array prosthesis to demonstrate that idea. This 5x5 array prosthesis is scalable to a larger array. It uses external clock for its timing making it suitable for any data rate. It has a programmable biphasic width controller (BWC), which can generate monophasic or biphasic current stimulus with or without interphase delay. The chip has been fabricated using 0.5 µm CMOS technology and tested.**

Keywords – M**ultiplexing, retinal prosthesis, Biphasic stimulus, current stimulator**

I. Introduction

Retinitis pigmentosa (RP) and age-related macular degeneration (AMD) are the two main diseases which turned more than 10 million peoples blind. RP and AMD are not curable by medicine. Retinal prosthesis is the solution for these people. Photoreceptors of retina help us see. Due to AMD or RP, photoreceptors degenerate or cease to exist [1]. The goal of most of the researches is to develop a retinal prosthesis that will replace photoreceptors and pass visual signal to the next level. Epiretinal prosthesis pass signal to the ganglion cells, while subretinal prosthesis relay signals to the bipolar cells. Research is in progress on both kinds of prosthesis. We saw some successes of retinal stimulation by only limited number of electrodes [2-3]. This success has demonstrated the ability to stimulate retina and give sight to the blind. So far the vision is limited to creation of stars like phosphene for the blind with the limited number of electrodes like an array of 5x5 [2] or 10x10 array [3]. In terms of density, it is only 20 electrodes/mm^2 [3]. Though it is crude, it has demonstrated the idea. For functional restoration of sight the required visual acuity is 20/80, which is equivalent to 2500 pixel/mm^2 [4]. That means we are to excite as many as 2500 electrodes/mm^2. For stimulation, the biphasic current stimulus is used [1, 5]. Biphasic current stimulus has four variables -- amplitude, width, interphase delay, and frequency. Typical values of these variables as reported in different papers are: amplitude 10-600µA, width 100µs-2ms, interface delay 0-1ms, and frequency 10-125Hz [5]. This suggests that the duration of engagement of biphasic pulse could be as long as 5ms. The persistence of vision is 1/30th of a second. This persistence of vision give us 33.33ms to complete one frame. If we apply multiplexing technique, and stimulate each neuron for 5ms, then only six electrodes could be stimulated within the time frame. So large-scale stimulation necessary by retinal prosthesis is a big challenge. Simple multiplexing technique won't work for large-scale stimulation. To address this problem we have developed parallel multiplexing technique [1]. By this technique we have been able to excite a large number of neurons within the persistence of vision. Though six electrodes could be excited through multiplexing technique, in our design we have considered only five electrodes to allow more stimulation time. Then we have divided the total number of electrodes in five groups, and applied parallel stimulation to all the electrodes of a group, and multiplexing among the groups. In this way we can excite as many neurons as we want by biphasic current stimulus, and still maintain the persistence of vision. To demonstrate this idea we have designed, fabricated, and tested a 5x5 array retinal implant chip (RIC). Our ultimate goal is an integrated wireless retinal prosthesis. If the wireless receiver is not on board of the RIC, then to interface it with wireless receiver our RIC needs only 5 wires, a huge reduction of number of wires compare to flexible retinal implant [6].

II. System Overview

The overall system of our retinal prosthesis is given in Fig. 1. Extraocular unit of this two units system has a CCD camera, an image processor, an encoder, and a transmitter built on an eyeglass frame. High-resolution image from a CCD camera is reduced to lower resolution image by the image processor to match the array of electrodes. The reduced image is then encoded and transmitted wirelessly after time multiplexing.

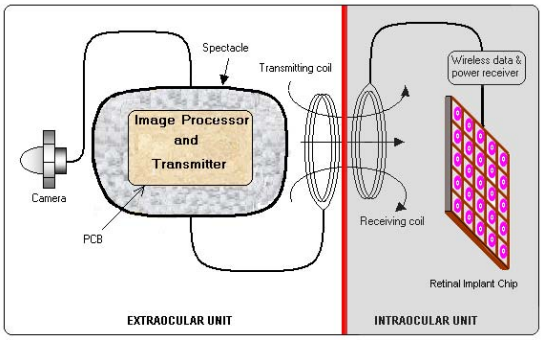


Fig. 1. Complete system of retinal prosthesis

Intraocular unit consist of a wireless data and power receiver, and a retinal implant chip (RIC). Wireless data and power receiver recovers each pixel and clock, and generates necessary power for the chip from its 13.56MHz carrier frequency. The RIC convert each pixel into biphasic current stimulus, and apply it to an array of electrodes in sequence. Extraocular and intraocular units are coupled together magnetically. Our design uses external clock for its timing. So its data rate is limited by the external clock. Another advantage of this design is that we can generate wide range of biphasic widths/interface delay, as they are the multiple of clock cycle.

III. DESIGN

The complete retinal prosthesis is a complex system. Our present design is focused on the part of the system that goes into the retina i.e. retinal implant chip (RIC) of intraocular unit. We are presenting a scalable unique design of 5x5 array RIC using parallel multiplexing technique. The block diagram of the RIC is given in Fig. 2. Four main functional blocks of the chip are biphasic width controller (BWC), data receiving register (DRR), current stimulator (CS), and neural stimulator (NS). These blocks are controlled by the retinal implant chip controller (RICC).

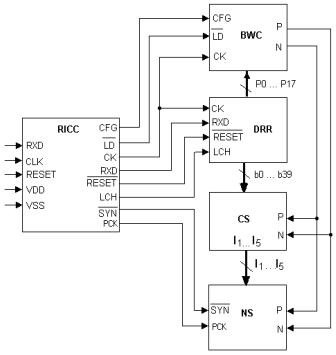


Fig. 2. Block diagram of retinal implant chip (RIC)

RICC: There are five wires through which RIC communicates with the wireless receiver. We assume that the wireless receiver is giving us time multiplexed serial data (RXD) with synchronized clock (CLK), and initial reset (RESET). With reset the controller starts counting (counter is shown as part of DRR block) and issue control signals to the various blocks as required.

BWC: To generate biphasic waveform of variable widths and interphase delay, we have designed a programmable BWC (Fig. 3a). BWC is made of three similar units for controlling cathodic (N), interface delay, and anodic width (P). Each unit has a synchronous binary counter composed of 6 TFF's (Fig. 3b) with six parallel inputs fed by 6 bits memory register (LCH0 to LCH17), which holds the programmable bits for the widths and interface delay of the biphasic waveform. By programming these six bits of the memory register, the variable widths and interphase delay are generated. For longer width or delay the unit should be programmed with lower number as the width or delay is the difference between the set number and 64. The beauty of the circuit is that without any hardware change we can generate only cathodic or anodic pulse by setting the other to zero or biphasic pulse without delay by setting interphase delay to zero.

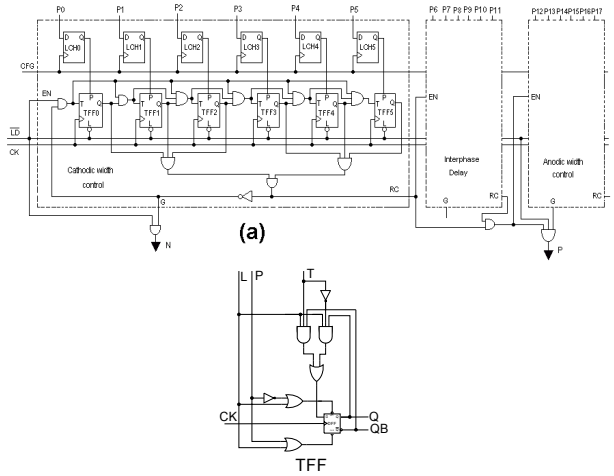


Fig. 3. (a) Biphasic width controller (BWC), (b) TFF

DRR: DRR (Fig. 4) is made of a serial to parallel converter, a register to hold 40 bits of data, and a counter, which generates a pulse at the end of the count. The received serial data is converted to parallel data by DFF0 to DFF39.

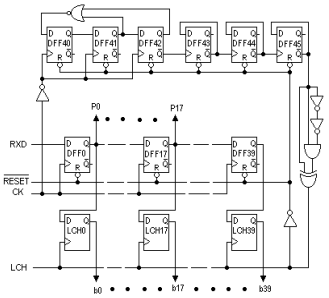
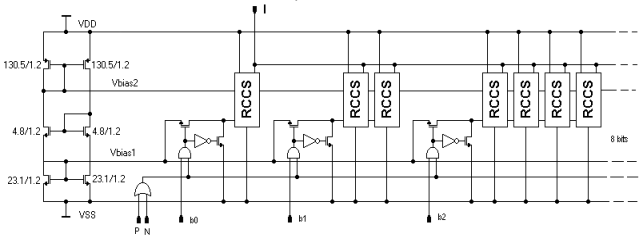


Fig. 4. DRR with counter, latch, and single pulse generator

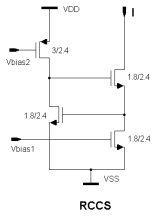
This 40-bit parallel data could be latched in BWC (Fig. 3a) or in DRR (LCH0-LCH39) by the controller RICC. After reset, the last 18 bits of first 40 bits loaded in DRR is stored in BWC as the configuration word by ascertaining CFG low. After that DRR will be receiving data of each pixel. When 5 pixels, each of 8 bits, are loaded in the DRR that data is latched in LCH0 to LCH39. Right after latching, DRR starts loading another 40 bits, while the old bits are available in latches for CS to generate equivalent current. The counter keeps count of the number of bits received, while the gates in the output generate a short pulse to latch and drive other units.

CS: CS (Fig. 5a) is an 8-bit current converter and converts binary-weighted data (b0…b7) into equivalent analog current (I). We designed our CS using regulated

cascode current sink (RCCS) (Fig. 5b), which uses negative feedback to stabilize the output current, and to increase the output impedance. CS has a bias circuit to generate biases for the RCCS. Bias2 is applied directly to the RCCS, while bias1 is controlled by transistors and gates. When the binary input is high and the cathodic (N) or anodic width control pulse (P) is high, then the bias 1 will be applied. Otherwise bias1 of RCCS will be ground. Control of bias1 by binary input could be enough, but the additional control by the OR gate helped us reduce the current surge during switching. CS has been design for a resolution of 2.5µA current, and can deliver 640µA current at 10KΩ and 7V for the full 8-bit pixel. At 5V it can deliver 484µA at 10KΩ load. For 5x5 array NS we have used five current stimulators, one for each column.



(a)



(b)

Fig. 5. (a) Current Stimulator (b) RCCS

NS: The function of NS is to demultiplex the analog current and stimulate the neurons. The design of 5x5 array NS is shown in Fig. 6. We have applied parallel multiplexing technique to design it. It has eleven I/Os (SYN, PCK, N, P, I_1 to I_5, VDD, and VSS) to interface with the other units. It is made of an array of probes, and a decoder (DFF1—DFF5). Each probe has four switches, which are controlled by two AND gates, which are, in turn, controlled by the decoder and the BWC. We have designed each probe with two concentric flat electrodes -- one circular and another donut. The structure of a probe is shown in Fig. 7. It is based on CMOS technology. The central and donut electrodes are fabricated on top metal-3 layer. The diameter of the central electrode is 60µm, and the diameters of donut electrode are 120µm and 140µm. Underneath the electrodes the switches and gates are grown. There are five current stimulating buses (I_1 to I_5); each of them carries the time-multiplexed stimulus for all the probes of a column. PCK is the clock for the decoder, which is 40 times slower than the data clock (CK). With start (SYN low), decoder points to the first row as DFF1 is set and others are cleared, and five different stimulus currents are applied to the five probes of the first row, the duration of which are controlled by N and P. Before the rising edge of next PCK cycle (which occurs after 40 CK cycles), DRR is loaded with new data for the next row; and at the rising edge next row is selected by the decoder (DFF2), and new data is latched in DRR, which is then converted into analog currents (I_1–I_5) by CS, and are applied to the probes of new row for the duration controlled by N and P. This pattern goes on till the end of 5th row, and then it starts all over again. So we are applying parallel stimulation to all the probes of a row, and multiplexing among the rows. To increase the array size we are to add more columns of probes with additional CS.

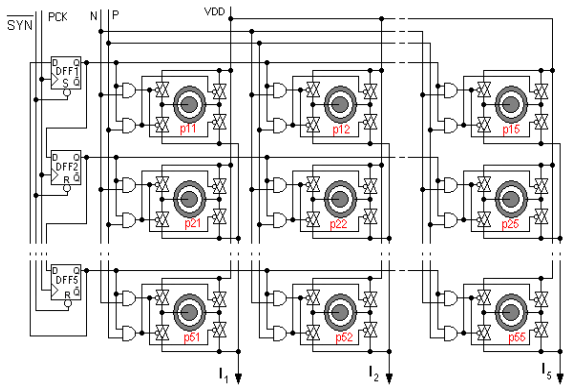


Fig. 6. 5x5 array neural stimulator

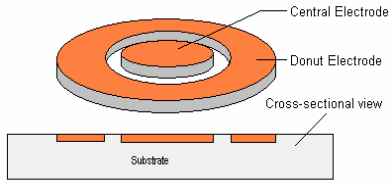


Fig. 7. Structure of a donut probe (Not to scale)

III. Test Results

The test of CS is plotted in Fig. 8. We have tested it with 5V and 10KΩ load for the whole range of 8-bit pixel. The test results reveal that the CS has 2.5µA resolution, and is linear up to 463µA till pixel value 190. Maximum current is 489µA at 8-bit pixel.

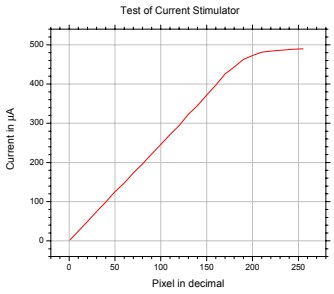


Fig. 8. Current Stimulator characteristics

The microscopic view of the 5x5 array NS is shown in Fig. 9. It is fabricated using 0.5µm CMOS technology. Probes array is laid out in 750µm×750µm area at the center, while the decoder at left side of the array. The die size of NS is 1500µm×1500µm. To get access to the probes, the NS is fabricated without package, and also with special package

designed for testing. Typical 10KΩ neural impedance is used as load. Clock is set at 1KHz, 5V and 50% duty. 442μA is applied to I_1 and152μA to I_3. Parallel stimulation test result is

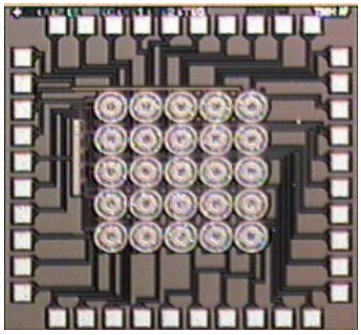


Fig. 9. Microscopic view of 5x5 array NS

presented in Fig. 10. We have presented here the outputs of probes P21 and P23 only. To present current by oscilloscope, it has been converted to voltage. P21 and P23 are the 1st and 3rd probe of the 2nd row of the array. So both of them were excited simultaneously during second cycle after the SYN pulse. The result shows that each probe was excited by biphasic waveform, and N and P control the cathodic, anodic, and interface delay. The stimulation was repeated after 5 clock cycles.

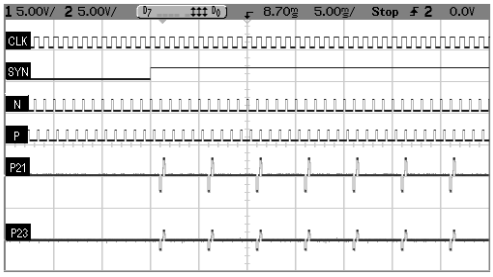


Fig. 10. Parallel stimulation of probes P21 and P23

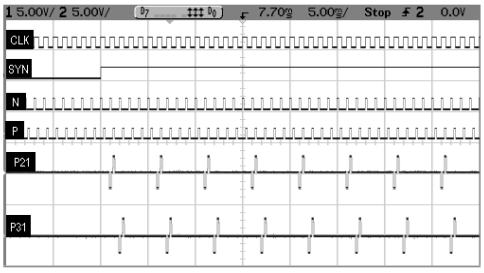


Fig. 11. Time multiplexed stimulation of probes P21 and P31

Test result of time-multiplexed stimulation is presented in Fig. 11. We have presented here the outputs of probes P21 and P31 only. P21 and P31 are the two probes of 1st column, but they belong to 2nd and 3rd rows of the array respectively. With the application of SYN pulse, probe P21 was excited after 1 cycle, while P31 after 2 cycles, but they have the same amplitude as both of them was excited by I_1. This demonstrates the time multiplexing stimulation among the rows. We have tested the chip for different frequencies and for different widths and interface delays by applying different currents, and found that the chip is working as designed.

III. Conclusion

We have designed, fabricated, and tested CMOS based scalable retinal implant chip. We have demonstrated that NS is capable of simultaneous stimulation of a large number of cells by biphasic current stimulus. With parallel multiplexing technique we can add as many columns of probes as we want, but we cannot increase the number of rows, as that will exceed the limit of persistence of vision. One unavoidable thing is that with each increase of column, additional CS is required. Multiplexing helped us design prosthesis with only a few components (e.g. 5 CSs, instead of 25) reducing the idle power dissipation to the bare minimum. NS has onboard flat probes, which eliminates the need of wiring them from the chip. We can also design components of wireless receiver in RIC to make it completely wireless or connect RIC to the wireless receiver through only five wires. For stimulation, RIC doesn't need address as is found in most of the prostheses. Sequential stimulation of each row by the clock is saving us from the wireless address transmission overhead. Programmable BWC and high resolution CS has made us possible to tune the prosthesis to suit the need of wide varieties of patients.

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