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A Transcutaneous Data Telemetry System Tolerant to Power Telemetry Interference

Mingcui Zhou, Wentai Liu, Guoxing Wang, Mohanasankar Sivaprakasam, Mehmet R. Yuce, James D. Weiland, and Mark S. Humayun

***Abstract*—Minimally-invasive implanted devices usually transmit both power and data through inductive coupling. By separating power and data carriers into different frequency bands, a high data rate can be transmitted without affecting power link efficiency. However in a dual band approach, the electromagnetic field from the power link interferes with data transmission. This paper presents a high data rate Differential Phase Shift Keying (DPSK) telemetry designed to tolerate interference without electromagnetic shielding or a high-order filter. On the transmitter side, by analyzing the nature of the interference, "frequency pre-distortion" is introduced to maintain the maximum efficiency. On the receiver side, a differential scheme is employed to provide inherent interference rejection. Using subsampling and novel analog demodulation, the scheme also eliminates the requirement of carrier recovery, thus reducing circuit complexity. The receiver achieves a 1Mbps data rate and can be upgraded to 2Mbps.**

I. Introduction

Inductive telemetry is commonly used for transmitting both power and data into implanted devices in a minimally-invasive method. In general, more information transmitted to the implant can improve the performance of prostheses such as cochlear and retinal implants. A high data rate telemetry is reported using Frequency Shift Keying (FSK) modulation in [1]. However, it suffers from low power efficiency since fast data modulation is directly applied to the power carrier. Usually the upper frequency of the power carrier in an implanted system is limited by coil self-resonant frequency and tissue absorption rate. Therefore fast modulation requires either a linear power amplifier or a low quality factor (Q) non-linear power amplifier. This results in low power efficiency of the transmitter, reduced battery life and increased device heating near the eye. One solution is to use a dual band approach by separating power and data into two frequency bands, achieving a high data rate without sacrificing efficiency of the power link. A problem arises in a dual band system where the strong electromagnetic field from the power link interferes with data transmission. This paper presents a high data rate Differential Phase Shift Keying (DPSK) telemetry robust to power interference without magnetic shielding or a high-order filter. On the transmitter side, "frequency pre-distortion" is introduced to maintain the maximum efficiency. On the receiver side, a differential scheme is employed to provide interference rejection. Using subsampling and novel analog demodulation, the scheme also eliminates the requirement of carrier recovery such as PLL and mixer circuits. This paper is organized as follows. Section II gives a brief overview of our dual band telemetry system. Section III describes the optimization of the transmitter under the strong interference from the power signal. Section IV explains the DPSK demodulation scheme with the simulation results. Section V gives the conclusion.

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M. Zhou, W. Liu, M. Sivaprakasam, and G. Wang are with the Electrical Engineering Department, University of California, Santa Cruz, Santa Cruz, CA 95064 USA (phone: 831-459-5766; e-mail: mingcui@soe.ucsc.edu, wentai@soe.ucsc.edu, mohan@soe.ucsc.edu, wgx@soe.ucsc.edu).

M. R. Yuce is with the School of Electrical Engineering and Computer Science, the University of Newcastle, Callaghan, NSW 2308, Australia (e-mail: mehmet.yuce@newcastle.edu.au).

J. D. Weiland and M. S. Humayun are with the Department of Ophthalmology, University of Southern California, Los Angeles, CA 90089, USA (e-mail: jweiland@usc.edu, humayun@usc.edu).

II. Dual Band Configuration

In our telemetry system, power and data are transmitted to the implants through two pairs of inductively coupled coils at different frequencies. As shown in Fig.1 (a), all four coils are placed coaxially to increase the coupling between the external and implanted coils. Furthermore, the implanted power and data coils are placed closely to reduce constraints on surgical operation. This configuration of coil placement

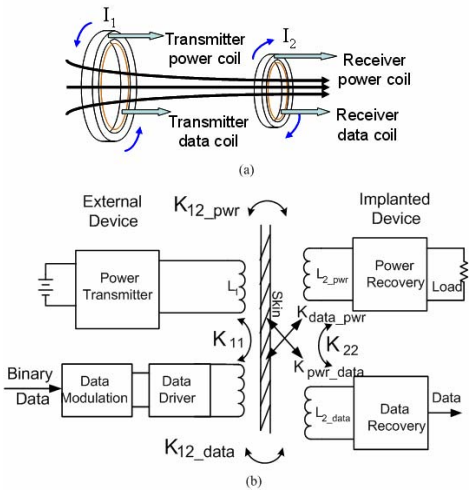

Fig.1 An overview of our telemetry system. (a) Placement of power and data coils. (b) Simplified diagram of the external and implanted devices.

has six coupling coefficients, among which K_{11}, K_{22}, K_{data_pwr}, and K_{pwr_data} relate to the electro-magnetic interference to the data transmitter and receiver. Due to physical proximity, the external power coil is the dominant interference source to the data transmitter, while both power coils affect the data signal on the receiver side.

III. Transmitter Optimization

A. Optimum Operation of the Class-E Amplifier

Power and data transmitters are both implemented using a Class-E amplifier, chosen for its high power efficiency [2] and its capability of *Q*-independent fast phase modulation [3]. The DPSK signal is generated by changing the amplifier input phase as described in [3]. As shown in Fig.2 (a), in a Class-E amplifier, the resonant tank consists of L, C, and C_1. R is the parasitic resistor of the inductor. The choke inductor supplies DC current to the resonant tank. The transistor turns on and off as a switch. Depending on the state of the switch (on/off), the resonant tank oscillates at different frequencies, but overall it completes a phase shift of 2π during one switching period. Therefore the switching frequency is equal to the carrier frequency. The inductor L in the resonant tank is a physical coil which transfers power or data through the magnetic coupling.

When the Class-E amplifier operates at the optimum state (also called the "tuned" state), the drain voltage of the transistor (V_{drain}) swings back to zero when the gate voltage (V_{gate}) becomes high, resulting in no power consumption by the transistor and ideally achieving 100% power efficiency. Fig.2 (b) shows the simulation result of a "tuned" Class-E amplifier for the data transmitter when no interference is present (*k*=0).

B. Frequency Shift

The Class-E amplifier for the data transmitter deviates from its tuned state when the external data coil is coupled to the power coil at a coupling coefficient (*k*) of 0.3. As shown in Fig.2 (c), under the interference from the power link, V_{drain} is not zero when the switch turns on. This results in energy loss on the transistor and an increase of power

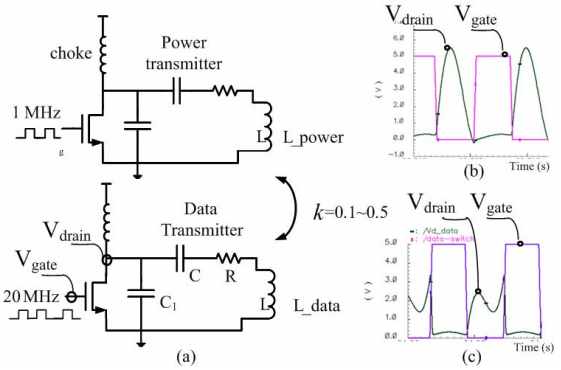

Fig.2 Transmission scheme (a) schematics of the power transmitter and data transmitter, (b), (c) Simulation results of the Class-E amplifier (data transmitter): (b) *k*=0 (c) *k*=0.3.

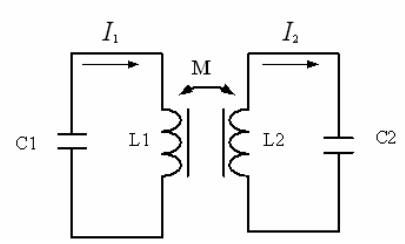

Fig.3 The linearized model of coupling between two resonant tanks

consumption by 2/3 compared to the original operation according to simulation results. This phenomenon is caused by the frequency shift of the resonant tank due to coil coupling.

In order to analyze the nature of the frequency shift, we use a simplified model to describe the resonant tank of a Class-E amplifier. Since the resonant tank completes a phase shift of 2π during one switching period, it is modeled as a simple LC tank whose oscillating frequency is equal to the carrier frequency. As shown in Fig.3, the two LC tanks represent the resonant tanks of the power and data transmitters, whose original frequencies are 1MHz and 20MHz. The mutual inductance indicates the magnetic coupling between two transmitter coils.

The mathematic expression of the model is shown in (1) and can be reorganized as (2). In (2), the solution of the eigenvalue in the matrix represents the frequency of the resonant tank, which is shown in (3).

$$V_1 = L_1 \frac{dI_1}{dt} + M \frac{dI_2}{dt} \tag{1.a}$$

$$V_2 = L_2 \frac{dI_2}{dt} + M \frac{dI_1}{dt} \tag{1.b}$$

$$C_1 \frac{dV_1}{dt} = -I_1 \tag{1.c}$$

$$C_2 \frac{dV_2}{dt} = -I_2 \tag{1.d}$$

where $M = k\sqrt{L_1 L_2}$,V_1 is the voltage on L_1 and V_2 is the voltage on L_2.

$$-\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} C_1 L_1 & C_1 M \\ C_2 M & C_2 L_2 \end{pmatrix} \frac{d^2}{dt} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix} \tag{2}$$

$$\frac{1}{\omega^2} = \frac{C_1 L_1 + C_2 L_2 \pm \sqrt{\left(C_1 L_1 + C_2 L_2\right)^2 - 4 C_1 C_2 \left(L_1 L_2 - M^2\right)}}{2} \tag{3}$$

When *k*=0, $\omega_1 = \frac{1}{\sqrt{L_1 C_1}}$, $\omega_2 = \frac{1}{\sqrt{L_2 C_2}}$ (4.a)

When *k*=1, $\omega_1 = \frac{1}{\sqrt{L_1 C_1 + L_2 C_2}}$, $\omega_2 = \infty$ (4.b)

The results in (3) and (4) show that the coupling between two coils results in frequencies splitting away from their original values. When $k \neq 0$, both resonant tanks will contain frequency components ω_1 and ω_2.

We will apply this analysis to the power and data transmitters in the dual band system. When no interference is present (*k*=0), the power and data resonant tanks remain at their original frequencies, where $\omega_1 = 1/(L_1 C_1)^{1/2}$ (1MHz

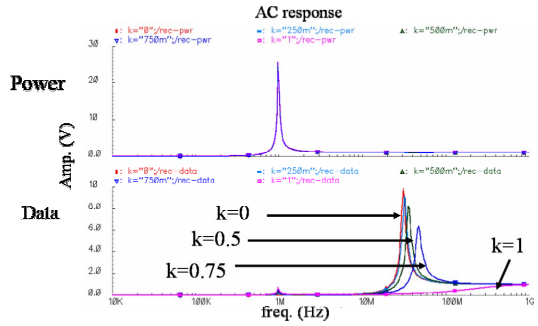

Fig.4 Simulation results of frequency shifts

power carrier) and $\omega_2=1/(L_2C_2)^{1/2}$ (20MHz data carrier). When $k\neq0$, ω_1' and ω_2' are the shifted frequencies. On the frequency down-shift side, $\omega_1'\approx\omega_1$ because $L_1C_1>>L_2C_2$. On the frequency up-shift side, different coupling coefficients result in different frequency shifts as shown in Fig.4. The larger the k is, the higher the shifted frequency is. When k =1, the upper frequency shifts to infinity. When L_1 (power) >> L_2 (data) and $\omega_1'\approx\omega_1$, the frequency of the power resonant tank is hardly affected due to the small amount of interference from the data transmitter. However, the data transmitter has a noticeable frequency shift in its resonant tank, causing the Class-E amplifier to deviate from its optimum operation state.

C. Frequency Pre-distortion

In order to compensate for the frequency shift in the data transmitter, frequency pre-distortion is proposed. The original frequency of the resonant tank is chosen to be lower than the carrier frequency; thus it shifts to the desired frequency under the interference. Unlike the coupling between the external and implanted coils, the coupling coefficient between two external coils (K_{11}) can be easily fixed. When k<1, the simulation results show that the Class-E amplifier can be re-tuned to its optimum state using frequency pre-distortion, maintaining its maximum power efficiency despite the strong interference.

IV. Receiver Design

A. Receiver Architecture

DPSK modulation is used for a data transfer rate of 1Mbps over a 20MHz carrier. A phase shift of 180° indicates "1", while 0° indicates "0". Fig. 5 shows the block diagram of the proposed DPSK receiver. The receiver data coil picks up the data signal as well as the strong power interference. At the front-end, a passive 1st-order high-pass filter is used to attenuate the interference. A band-limited amplifier buffers the signal for the demodulator and also provides anti-alias filtering. The signal is then sampled and compared to the samples from the previous symbol period. Since the phase can be translated to amplitude, a difference in amplitude between symbol samples indicates a 180° phase shift (a "1"), while no difference indicates 0° phase shift (a "0").

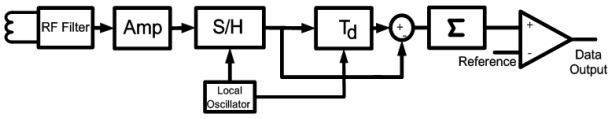

Fig. 5 Block diagram of the DPSK receiver

The proposed demodulation scheme uses subsampling, where the sampling frequency is lower than the carrier frequency. The subsampling clock is provided by a local crystal oscillator. It is chosen according to the carrier frequency $f_s=4f_c/(2n+1)$, where f_s is the sampling frequency, f_c is the carrier frequency, and n is an integer larger than 1 [4]. In this design, for a carrier frequency f_c=20MHz and n=2, the sampling frequency f_s is 16MHz. The relationship between the sampling frequency and carrier frequency ensures that the samples will not always occur at the zero crossing point of the received data carrier. The phase drift of the sampling clock due to frequency deviation will not affect the result because with the two adjacent symbols being compared, the phase drift is small and hence negligible within a symbol period. Therefore carrier recovery circuits such as PLL and mixer can be eliminated.

B. Interference Rejection

Using the differential demodulation of a DPSK signal, the periodic interference can be rejected. Since the power link signal uses a 1MHz carrier frequency, data signals sampled 1µs apart are affected by power link interference with the same magnitude. When the data rate is 1Mbps, the sampled DPSK signal is compared to its previous symbol which is exactly 1µs ahead (one symbol period). By taking the analog difference of the sampled data, the interference becomes a common-mode signal and is cancelled.

Note that this scheme is also applicable when the symbol rate is higher than the power frequency. For example, when the power interference remains at 1MHz and the data rate increases to 2Mbps, the DPSK signal can be coded in such a way that each sample is compared to its counterpart from two-symbol-periods earlier to counteract the interference effect.

C. Circuit Implementation

Fig. 6 shows the simplified circuit diagram for data demodulation. The current data samples are stored on a

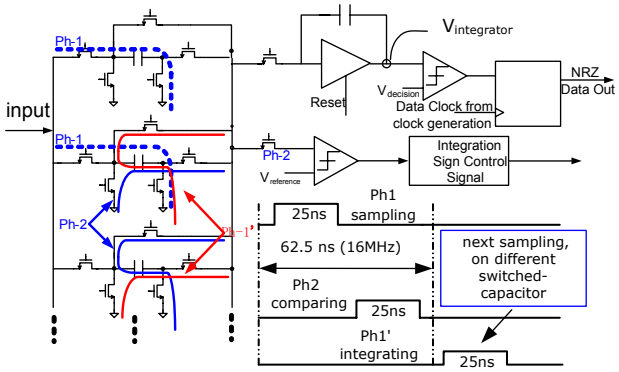

Fig. 6 Simplified circuit diagram for the demodulator

switched-capacitor array, waiting to be compared with samples of the next symbol period. During phase-1 (Ph-1), one sampled signal is simultaneously stored on two capacitors (dotted path), one for comparing with the corresponding sample from the previous symbol, the other for comparing with the sample of the next symbol. Phase-2 (Ph-2) computes the analog difference between the current sample and its previous counterpart (continuous path). The sign of the analog difference is detected using a comparator. Phase-1' (Ph-1') sums up the absolute value of the analog difference (continuous path). The output of the integrator is equal to the sum of the absolute difference between the current symbol and the previous symbol, and it is reset at every symbol edge. Before each reset, if the integrator output is below the reference voltage, two adjacent symbols are assumed to have no phase difference, representing "0". If the integrator output is larger than the reference voltage, two adjacent symbols are assumed to have different phases, representing "1".

D. Synchronization from Preamble

A data clock is used to reset the integrator at each symbol edge. The 1MHz data clock frequency is derived from a 16MHz sampling clock with 16 possible phases. The clock phase closest to the symbol edge is searched and captured during the preamble sequence "1, 0, 1, 0…" The integrator reset is first chosen arbitrarily from 16 possible phases, and then it is shifted by one sampling period after every two symbol periods. As shown in Fig. 7, a and b are the integrator outputs right before each reset. When the integrator is reset at the middle of a symbol, a=b; the sign of (a-b) changes whenever the reset phase passes the mid-symbol point. Therefore, by detecting this sign change of (a-b), we can locate the reset phase closest to the symbol edge by delaying the mid-symbol phase for eight sampling periods. In the worst case, the edge is captured in 34 symbol periods where all 16 possible phases are searched before finding the one closest to the symbol edge. Therefore, at the beginning of each data package, a 36-bit preamble signal is used for synchronization. In order to compensate for the phase drift due to crystal frequency deviation, the symbol edge is recaptured at the beginning of every data packet.

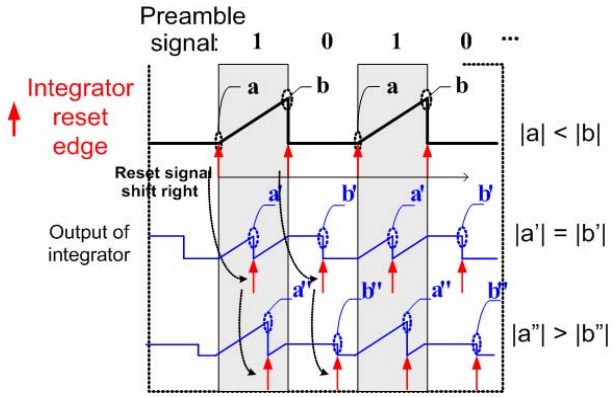

Fig. 7 Output of the integrator during preamble sequence

E. Simulation Results

The simulation results are shown in Fig. 8. From top to bottom, the waveforms are digital DPSK signal at the input of the data transmitter, input of the demodulator (after filter), output of the integrator, and the demodulated binary data. The circled parts in the picture indicate 180° phase shifts which represent "1" for DPSK signal. The simulation results show that after filtering, even with interference stronger than the data signal, the demodulator can still recover the data correctly, demonstrating the interference tolerance of our scheme.

V. Conclusion

A data telemetry designed for dual band systems is optimized in the following aspects. By using frequency pre-distortion, the data transmitter maintains its maximum power efficiency despite the frequency-shift under the strong interference from the power telemetry. By using subsampling and analog demodulation, we eliminate high order filters and the requirement of carrier recovery such as PLL and mixer. Simulations show that the receiver is able to achieve a 1Mbps data rate and can be upgraded to 2Mbps with the total power consumption of 6mW for the receiver.

References

[1] M. Ghovanloo, K. Najafi, "A wideband frequency-shift keying wireless link for inductively powered biomedical implants," *IEEE Transactions on Circuits and Systems I*, pp. 2374-2383, Dec. 2004.

[2] N. O. Sokal and A. D. Sokal, "Class-E--A new class of high-efficiency tuned single-ended switching power amplifiers," IEEE *J. Solid-State Circuits*, vol. 10, pp. 168-176, June 1975.

[3] G. Wang, W. Liu, M. Sivaprakasam, M. Zhou, J. D. Weiland, and M. S. Humayun, "A wireless phase shift keying transmitter with Q-independent phase transition time," *Proc. IEEE 27th EMBS Conference*, Sept. 2005.

[4] M.Yuce, "A Differential-based multiple bit rate PSK receiver: theory, architecture, and SOI CMOS implementation," Ph.D. thesis, North Carolina State University, Raleigh, NC, United States, 2004.

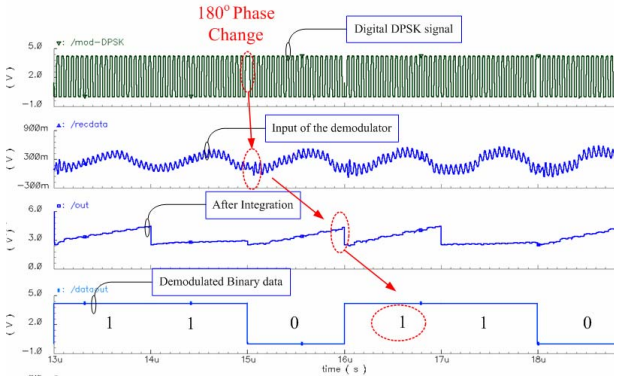

Fig. 8 Simulation results, from top: digital DPSK signal at the input of the data transmitter, input of the demodulator (after filter), output of the integrator, and the demodulated binary data.