

A multi-chip-architecture based flexible stimulation device for retinal prosthesis with a flip-chip packaging technique

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Abstract— In the present work, we designed a multi-chip-architecture based flexible neural stimulation device for retinal prosthesis. Based on the multi-chip architecture, a novel CMOS stimulation device was successfully designed and characterized. A packaging technique for thin, flexible neural stimulation device was also proposed and demonstrated. Flip-chip bonding technology plays an essential role in the fabrication of the present thin and flexible neural stimulation device.

I. INTRODUCTION

IN the last decade, variations of LSI-based prosthesis technologies have been proposed and demonstrated. Retinal prosthesis is one of the most major and most expected applications, and a lot of efforts have been dedicated for the development of the retinal prosthesis technologies [1-5]. In some major retinal diseases such as age-related macular degeneration (AMD) and retinitis pigmentosa (RP), only the visual cells were seriously damaged but the neural cells such as retinal ganglion cells (RGC) are partially remained. The retinal prosthesis technology aims to provide substitutional visual functionality for such patients.

We have been developing LSI-based retinal prosthesis devices taking approach of suprachoroidal transretinal Stimulation (STS) and subretinal stimulation [6-8]. Two dimensionally patterned electric stimulation on the remained retinal neural cells is expected to evoke images consists of phosphenes. The structure of the retinal stimulation device is one of the largest issues in the development of the retinal prosthesis technology. Considering the quality of the prosthetic image evoked by the retinal stimulation, the retinal

stimulation device should be LSI based device. The simple multiple electrodes without demultiplexer LSI is not acceptable because of the number of interconnections. However, since Si, material of the LSI device is rigid and a single-chip stimulator device cannot be used for retinal prosthetic applications. To overcome this issue, we have proposed "multi-chip architecture" to configure a thin, flexible retinal stimulation device [6-8].

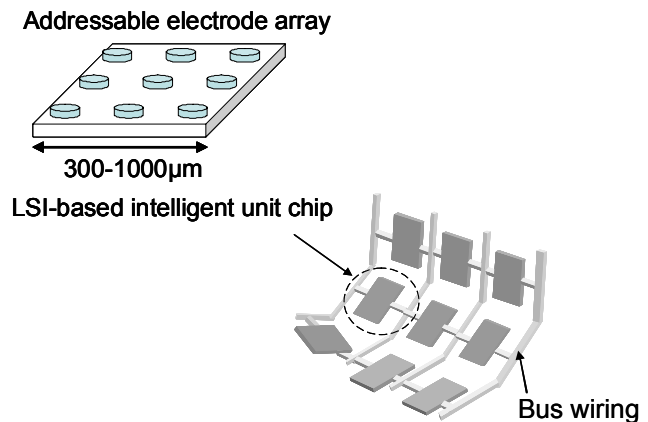


Fig. 1. Concept of the multi-chip thin and flexible retinal stimulation device

In this work, based on the proposed architecture, we designed an LSI stimulation device and developed a new packaging structure with higher reliability and durability for biological environment. Fig. 1 shows the concept of the multi-chip thin and flexible retinal stimulation device.

II. DESIGN AND CHARACTERISTICS OF THE MULTI-CHIP RETINAL STIMULATION DEVICE

A. Neural stimulation device with multi-chip architecture

The multi-chip retinal stimulation device consists of small-sized unit chips which can work in stand alone. Fig. 2 shows layout and block diagram of the present unit chip. Table 1 shows the specification of the unit chip, comparing with the previous proto-type device [6, 7].

Manuscript received April 3, 2006. This work was supported in part by the "Artificial Vision System" project of the New Energy Development Organization (NEDO) of Japan, and Health and Labor Sciences Research Grants, Japan.

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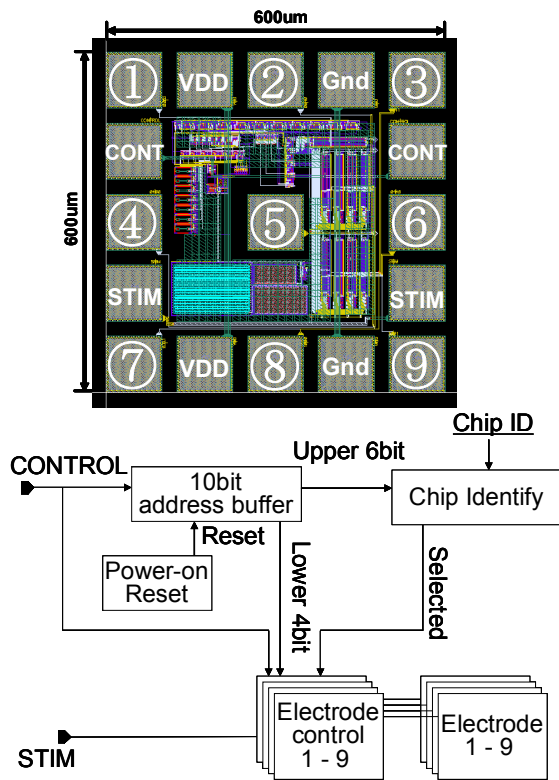


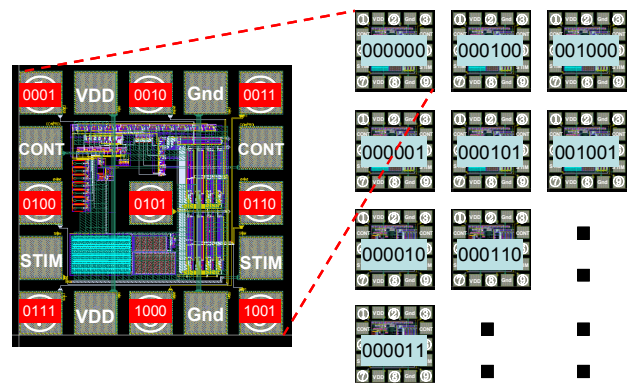
Fig. 2. Layout and block diagram of the unit chip.

TABLE I
SPECIFICATIONS OF THE RETINAL STIMULATION DEVICE

	Present device	Previous prototype [6,7]
Fabrication Process	0.35µm 2-poly 4-metal standard CMOS	0.6µm 2-poly 6-metal standard CMOS
Unit chip size	600µm x 600µm	600µm x 600µm
Series resistance	~200 Ω	~1k Ω
Reset sequence	Power on reset	Logic
Number of electrodes per unit chip	9	9
Address space for unit chip (Max. No. of unit chips)	6 bit (64)	4 bit (16)
Max. No. of electrodes in multi-chip device	576	144

The unit chip has a size of 600µm x 600µm. It has nine stimulation pads and four input lines including the power

supply lines. Each stimulation pads has unique 4-bit address to selectively activate the electrodes. The four input lines are; VDD, GND, CONTROL, and STIM. VDD and GND lines are for power supply (5V and 0V DC). The control and neural stimulation can be achieved with only two lines; CONTROL and STIM. The basic operating sequence for the chip is basically compatible with that was designed in the previous works. One of the stimulation electrodes can be selected with the number of the pulses applied on the CONTROL line. The unit chip counts the pulses applied on the CONTROL line with 10-bit address buffer. The lower 4 bit for the address buffer was used for electrode selection, and the upper 6 bits, as shown in Fig. 3.



Electrode address Unit chip address

Fig. 3. Address assignment for electrodes and unit chips.

One of the stimulation electrodes is selected according to the value in the lower 4 bits of the address buffer. The 6-bits address space for unit chips enables to control arbitrary number of unit chips (up to 64) with only one set of input lines. Therefore, the present multi-chip stimulation device platform can be configured in 64-chip device with 576 stimulation electrodes. For the sake of flexibility, the unit chip array should be assembled in 1000 - 1200µm pitch. Area of 64-chip device is estimated to be approximately 58 - 80 mm² and it is expected to cover the important part of the human retina.

B. Power on reset

The reset of the address buffer is important to correctly select the unit chip and stimulation electrode. To ensure a consistency between the addressed stored in the unit chips, a reliable reset mechanism is required. We implemented a simply configured power-on-reset (POR) circuitry. The unit chip is automatically reset when the DC power is supplied. An R-C retardation circuitry was implemented to ensure the power-on-reset operation. Owing to this mechanism, the STIM line can be used only for current-controlled stimulation onto

the retina.

C. Series resistance for neural stimulation

Fig. 4 shows (a) series resistance between the STIM input and selected stimulation electrode, and (b) leakage current into un-selected stimulation electrode.

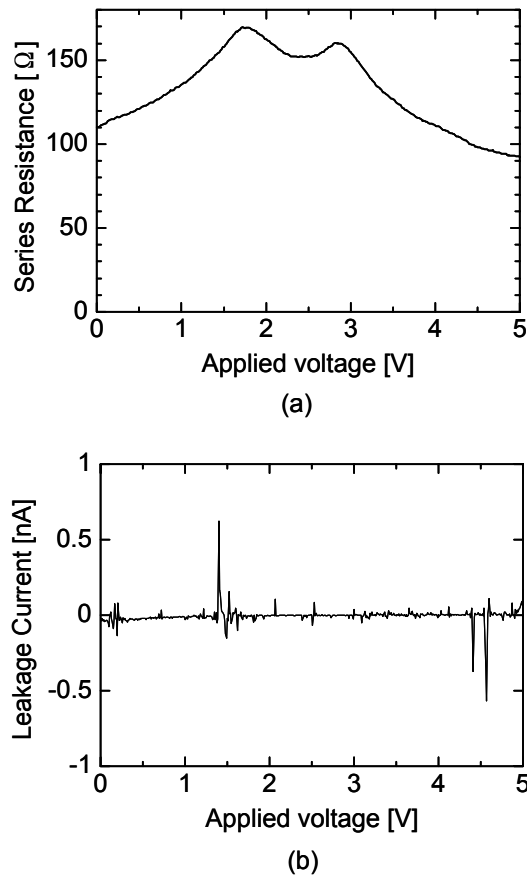


Fig. 4 (a) Series resistance between the STIM input and selected stimulation electrode, and (b) leakage current into un-selected stimulation electrode.

Since the connection between STIM input and selected stimulation electrode is established with a transmission-gate type switch, the series resistance shown in Fig. 4(a) depends on the input voltage. The maximum series resistance is smaller than $180\ \Omega$. It corresponds to 180mV for 1mA stimulation. On the other hand, the resistance between STIM input and un-selected stimulation electrode is larger than $1\text{G}\ \Omega$. It guarantees that leakage current via un-selected electrodes is smaller than 1nA , as shown in Fig. 4 (b). These series resistances are expected to be sufficient to carry out current-controlled retinal stimulation.

III. NOVEL MULTI-CHIP PACKAGING USING FLIP-CHIP TECHNOLOGY

In the previous works, we have developed a device packaging for multi-chip thin and flexible neural stimulation device [6, 7]. The aligned unit chips were bonded on a polyimide flexible substrate. Top surface of the unit chips with Pt/Au bump electrodes are molded with an epoxy resin layer keeping the top of the Pt/Au electrodes exposed. In that process, the unit chips were sealed with the epoxy resin layer from biological environment. Since a lot of stimulation electrode penetrates the epoxy resin layer, the yield of the packaging process was not sufficiently good (less than 50%). The durability of the seal quality should be improved, too. In order to improve the yield to seal quality, it is favorable not to form the stimulation electrode directly on the unit chips. The unit chips should be molded with smallest seal length, or between waterproof films. To achieve a better seal quality, we propose and demonstrate a new device structure and packaging process.

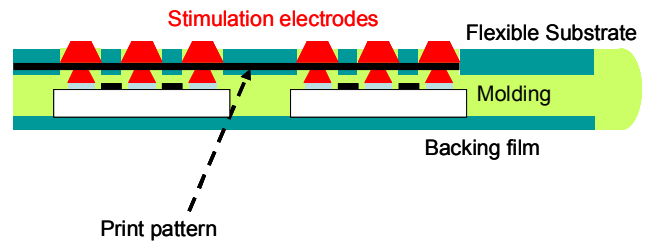


Fig. 5 The structure of the proposed retinal stimulation device.

Fig. 5 shows the proposed structure for multi-chip thin and flexible retinal stimulation device. A single layer polyimide flexible substrate with metal pattern is prepared to supply signals to the unit chips and interconnect the unit chips and stimulation electrodes. The unit chips are placed between the polyimide flexible substrate and another backing film. Fig. 6 shows the packaging process of the multi-chip stimulation device shown in Fig. 5.

We design and fabricate an arrayed unit chips in one die. At first, grooves to separate the unit chips are formed. Connection bumps for flip-chip bonding are formed on the pads of the unit chips. We use Au ball bump as the connection bumps. Then the die is bonded onto the backside of the flexible patterned substrate with flip-chip bonding technique. Bump electrodes were formed on the top of the flexible substrate. Then, the bottom of the die was grinded and the unit chips are separated. The separated unit chips were molded with molding material and backing film.

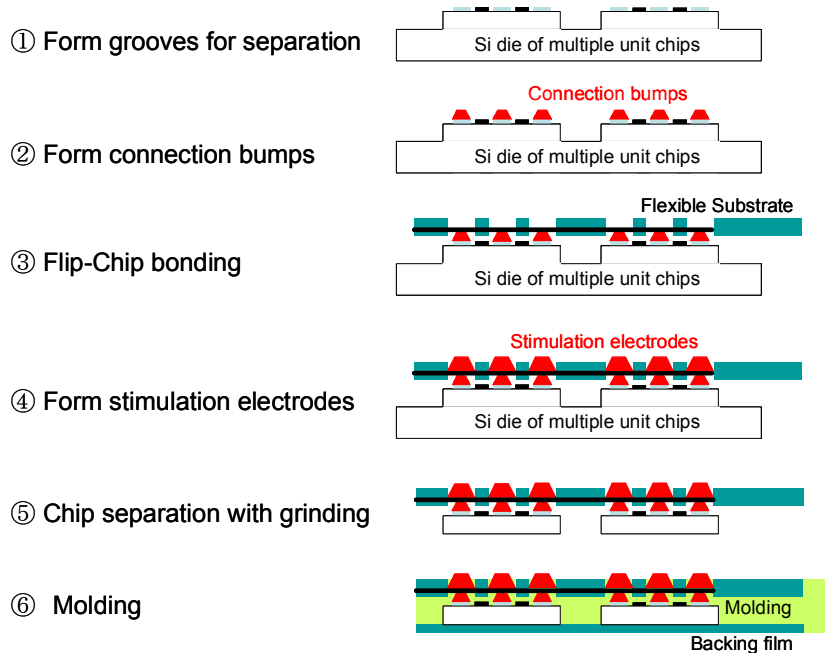


Fig. 6 Packaging process for the retinal stimulation device.

Fig. 7 shows a model device in which Si dummy wafers with the size of the unit chips are assembled with the proposed fabrication process. The model shows that a retinal stimulation device fabricated with the proposed packaging has acceptable thickness (approximately $250\mu\text{m}$), and enough flexibility to fit eyes of the human and other mammals. Process optimization for the CMOS unit chips shown in Fig. 2 are now undergoing, and will be presented at the conference with performance of the assembled thin and flexible stimulation device.

IV. CONCLUSION

Based on multi-chip architecture, thin and flexible retinal stimulation device was proposed and fabricated. The present stimulation device has 6-bit address space for identification of the unit chip. We can configure 64-unit chips, 576 stimulation electrodes which will cover the most of the essential retinal area for visual sensation. Not only device circuitry, but also the new device packaging was proposed. In order to achieve better process yield and reliability, we developed a new structure with flip-chip bonding technology. We confirmed the proposed structure is feasible to realize multi-chip retinal stimulation device with enough thinness and flexibility.

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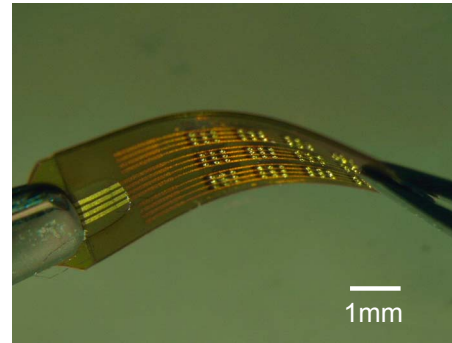


Fig. 7 Assembled model for the retinal stimulation device with flip-chip bonding technology ($600\mu\text{m} \times 600\mu\text{m} \times 50\mu\text{m}$ Si wafers were aligned and molded in 3×4 array.)

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