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VLSI Implementation of a Nonlinear Neuronal Model: A "Neural Prosthesis" to Restore Hippocampal Trisynaptic Dynamics

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Abstract— **We are developing a biomimetic electronic neural prosthesis to replace regions of the hippocampal brain area that have been damaged by disease or insult. We have used the hippocampal slice preparation as the first step in developing such a prosthesis. The major intrinsic circuitry of the hippocampus consists of an excitatory cascade involving the Dentate Gyrus (DG), CA3, and CA1 subregions; this trisynaptic circuit can be maintained in a transverse slice preparation. Our demonstration of a neural prosthesis for the hippocampal slice involves: (i) surgically removing CA3 function from the trisynaptic circuit by transecting CA3 axons, (ii) replacing biological CA3 function with a hardware VLSI (very large scale integration) model of the nonlinear dynamics of CA3, and (iii) through a specially designed multi-site electrode array, transmitting DG output to the hardware device, and routing the hardware device output to the synaptic inputs of the CA1 subregion, thus by-passing the damaged CA3. Field EPSPs were recorded from the CA1 dendritic zone in intact slices and "hybrid" DG-VLSI-CA1 slices. Results show excellent agreement between data from intact slices and transected slices with the hardware-substituted CA3: propagation of temporal patterns of activity from DG→VLSI→CA1 reproduces that observed experimentally in the biological DG→CA3→CA1 circuit.**

I. Introduction

We are developing a neural prosthesis to replace hippocampal brain function that is lost due to stroke, epilepsy, or dementia. In doing so, we seek to restore long-term memory formation that depends on the hippocampus, and that often is severely diminished in brain-damaged and Alzheimer's patients. Our concept of such a prosthesis is a biomimetic model of the nonlinear dynamics of the hippocampus – a model that captures how hippocampal circuitry re-encodes, or transforms, incoming spatio-temporal patterns of neural activity (i.e., the contents of short-term memory) into outgoing spatio-temporal patterns of neural activity (i.e., the contents of long-term memory) [1]. Multi-site electrode arrays capable of both electrophysiological recording and electrical stimulation would couple such a biomimetic model to undamaged regions of the brain afferent (before) and efferent (after) to the damage. Thus, through bi-directional communication with the brain, the prosthetic system could "by-pass" the damaged tissue, and allows the biomimetic model to substitute for lost hippocampal function.

Because of the complexity of such a goal, we have used the hippocampal slice preparation as the first step in developing such a prosthesis. The major intrinsic circuitry of the hippocampus consists of an excitatory cascade involving the Dentate Gyrus (DG), CA3, and CA1 subregions; this trisynaptic circuit can be maintained in a transverse slice preparation. Our demonstration of a neural prosthesis for the hippocampal slice involves: (i) surgically removing CA3 function from the trisynaptic circuit by transecting CA3 axons, (ii) replacing biological CA3 function with a hardware model of the nonlinear dynamics of CA3, and (iii) through a specially designed multi-site electrode array, transmitting DG output to the hardware device, and routing the hardware device output to the synaptic inputs of the CA1 subregion, thus by-passing the damaged CA3.

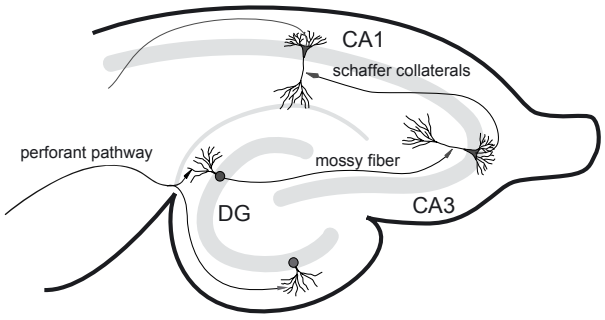

Fig. 1. The intrinsic trisynaptic pathway in a hippocampus slice. The main intrinsic circuitry of the hippocampus consists of three major subregions: DG, CA3, and CA1. Input signals from perforant path fibers excite DG granule cells. DG output, in turn, excites CA3 pyramidal cells through mossy fibers. Output from CA3 is transmitted to CA1 pyramidal cells. This so-called "trisynaptic pathway" is considered to be the principal network involved in hippocampal neuronal information processing.

An important component of our hippocampal prosthesis is implementation of the biomimetic model in hardware, to achieve miniaturization, parallel processing, and rapid computational speed. We have previously shown

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replacement of the CA3 region of the slice as described above with a biomimetic model of CA3 nonlinear dynamics implemented using a Field Programmable Gate Array (FPGA) [2]. Recently, we have successfully designed and fabricated a VLSI (very large scale integration) microchip based on our FPGA model. Here we demonstrate replacement of CA3 using a VLSI implementation of the biomimetic model. The data presented in this article was collected with both the FPGA and VLSI devices. Within each experiment, the nonlinear model of CA3 dynamics was simulated and then implemented into the hardware device. The results show that the propagation of spatio-temporal patterns of activity from the intact slice model (DG→CA3→CA1) can be reproduced in a replacement model (DG→VLSI→CA1).

II. Materials and Methods

A. Hippocampal Slice Preparations

Hippocampal slices were prepared from 8-10 week old male Sprague-Dawley rats (250-300 gm). Animals were first anesthetized with halothane and then decapitated. Their skulls were rapidly removed and the brain was carefully extracted. Hippocampi were separated from the cortex within iced sucrose buffer solution. Four hundred micron thick hippocampal slices were cut transversely from ventral hippocampi using a vibratome. This protocol was approved by the Department of Animal Resources and Institutional Animal Care at the University of Southern California. Slices were incubated for at least one hour in 2mM $MgSO_4$ artificial cerebral spinal fluid (aCSF) at room temperature. During each electrophysiological recording session, one slice at a time was transferred to a Multichannel Systems Multi Electrode Array (MEA) system containing a chamber perfused with normal aCSF (NaCl 128mM, KCl 2.5 mM, NaH_2PO_4 1.25 mM, $NaHCO_3$ 26 mM, Glucose 10 mM, $MgSO_4$ 1 mM, Ascorbic Acid 2 mM, $CaCl_2$ 2mM), and maintained at room temperature (25-26 ºC). In order to reduce inhibition from CA3 mossy fibers, 2.5-5 μM picrotoxin was added to the aCSF. All solutions were bubbled with 95%O_2 and 5%CO_2 mixed gas.

B. Recording and Stimulation

Extracellular recording: Electrophysiology data was collected by an extracellular recording MEA system (www.mutilchannelsystems.com). Our MEA system consists of pre-amps, a data acquisition device, and software operated with a custom-built, 60-channel conformal planar multielectrode array [3]. The geometry of this conformal array was designed to match the cytoarchitecture of hippocampus slices. The electrodes of this conformal array are platinum based. Data were collected at a sampling frequency of 10 kHz per channel with a gain of 1200 and recorded using MCRack (v3.2.1.0).

External electrode stimulation: Electrical stimulation was applied to the perforant pathway (PP) of each slice with an external electrode to generate electrophysiological responses throughout the trisynaptic pathway (evoked field potential responses in DG, CA3, and CA1). When the full trisynaptic response was observed, we then stimulated the slice with a series of random impulse trains (RITs). Four 300-pulse Poisson distributed RITs consisting of fixed current intensity (biphasic, 100-300 μA) were delivered to the PP by an external bipolar electrode of twisted Nichrome wires. A 5-7 minute waiting period occurred between each RIT.

Internal electrode stimulation: During the replacement experiment hardware generated biphasic current stimulation was sent to the stratum radiatum of CA1 through a pair of microelectrodes in the MEA. The current was first set at 50% of maximal intensity based on the I/O curve (Fig. 3, 50-70 μA) and fine adjustments were applied as necessary.

C. Removing CA3 Function from the Trisynaptic Circuit

To remove the contribution of CA3 from the trisynaptic circuit of the hippocampal slice, we used a sharpened piece of Poly Dimethyl Siloxane rubber (PDMS) that was fixed and stabilized by an 18 gauge syringe needle. This cutting device was held by a micromanipulator. Before placing the slice on the array, the relative coordinates for positioning the cutting device was measured and marked to correspond to the region of CA3 axons projecting to CA1.

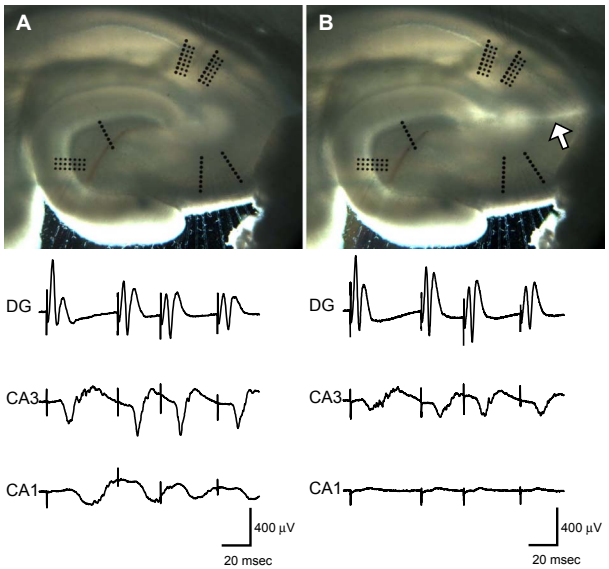

Fig. 2. Confirmation of removing CA3 function from the trisynaptic circuit. Typical trisynaptic responses recorded in a quadruplet train in A) intact slice. No CA1 responses were triggered in B) transected slice. The location of transection is indicated by the arrow.

To confirm that the CA3 to CA1 pathway was successfully transected, we applied a four pulse train of stimulation to the PP and measured the response in CA1. Figure 2A shows typical trisynaptic responses recorded from an intact slice in the DG, CA3, and CA1 subregions. In Fig. 2B, no CA1 EPSPs are observed in a slice with transected CA3 axons. To verify that properties of synaptic transmission in CA1 were not significantly altered after transecting CA3 efferents, paired-pulse stimulation was applied to the stratum radiatum

of CA1 (the region of CA3 afferents to CA1) before and after the transection process. The paired-pulse stimulation protocol included current intensities ranging from 10 to 100 μA, with 10 μA increments, and a 30ms inter-pulse interval. In Fig. 3, typical paired-pulse facilitation is observed (difference in field EPSP amplitude to the 1st and 2nd pulses). Although the I/O curves show a slight increase in amplitudes of field EPSPs to both 1st and 2nd pulses, the differences at 50% of maximal intensity (the intensity used during random train stimulation) is negligible. Hence, fundamental properties of synaptic transmission in CA1 are preserved.

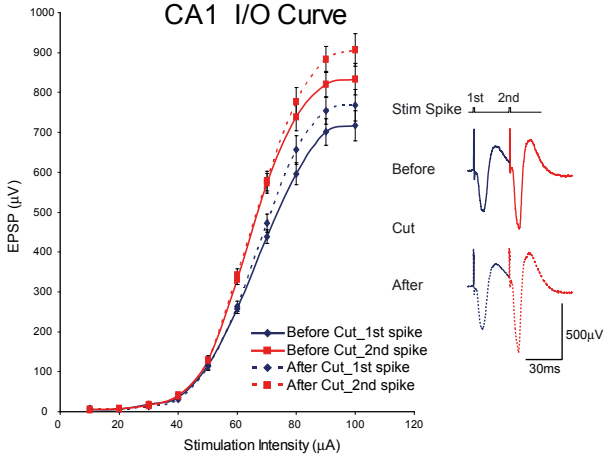

Fig. 3. CA1 I/O curve in intact and damage slice model. Paired-pulse stimulation was applied. The response of the first stimulus was presented in black diamonds and the response of the second stimulus was presented in gray squares. The full line shows the intact slice and the dash line shows the transected slice response.

D. CA3 Modeling Approach

A single input/output Volterra-Poisson model was used to represent the nonlinear dynamics of CA3 function. From the recorded datasets, amplitudes of DG population spikes (PSs) were used as measures of the input to CA3, and amplitudes of CA3 PSs were used as measures of system output. Model estimation was completed using PS amplitudes and interspike intervals of the input/output sequences. The nonlinear input/output characteristics are defined in terms of the kernels (k_i) of a functional power series of the following form [4]:

$$y(n_i) = A_i k_1 + A_i \sum_{n_i-\mu<n_j<n_i} A_j k_2(n_i - n_j) + A_i \sum_{n_i-\mu<n_{j_1}<n_i} \sum_{n_i-\mu<n_{j_2}<n_i} A_{j_1} A_{j_2} k_3(n_i - n_{j_1}, n_i - n_{j_2})$$

where A_i, A_j represent the varying amplitudes of PSs recorded at the DG (input), $y(n_i)$ represents the PS amplitudes recorded at CA3 (output) and k_1, k_2, and k_3 are the 1st, 2nd, and 3rd order kernels respectively. n_i is the time of occurrence of the current impulse in the input/output sequence and n_j is the time of occurrence of the j^{th} impulse prior to the present impulse within the kernel memory window μ. Estimation of the kernels is facilitated by expanding them on the orthonormal basis of Laguerre polynomials, the coefficients of which can be obtained via least squares method.

E. VLSI Implementation

To replace CA3 function, the entire input/output (DG to CA3) response system of the hardware implementation is depicted in Fig. 4. This device has three major interfaces to: the host PCI system, an analog-to-digital converter, and to a digital-to-analog converter. The PCI provides a primary 33 MHz clock and all other slower clocks used in the design are derived from the primary using clock synthesis. The PCI control buses give the commands to upload the values to registers inside the chip through proper address decoding. Some diagnostic values can be read from the chip back to the host. The incoming neural signal was amplified with a 1200 gain to get a suitable signal range for TI TLC4541 5V ADC running in 10 kHz. After converting to the digital domain, each extracted amplitude is represented using unsigned 16 bits as 0000 (Hex) for -5V and FFFF (Hex) for 5V. A Finite State Machine is responsible for generating control signals for the data path blocks such as spike detection, polynomial update, output response generator, and biphasic output waveform generator. Since the computation has to be executed rapidly enough so that it will complete before the next PS, the Laguerre polynomial update and output generator sub-blocks are at a rate of 2.6 MHz. The spike detection runs at 10 KHz and waveform generator block at 20 KHz to meet the ADC and DAC data throughput speed.

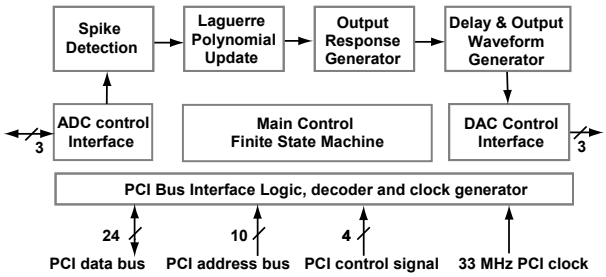

Fig. 4. Block diagram of the VLSI

The design was implemented using VHDL language and simulated by Mentor-Graphics ModelSim. After logic synthesis, placement, and routing using standard cells, the VLSI was fabricated using a TSMC 0.18 μm process with a 1.1 mm^2 area. The die photo is shown in Fig. 5. Total gate count after synthesis is 2000, and the whole chip consumes only 230 nW (excluding the peripheral data converters).

F. Experiment Protocol

(1) Preparing Hippocampus slices
(2) Positioning the slice over the conformal MEA
(3) Stimulating the PP with RITs, Recording the trisynaptic responses in DG, CA3 and CA1
(4) Building a mathematical model of the CA3 subregion
(5) Loading the Laguerre coefficients into FPGA/VLSI device
(6) Terminating the CA3-CA1 connections

(7) Stimulating the PP with the same RITs, recording the responses in DG and CA1

(8) Comparing CA1 response from (3) and (7)

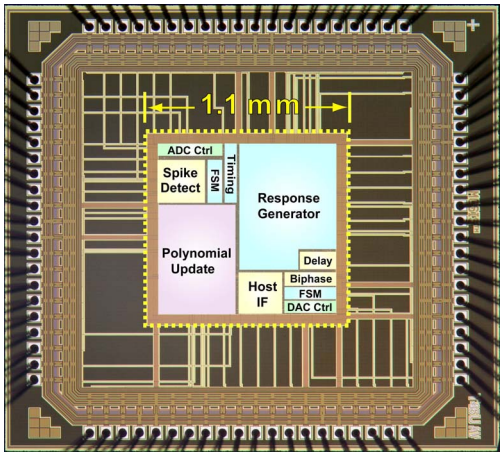

Fig. 5. The die photo of the VLSI implants. (Fabricated by TSMC 0.18 CMOS with a 1.1 mm^2 area)

III. Results

Neuronal signals that represent the output from the DG provided the input to the VLSI-based biomimetic model of CA3 nonlinear dynamics. Output from the VLSI device, which represents the equivalent of responses from CA3, provided the activation of synaptic inputs to CA1. In total, the system processed real-time signals from DG, and utilizing the VLSI computational kernel model, both transformed those DG inputs into biologically appropriate CA3 outputs, and converted those outputs into biphasic current stimulation. The stimulation was then sent to the CA1 subregion to induce field EPSPs (Fig. 6).

Fig. 6. In the transected slice model, DG was elicited from RITs stimulation (upper traces) and the signal was connected to the VLSI device where DG spike analyzing, CA3 kernel model prediction, and biphasic output generation were processed in real-time (middle box). CA1 field EPSPs were induced by the "hybrid" model (lower trace).

Results from five successful experiments (all phases completed) are reported here. Examples from two of those five are shown in Fig. 7. Each panel illustrates results from one experiment: amplitudes of population EPSPs recorded from the CA1 region are shown as a function of 50 impulses chosen from among 2,400 impulses of the random trains (1,200 administered before transecting inputs to CA3; 1,200 administered after transection). Time intervals between impulses are not represented in the figures; only "Input Event" number (sequence of sample impulses) is shown to collapse the x-axis. Data for the intact slice (CA1 trisynaptic) are shown in black squares; data for the "hybrid" slice with the substituted FPGA model of CA3 (CA1 replacement) are shown in gray diamond. For what is a wide range of intervals captured in this 50-impulse sequence, and what is a 3-5 fold difference in population EPSP amplitude, CA1 output from the hybrid slice matches extremely well the CA1 output from the intact slice. The accuracy of the amplitude comparison was evaluated using the normalized mean square error (NMSE) of the amplitude and the average NMSE was 12.5%. More experiments and quantification studies are in progress now to optimize the system. In the future, the major focus will be on reducing the CA1 NMSE and expanding to multi-channel model.

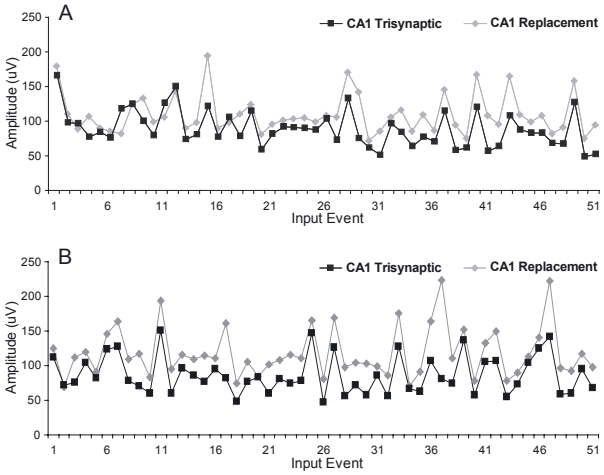

Fig. 7. A Comparison of CA1 field EPSP amplitudes in response to RIT stimulation in the intact slice ("CA1 Trisynaptic" in black squares) and after replacement of subregion CA3 with A) FPGA and B) VLSI ("CA1 Replacement" in gray diamonds).

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