

# Active Electrode Arrays by Chip Embedding in a Flexible Silicone Carrier

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**Abstract** – Future cochlear implants demand a higher density of stimulation sites (electrodes) and enhanced functionality (e.g. feedback information). The current generation of implanted cochlear prostheses is making use of a completely “passive scheme” and cannot meet these requirements. An “all-Silicon” concept integrating active components with passive electrodes in Silicon has been proposed but does not offer the flexibility/stretchability of current silicone-based devices. This paper introduces a novel concept based on Silicon chip embedding in a flexible silicone carrier. The process and experimental results will be presented. The concept is also applicable to other types of implanted electrodes, e.g. retinal implants.

## I. INTRODUCTION

In the area of medical implants, cochlear prostheses are one of the main driving applications for new technological developments. Indeed, although about 100.000 persons worldwide have already received such devices, there still is a need for improved performances, e.g. increased number of channels or electrodes [1], [2]. Generally speaking, in the field of electro stimulated biomedical implants, higher electrode densities are becoming of growing interest.

At the same time, the importance of MEMS in the fields of biological or medical applications has been in constant expansion. The development of so-called biomicro-electromechanical systems (bio-MEMS) has become more and more popular [3]. With bio-MEMS, next to stimulation, the possibility for enhanced functionality is made possible. One example of this is the feedback of data from the stimulated region, with or without pre-processing.

From the packaging aspect, when implants have to be inserted in small organs, with minimal invasive surgery, miniaturization obviously becomes a key requirement. As medical implants are rather complex systems including a broad variety of components (e.g. power source,

transducers, control units), special attention has to be paid to the packaging technology in order to be able to produce a compact device.

Regarding the current generation of implanted cochlear prostheses, all electronics are located close to the skin, where a transmitter coil ensures the communication with an external module, together with the power supply [1], [2]. A long bundle of wires, embedded in silicone, links the electronics to 16 to 22 passive electrodes, the stimulation electrodes, which are located inside the cochlea. One individual wire is required for each electrode. The length of this “cable” is approximately 20 cm. This is what is called the *passive scheme* in this paper (Fig. 1.a). Current manufacturing technique is based on manual assembly and is therefore relatively expensive.

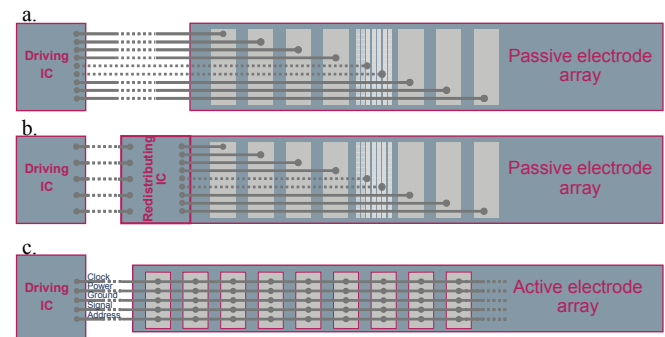


Fig. 1 Schematic representation of up to date implanted electrode array or passive electrode device (a), of active chip/passive electrodes device (*all-Silicon*) (b) and of the proposed active electrode array (c).

In recent work [4]-[6], the Department of Electrical Engineering and Computer Science from the University of Michigan has proposed a cochlear implant where they make use of an active chip to drive an array of passive electrodes. This active chip is located close to the electrode array. Using signal multiplexing, this limits the number of wires required to connect that chip to the main electronics (e.g. power supply, speech processing unit), allowing wider metal tracks and therefore lower resistivity. From this chip, gold leads are redistributing the current to the passive electrodes. This is an *all-Silicon* (Fig. 1.b) approach where the part implanted in the cochlea is made of one single piece of Si. This approach is very promising. However, being made of one Si piece, some concern can be raised regarding the reliability of the device. Due to the shape of the cochlea, an important bending of the implant is required and although the proposed device can be made very thin, it is still made of a

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brittle material. It also involves several dielectric materials whose integrity under bending may be affected. This can result in reliability and/or biocompatibility problems. In addition, the limitation of this layout is that an individual link is still required for each electrode. If a larger number of stimulation sites is desired, the small dimensions of the cochlea, with a width varying from  $\sim 1000 \mu\text{m}$  down to  $\sim 200 \mu\text{m}$ , would impose a specific redistribution design of the connections to the passive electrodes, like a multilayer redistribution scheme.

We propose to go one step further and, by reducing the size of the chips, to connect the main electronics part directly to the microelectrodes, following a concept that we call “active electrode array”. In order to improve the reliability, the whole structure is embedded in a silicone material.

The active electrode array introduced in this paper corresponds to the schematic of Fig. 1.c. Each electrode is a real chip whose backside is covered with biocompatible metal, acting as stimulation site. Using a bus architecture and multiplexer-demultiplexer IC’s, those active electrodes are interconnected via a limited number of leads. When addressed, the chip delivers some current at the selected stimulation site. One can see that, with the appropriate electronics, where the number of leads required for passive electrodes is directly proportional to the number of electrodes, the active electrodes concept requires a very limited number of lines. Basically, for stimulation, it is already possible to drive a large number of electrodes with only five lines (clock, power, ground, signal and address).

The proposed method aims at producing micro electrode arrays, using thin-film technology. This allows low dimensions, with a micrometer control, and a very high reproducibility. It should also help reducing the cost compared to current production processes.

Beside cochlear prostheses, which make use of 1D electrode arrays, another key application is retina implant, where 2D electrode arrays are required. To some extent, such 2D electrode arrays bring similar challenges than cochlear prostheses [7] and the solution presented here could fill the needs of the retina implants as well.

## II. PROCESS TECHNOLOGY

Fig. 2 details the different steps required for the CMOS transfer. Using wafer to wafer bonding, an active wafer is assembled face down to a carrier wafer. With back grinding and polishing, the active wafer is thinned down to the desired thickness. After this step, the resulting stack is aligned and bonded to another carrier wafer on which a sacrificial layer has been deposited, together with any metallization. The top wafer (first carrier wafer) is debonded and the active side of the device wafer is then exposed. After singulation at wafer level using Deep Reactive Ion Etching (DRIE), further packaging can take place using thin film technology. The individual dies can be insulated, coated,

connected and embedded.

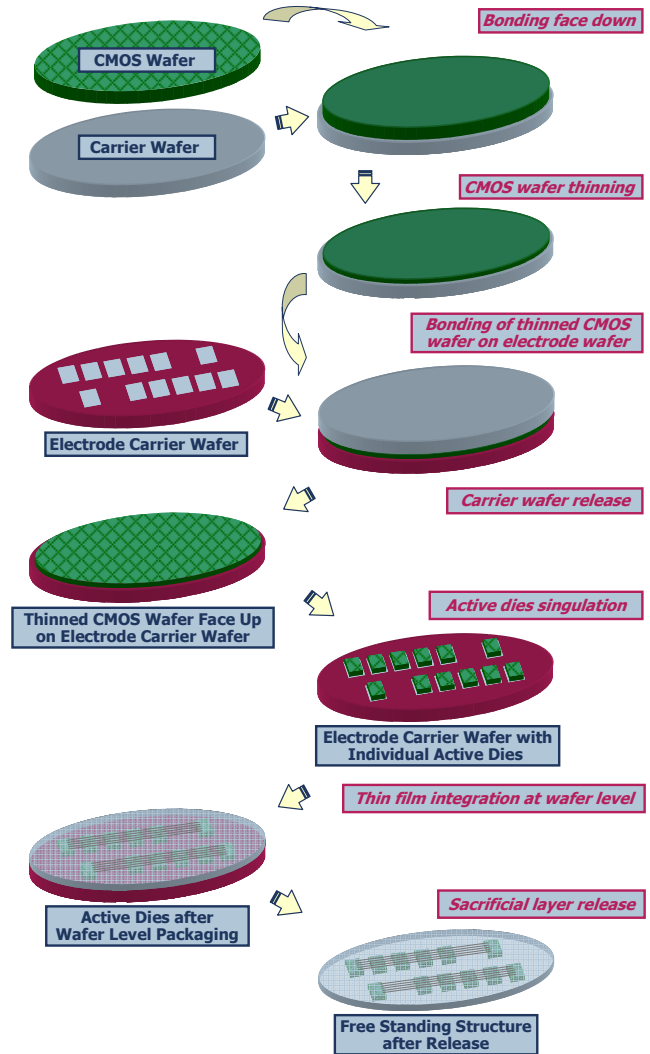


Fig. 2 Schematic presentation of the process flow.

The baseline of our process is the use of temporary carrier substrates. This results in the realization of the whole process at Wafer Level (WL), the final step being the release of the manufactured structures by removal of a sacrificial layer.

Several process steps of the above flow are based on the Ultra Thin Chip Stacking (UTCS) process [8], [9]. In addition, novel technology was developed for removal of the sacrificial layer so that individual, flexible electrodes are released. Fig. 3 shows a schematic cross section of a 1D electrodes array after the release.

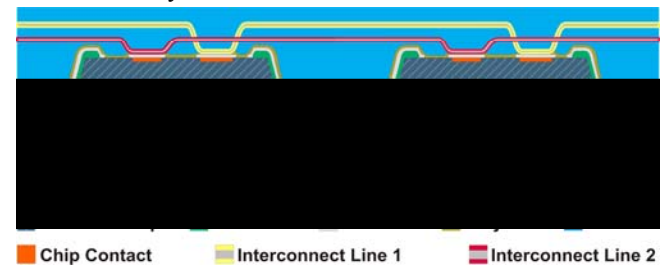


Fig. 3 Schematic representation of the active electrodes after release (cross section view).

This parallel approach (all dies are transferred at once) presents the advantage of placement accuracy and throughput (wafer to wafer bonding compared to flip chip die bonding). However, a drawback is that, for low density arrays, a significant amount of the active wafer is wasted when trimmed down to single chips (Fig. 2). Therefore, when the application doesn't require a very dense array of electrodes, a slightly modified process flow is used, based on die-to-wafer assembly. This also allows combining IC's of various types in one device. This process is however beyond the scope of this paper.

### III. RESULTS

Whereas silicone embedding is frequently used in bio medical implants, the integration of elastomeric materials in MEMS is rather uncommon. As already mentioned the use of silicone as dielectric and embedding material is proposed in our process since it combines flexibility and stretchability, which obviously improves the reliability. Indeed, any device implanted in the human body is subject to repeated deformation (body movement, heartbeat, etc.) which could cause fatigue failure of the complete device, or part of it, after some time.

Fig. 4 shows metal tracks embedded in a flexible silicone substrate. This sample has been produced using part of the proposed process flow, without integrating the thin die. This is a first step towards the manufacturing of the final demonstrator.

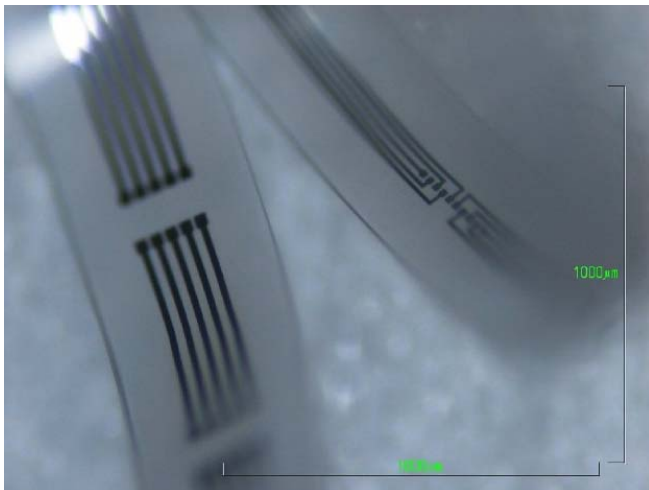


Fig. 4 Picture of metal tracks embedded in a silicone matrix.

Current devices have been realized using a photo definable silicone material, which is patterned with commercial lithography and development techniques. This silicone processing includes several baking steps which are very critical. The photosensitive properties of the silicone are based on a Pt catalytic effect, which is strongly enhanced with higher temperature. As a consequence, when the silicone film is deposited on top of a metal layer, the sensitivity can be boosted and patterning may become impossible, depending on the type of metal. One solution is

to lower the baking temperature, which is only feasible up to a certain extent, as evaporation of the solvent contained in the silicone still requires a certain heating of the film. A better solution is to switch to another underlying material. The second approach was chosen and a thin Ti layer was inserted. This one has no boosting effect on the silicone patterning and presents the advantage that it is a biocompatible material. As shown in Fig. 5, with the same baking parameters, adding a 30 nm thick Ti layer on top of a 1 μm thick Al layer makes the silicone lithography very well defined.

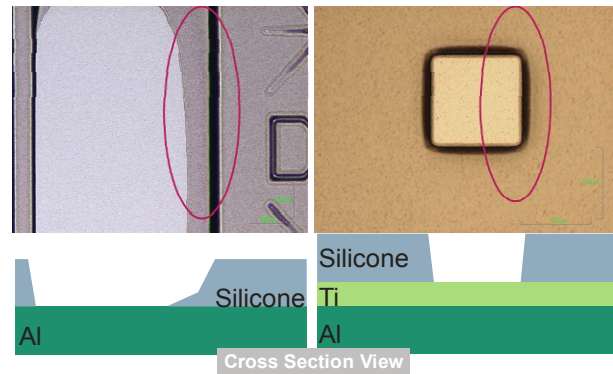


Fig. 5 Influence of the underlying metal layer on the pattern definition of the photo sensitive silicone. Poor definition and large scum when on top of Al (1 μm) (left, x20), while good definition and no visible scum when on top of Al (1 μm)/Ti (30 nm) (right, x40).

Further experiments carried out with different thickness of Ti showed that 10 nm is a minimum for the Ti to "hide" the Al from the silicone. Moreover, Ti is known as a good adhesion material and the interface with the silicone is then reinforced. Therefore, all metal layers involved in this work are actually a sandwich of the desired metal between two thin Ti layers. In addition, Ti presents the advantage that it is a biocompatible material.

As an alternative, silicone can also be used and patterned by plasma. Dry etch patterning of the silicone based on a fluorine plasma has already been demonstrated [10]. Etch rate close to 1 μm/min can be achieved.

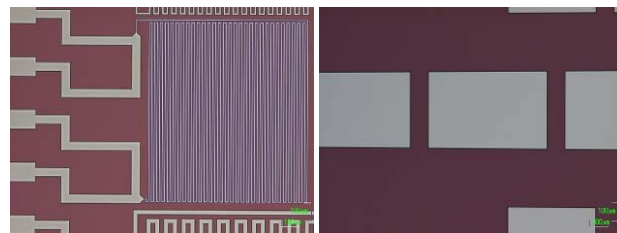


Fig. 6 Pt patterns obtained by lift-off; meanders test structures used for determination of the metal sheet resistance (left) and patterned Pt electrodes as on the electrode carrier wafer (right).

Beside the embedding/dielectric material, other materials involved in the fabrication have to be customized to the cochlear application keeping biocompatibility in mind. As metal, Pt is chosen. This material is biocompatible and



commonly used in stimulation electrodes. In the active electrode array, Pt is used as electrode surface, as capping material for the die and as metal interconnect. However, Pt is not easily etched and therefore a lift-off technique was developed. Fig. 6 presents pictures of the realized Pt patterns. A compromise was reached between a thick Pt layer, more difficult to process by lift-off, and a thin layer, whose electrical resistance would have been too high. Final selection was a layer thickness of 1  $\mu\text{m}$ , for a sheet resistance of  $\sim 170 \text{ m}\Omega/\text{square}$  (or less than 100 Ohms resistance for a 50  $\mu\text{m}$  width and 30 mm long track).

In addition to the silicone and the Pt, another frequently used biocompatible material, parylene C, is applied. It encapsulates the Pt interconnects to improve their mechanical resistance. It is also used as additional capping material for the dies. Adhesion of the metal and silicone to the parylene was increased by an  $\text{O}_2$  plasma prior to deposition.

The final release of the temporary carrier results in the free-standing flexible devices (Fig. 2.J). It requires the selection of a sacrificial layer. Key feature of this layer is that it must stand the whole process, but still be easily removable ultimately.  $\text{SiO}_2$  was considered, but standard etching takes place in vapor HF [11], [12], what is not suitable for such application. A thermally releasable sacrificial material was another option. Different types of such material exist, but none of them was offering stability during the silicone cure (250  $^\circ\text{C}$ ), together with a convenient release leaving a residue free surface. Based on work from Stephan Metz *et al* [13], we used Al as sacrificial layer. The technique is based on an enhanced anodic dissolution of the Al layer when immersed in a sodium chloride solution while a positive potential is applied to the sacrificial layer. The obvious advantage of such technique is that the release takes place at room temperature, in a neutral saline fluid, and it avoids the use of acid or any other aggressive solution.

The die singulation at wafer level is another critical step of the process (Fig. 2.H). Using standard DRIE, the generated sidewalls of the structure are vertical, which makes subsequent steps (dielectric application) complex. In order to facilitate the sidewall coverage, we optimized the DRIE process, which resulted in  $\sim 65^\circ$  sloped sidewalls (Fig. 7).

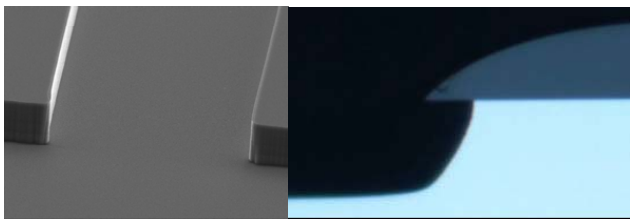


Fig. 7 Standard DRIE process (left) and optimized process to achieve sloped sidewalls (right, before photo resist mask removal)

After release, the devices can be handled individually and both mechanical and electrical measurements are possible.

Electrical measurement of a metal track embedded in the silicone carrier (as in Fig. 4) has been carried out. This measurement was performed on a flat sample. The sample has then been rolled up in order to form a 360 $^\circ$  loop and new resistance measurement has been performed. Results showed that even when completely bent, the embedded track is still conductive.

By the time of the conference, electrical characterization of the realized samples will be complete. Reliability data will be available as well, based on electrical measurement after accelerated ageing testing.

As suggested when mentioning the use of silicone, one important feature of this material is its stretchability. However, the metal wires themselves are not stretchable.

For that reason, in parallel to this work, we also investigated the possibility to make the interconnect stretchable and therefore, if and where required, to allow some stretchability to the whole device. For a cochlear implant, this would mean that it would be possible to adapt the design such that the portion of the implant comprised between two electrodes is stretchable. This is also of potential interest for the part of the implant situated between the driving IC and the electrodes..

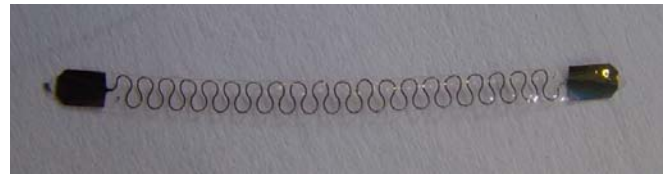


Fig. 8 Picture of stretchable interconnection, achieved by appropriate design of the metal path.

The outcome of this work is that stretchability may be achieved by adapting the path of the metal interconnect, designing it in a meander shape rather than a straight shape. Fig. 8 illustrates a “horse-shoe” shaped interconnection embedded in a silicone carrier.

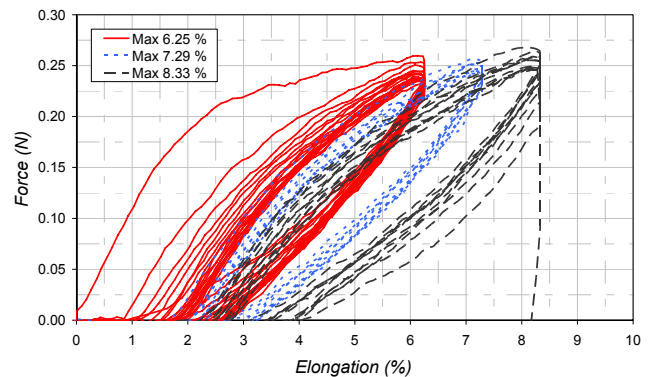


Fig. 9 Force – deformation curve of a metal track embedded in a silicone carrier.

Fig. 9 presents the force-deformation curve of such a structure submitted to repeated deformation. This is for a 24 mm long structure in silicone, 35  $\mu\text{m}$  thick, with embedded metal tracks as shown on Fig. 7. The tensile test

was set up to stop the elongation at a fixed deformation and bring the sample back to its original length, still recording the force. The first series of tests was done up to 6.25 % elongation.

The first curve on Fig. 9 corresponds to the plastic deformation of the structure. After that, for the subsequent deformation cycles, an elastic hysteresis is observed. This elongation to 6.25 % is repeated 20 times. The system is then set to extend the sample of 7.29 % of its original length. The cycle is repeated 10 times and, again, an elastic hysteresis is observed. Finally, the deformation cycle is extended to 8.33% and, after ten additional cycles, the sample broke. This shows that the silicone structures realized with thin film can be made stretchable, even with a thickness of  $\sim 35 \mu\text{m}$ . To some extent, repeated deformation can be applied without break of the silicone. Simple electrical resistance measurements realized after stretching experiments showed that the embedded metal track was still conductive. Further work will be done to improve the stretchability to higher deformation and to investigate the conductivity during deformation.

#### IV. CONCLUSION

Cochlear prosthesis is a driving application for the development of electro stimulating medical implants. As a larger number and a higher density of electrodes are desired, current technology needs to be improved and alternative concepts are required. We developed a concept based on the embedding of active chips in a silicone carrier to form a new generation of electrode arrays. This novel technology uses biocompatible materials, as Pt and parylene C, to seal the active chip. The whole electrode array is embedded in silicone. Stretchability of the silicone, coupled with an appropriate design of the metal interconnects at sensitive locations, should allow improved reliability of the device.

#### ACKNOWLEDGMENT

Several results presented in this work were supported by the European Community in the frame of the Healthy Aims Project IST-2002-1-001837 and the Institute for the Promotion of Innovation by Science and Technology in Flanders (IWT-Vlaanderen) in the frame of the Bioflex project (IWT-040101).

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