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A Wireless Power Interface for Rechargeable Battery Operated Neural Recording Implants

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***Abstract*—This paper describes an integrated analog front-end for wireless powering and recharging of miniature Li-ion batteries used in implantable neural recording microsystems. DC signal extraction from a wireless carrier is accomplished using Schottky barrier contact diodes with lower forward voltage drop for improved efficiency. The battery charger employs a new control loop that relaxes comparator resolution requirements, provides simultaneous operation of constant-current and constant-voltage loops, and eliminates the external current sense resistor from the charging path. The accuracy of the end-of-charge detection is primarily determined by the voltage drop across matched resistors and current-sources and the offset voltage of the sense comparator. Experimental results in 0.6µm bulk CMOS technology indicate that ±1.3% (or ±20µA) end-of-charge accuracy can be obtained under worst-case conditions for a comparator offset voltage of ±5mV. The circuits occupy 1.735mm^2 with a power dissipation of 8.4mW when delivering a load current of 1.5mA at 4.1V (or 6.15mW) for an efficiency of 73%.**

I. INTRODUCTION

Low power wireless interfaces for implantable neural recording devices are essential for data acquisition and long-term bio-compatibility studies in behaving animals as the use of tethered percutaneous connectors increases the risks of skin irritation and infections [1]-[3]. Powering of these devices is accomplished using a common framework consisting of an external backpack, an inductive link and the implant microsystem [1]. Owing to the size constraints of the implant site, weak coupling of inductive links and radiation limits, the backpack or external powering device is placed in very close proximity (<10mm) to the implant, often attached directly to the animal. The direct attachment of potentially bulky backpacks during neural recording sessions, especially when involving small animals such as rodents, may result in increased acclamation time for the animal, possible damage to the external hardware, while creating inconveniences to the researchers during electrophysiology experimentation (i.e. limiting the type of experiments involved due to the mechanical interface).

In this work, we depart from the traditional backpack based approach and remove the external components attached to the animal during neural recording sessions. This initial definition of the mechanical interface suggests that powering of any implant microsystems must be accomplished via a biocompatible rechargeable battery. As battery technology continues to advance toward higher volumetric densities, faster charge cycles and even potential integration with solid state devices, the demand for a low power electronic interface capable of supporting a rechargeable battery implant framework is likely to increase. While battery recharging is still accomplished using an external backpack, the animal is void of any external components during neural recording sessions, thus simplifying the mechanical interfaces during experimentation. The key benefit that it offers over traditional neural implants in behaving animals is increased flexibility – the device can be operated with or without an external module strapped to the animal. Moreover, operating the devices in two phases eliminates the interference on the telemetry link due to a strong power carrier.

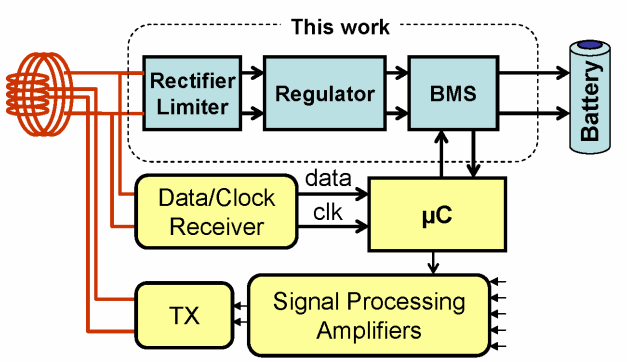


Fig.1. Rechargeable battery powered electronic implant system block diagram.

As shown in **Fig. 1**, this paper focuses on a low power analog front-end wireless power interface with battery management system (BMS) for an implantable multi-channel neural recording brain-machine interface device. Circuit implementation details of the schottky diode based rectifier, regulator and battery control loop are presented in section II. Measurement results and concluding remarks are provided in sections III and IV, respectively.

II. CIRCUIT DESCRIPTION

Fig.1 shows a block diagram of the battery powered wirelessly rechargeable implant system. During the recharging phase, an externally supplied 4MHz wireless power carrier is rectified and regulated to generate a stable supply voltage. This supply powers the control loops used to provide the appropriate current/voltage profiles for sensing and charging the battery. The TX/RX antennas and the battery are the only external modules of the electronic chip.

A. Schottky barrier diode rectifier

Front-end rectification circuits for biomedical implants are often implemented using diode connected devices or p-n junctions [2]. However, schottky barrier diodes offer higher

operating frequencies and lower forward voltage drop compared to standard p-n junction based diodes [4]. By selectively blocking the n+/p+ implants in desired diffusion areas, Ti-Si schottky barrier diodes are fabricated in standard 0.6µm CMOS process. A cross-section and layout of a schottky contact diode is shown in **Fig. 2a**. The barrier height of the schottky contact is primarily determined by foundry process parameters (i.e. Ti-Si contacts and doping concentrations) and the parasitic series resistances. The cut-off frequency of the schottky contact is determined by the zero bias junction capacitance (C_{JO}) and the total resistance determined by the n-well (R_D and R_W) and ohmic contact (R_C) parasitic resistances. To maximize the cutoff frequency, it is desirable to use a small schottky contact area [5]. The current handling capability is improved by placing multiple schottky diodes in parallel. The reliability characteristics of all schottky diodes are improved by fabricating the schottky contacts with a self aligned p+ guard ring to extend the breakdown voltages. Without the guard ring, the breakdown voltage can be as low as 4-5V [6].

The schottky contacts are used to implement a full-wave rectifier, as shown in **Fig. 2b**. Simple observation shows that the parasitic n-well/p-sub diodes are either reversed biased or appear in parallel with the schottky contacts. Since the schottky forward voltage drop is smaller than the parasitic diodes, the rectifier exhibits a smaller turn-on voltage for improved efficiency. Moreover, the full-wave rectifier topology delivers twice the current per cycle compared to a half-wave rectification circuit. The minimum voltage across the input LC tank is one schottky forward voltage drop below the ground potential of the chip. The maximum operating voltage of the rectifier is determined by the parasitic n-well/p-sub reversed biased breakdown voltage, which is sufficiently large to withstand the 5V coupled voltage at the antenna terminals [7].

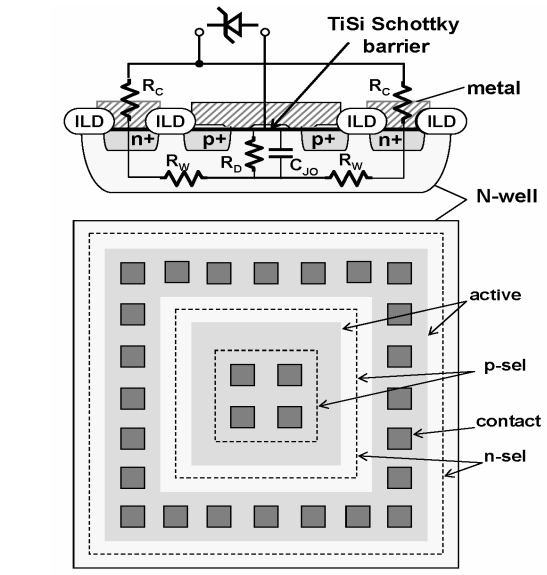


Fig. 2. (a) Cross-section and layout of a Schottky barrier diode and (b) front-end interface with full-wave rectifier, RF limiter and supply voltage regulator.

B. Front-end regulation

Following a 4MHz LC resonant tank and the full-wave rectifier, the voltage across a 2.2nF on-chip storage capacitor (C_S) is regulated to provide a stable supply voltage for the implant electronics. Over-voltage protection is accomplished using an RF limiting circuit, which is a standard modification to silicon-controlled rectifier circuits commonly used in electrostatic discharge (ESD) topologies [8]. The limiter operates by shunting the current to reduce the effective loaded quality factor of the chip when the rectified voltage exceeds a target voltage, which is determined by the voltage drop across a cascade of diode connected nMOS devices (**Fig 2b**). DC voltage generation for the implant electronics is accomplished via the negative feedback of the operational amplifier. A pMOS pass device topology, as opposed to an nMOS device, is used to achieve low dropout voltage without having to generate an overdrive voltage that exceeds the induced rectified voltage – this pMOS topology, however, exhibits lower bandwidth. The voltage (V_B) is generated from the battery using a supply independent reference circuit [9].

C. Battery control loop

The typical charging profile for Li-ion batteries, determined mainly by its chemistry and composition, is shown in **Fig. 3a**. The battery is first charged at a constant current (CC) rate to its upper threshold of 4.1V, followed by a constant voltage (CV) until the charging current drops to about 4% of the initial applied CC rate [10]. As shown in **Fig. 3b**, a high precision external sensing resistor (R_{SENSE}) is inserted in the battery charging path for accurate current measurement and end-of-charge (EOC) detection. A low value is typically chosen to maintain the maximum voltage drop across R_{SENSE} to within 100mV so as not to affect the charging profile and minimize the power dissipation – this is particularly important when the dynamic range of the battery current is large. This requires a high resolution (V_{RES}) comparator with low input referred offset (<<1mV), which is difficult to implement in an implant environment with non-ideal ground/supply voltages. Chopping techniques and high-order sigma delta A/D converter can be used to improve detection accuracy at the expense of increased implementation complexity [11].

In the proposed control loop, the external resistor R_{SENSE} is removed altogether and replaced with two integrated matched resistors that provide increased voltage sensing margin for end-of-charge detection. This relaxes the resolution requirements of the comparator and provides the additional benefit of decreasing the overall footprint of the implant unit. In addition, this approach permits the simultaneous operation of both constant-current and constant-voltage loops without disrupting or destabilizing the charge process.

The circuit implementation of the battery control loop is illustrated in **Fig. 3c**. The bias circuit (N1-N4 and P5) gener-

ates a reference current I=260nA for the current source legs I_A=98I (N5-N6) and I_B=48I (P4). When the battery cell is fully discharged (V_{BAT}~2.7V), the voltage sense amplifier (A1) drives P3 into cutoff. The full current difference I_A-I_B is reflected via the current-mirror (P1-P2) to provide the battery cell with a constant current of approximately 1.5mA (i.e. 50·260nA·114~1.5mA) - this is equivalent to 0.5C charge rate for a 3mAh battery [12]. As the battery charges, the cell voltage increases from 2.7V to V_{REF}~4V, driving P3 into conduction via the negative feedback of amplifier A1. The current difference I_A-I_B is progressively steered into the P3 leg, decreasing the available output current for charging the battery. The end-of-charge (EOC) signal is generated by comparing the voltage difference (V_B-V_A) between resistor R_A and R_B. By setting R_A=R_B, the EOC trigger voltage occurs when a current of 48xI from IA is steered into the P3 leg. The ratio of the cutoff current to the initial charge current can be easily derived as:

$$\eta = \frac{I_{cutoff}}{I_{initial}} = \frac{I_A - 2I_B}{I_A - I_B} \quad (1)$$

For I_A=98xI and I_B=48xI, the ratio of the cutoff current to initial charge current is ideally independent of the reference current I and is given by η= 2xI/50xI= 4%. The accuracy of end-of-charge detection is thus primarily determined by the offset voltage of the sense comparator and the matching accuracy of resistors and current sources instead of the absolute value of a single sensing resistor. With proper layout, mismatch less than 2% can be easily attained across process variations. Moreover, since the proposed topology does not require sense resistors in the battery charging path, these can be made much larger to generate an easily detectable voltage difference, relaxing the offset and resolution requirements of comparator A2 and thus facilitating EOC detection.

III. EXPERIMENTS

A. Packaging platform

A custom package platform was developed to test the proposed circuits. As shown in **Fig. 4**, a chip-on-board (COB) technique is used to attach the fabricated CMOS die onto a standard circular printed circuit board (PCB). In addition to serving as a platform for the die, the 9mm diameter circular 16mil thick PCB serves as a fixture for the secondary inductor. Standard 3/44 AWG litz wire is used to wind a 48µH coil around a miniature ferrite core attached to the PCB substrate. The ferrite core lowers the required number of turns by 20% to yield a higher measured Q of 38 at 4MHz. Notice that since the die is directly above the inductor, the measurements also include the effect of induced fields and potential noise pickup from the coil – this leads to a more realistic test environment for the targeted space limited implant.

B. Measurement results

A prototype chip was fabricated in standard 0.6µm 3-metal 2-poly 5V Bulk CMOS technology in order to validate circuit functionality. The circuits are powered using a close proximity inductive link developed using standard design procedure [13], and consists of primary coil with 75µH of inductance and an outer diameter of 9mm. **Fig. 5a** shows the transient regulator response when an externally generated 0

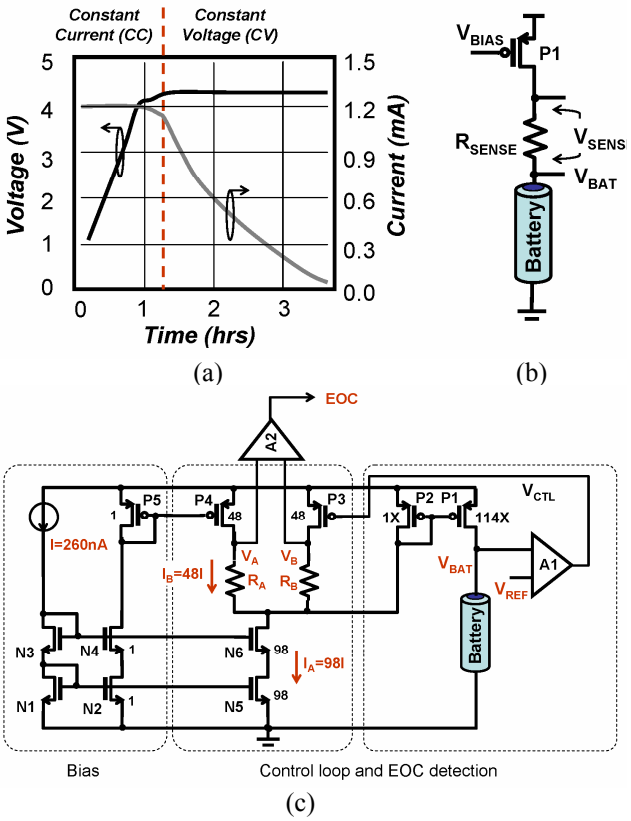
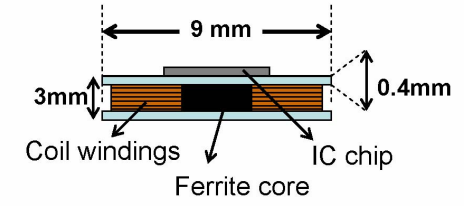


Fig. 3. Li-ion battery charging: (a) typical charge and discharge profiles, (b) basic charge sensing topology and (c) proposed control loop.



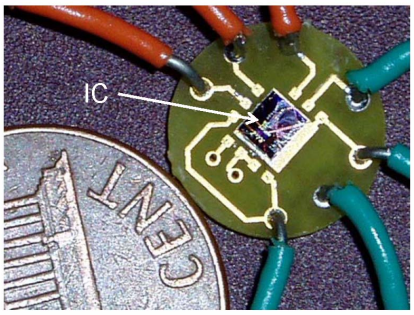


Fig. 4. IC chip-on-board packaging with test pins and coil antenna wound around a ferrite core.

to 2mA load step is applied as the link is powered by the primary coil voltage. The measured response is within 15% (or 600mV/4.1V) of the target 4.1V supply. The regulator exhibits a load regulation of 2mV/mA (or 240ppm/1mA), a line regulation 2mV/V and a low dropout voltage of 50mV. At 4MHz, the worst-case measured peak-to-peak ripple voltage at the output is within 100mV. The RF limiter draws 0.5µA when the rectified voltage is Vi=4.2V and 14mA for

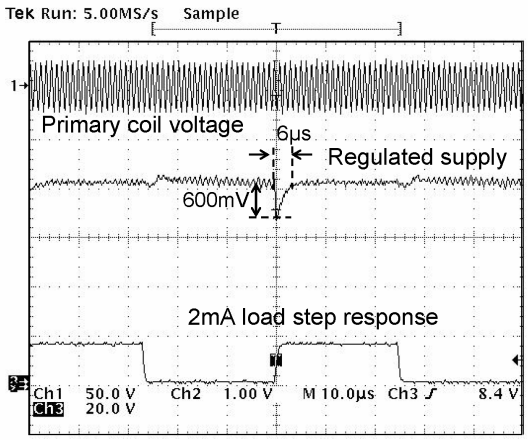
Vi=5V, which is sufficiently large to de-Q the input resonant LC tank. The quiescent current of the front-end circuitry is 22.5µA when Vi=4.2V (or power dissipation ~95µW).

Charging profile experiments for the battery control loop were performed with a large storage capacitor (instead of a battery) to decrease the charge time and illustrate the dynamic voltage and current waveforms. The voltage difference across an external 200Ω sense resistor was measured to determine the charge current, as shown in **Fig. 5b**. During the constant-current phase, the circuit delivers 1.5mA via P1 resulting in a linear increase in battery voltage (V_{BAT}). The EOC during the constant-voltage phase is detected once the battery current reaches 5% of the nominal constant charging current of 1.5mA, triggering the EOC signal at output of comparator A2. The design target was intentionally set higher at 5% (or 75µA) to ensure that an EOC signal is generated under nominal conditions despite mismatch variations. Digital trimming is employed in the comparator and current mirror to measure the effect of device mismatch. Measurements show that a 1.5% mismatch in P4-P5 current mirror results in a 3% increase of EOC (or 45µA) and that ±5mV comparator offset causes a ±1.3% (or ±20µA) increase in EOC.

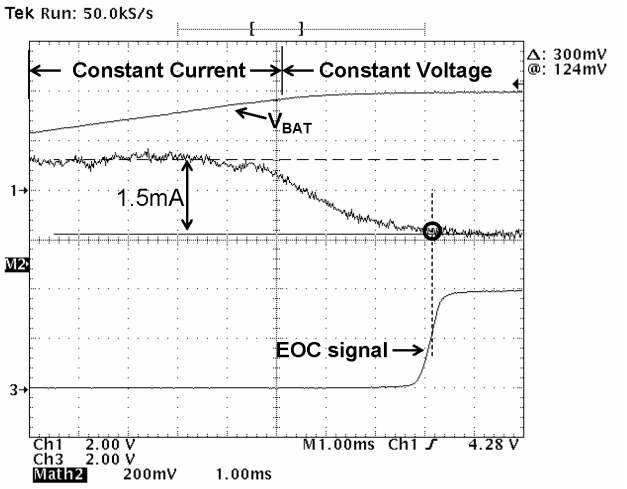
The measured power dissipation of the battery control loop is 160µW, with an efficiency that ranges from 66% to 95%, depending on the charging phase. The total measured loaded power dissipation of the chip is 8.4mW when delivering 1.5mA at 4.1V to the load (or 6.15mW) for an efficiency of 73% - this includes secondary coil loss, rectifier, RF limiter, regulator and battery control loop. The overall area of the front-end circuits and control loop is 0.3mm^2, while the 2.2nF charge storage capacitor occupies an additional 920µm by 1560µm (or 1.435mm^2).

IV. CONCLUSIONS

Low power integrated circuits for an implantable microsystem with wireless power link and rechargeable battery control loop are presented. The front-end electronics employ a schottky barrier diode rectifier to achieve low turn-on voltage and an RF limiting and regulation circuit that attains 2mV/mA and 2mV/V of load and line regulation, respectively. The proposed battery charger uses integrated current sense resistors with an end-of-charge detection accuracy that is primarily determined by the matching accuracy of current sources and comparator offset. The accuracy of the state-of-charge estimation after digital trimming of the current-mirror leg is within ±1.3% for a comparator offset of ±5mV. The circuits occupy 1.735mm^2 with a power dissipation of 8.4mW when delivering a load current of 1.5mA at 4.1V (or 6.15mW) for an efficiency of 73%.



(a)



(b)

Fig. 5. Measured results (a) load response of regulated supply and (b) battery control loop charging.

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