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Design and Evaluation of a 2D Array PIN Photodiode Bump Bonded to Readout IC for the Low Energy X-ray Detector

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***Abstract*— A 2D array radiation sensor, consisting of an array of PIN Photodiodes bump bonded to readout integrated circuit (IC), has been developed for operation with low energy X-rays. The PIN photodiode array and readout IC for this system have been fabricated. The main performance measurements are the following: a few pA-scale leakage current, 350pF junction capacitance, 30㎛-depth depletion layer and a 250㎛ intrinsic layer at zero bias.**

This PIN photodiode array and readout IC were fabricated using a PIN photodiode process and standard 0.35㎛ CMOS technology, respectively. The readout circuit is operated from a 3.3V single power supply.

Finally, a 2D array radiation sensor has been developed using bump bonding between the PIN photodiode and the readout electronics.

I. Introduction

THIS paper reports on a study of digital X-ray imaging for general radiography. The study is based on an X-ray imager that uses a 2D array PIN photodiode with bump bonding to a CSA (Charge Sensitive Amplifier) with an ASIC (Application Specific Integrated Circuit) for low energy detection.

2-D digital radiation sensors such as the CZT, CdTe and a-Se have disadvantages that include difficulty of viewing a large field, high cost, and the requirement for high voltage as compared to indirect radiation type sensors. These disadvantages are in spite of a direct type detector and 100% fill factor. Additional problems are the sensor's sensitivity to temperature and flat panel distortion. The CCD is difficult to view in a large field and has high cost. Moreover, for the CCD system, front-end electronics are needed for the design of each individual system. The CMOS sensor is a low cost and monolithic system with a low SNR (signal to noise ratio), because it is a PN junction photodiode. It also has the problem of difficult viewing in a large field.

Therefore, we developed a new radiation sensor, a 2D array PIN photodiodes bump bonded to readout electronics. It has a higher SNR than the CMOS sensor because of an attached intrinsic depletion layer. Moreover, it can adequately accommodate large areas, and sensor thickness because of the use of a Si-wafer from the PIN photodiode process.

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II. Materials and Methods

A. Front side and Back side Illumination of the PIN Photodiode

The 2D array PIN photodiode, we suggested, has been developed with bump bonding between the PIN photodiode and readout integrated circuit (IC). This device can have front side illumination and back side illumination according to the incident direction of photon.

The advantage of a front side illumination photodiode is that it can use an existing photodiode process. It does not need reverse bias voltage because most of light from the scintillator can be absorbed on the surface of the silicon wafer as shown in Fig. 1(a). Therefore, the frond side illumination method can reduce noise created by high voltage. However, because of metal line for the cathode, placed on the frond side of photodiode, the fillfactor is reduced.

The advantages of a back side illumination photodiode are that it can have a one-hundred percent fill factor and quantum efficiency as shown in Fig. 1(b). However, light from the scintillator, incident from the back side, requires a high reverse bias voltage to ensure thick depletion layer of photodiode. Therefore, the leakage current is increased by this high voltage [1].

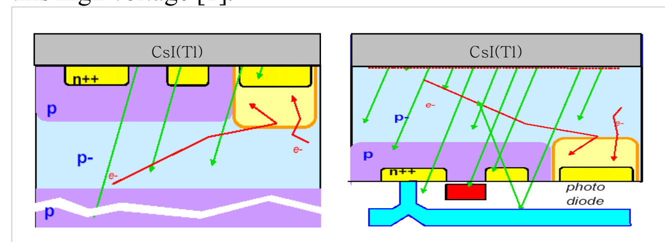

Fig. 1. (a), (b) Illumination in front and back side

B. Design of PIN Photodiode

A PIN photodiode has been used in a solid-state detector for X-ray detection as a photosensor of visible light from the detector's scintillator. Generally, as the light from the scintillator is of short wavelength, having a peak at 450~650nm, the light is absorbed within a very shallow layer near the surface of the photodiode before arriving at the depletion layer. It does not contribute to the signal. In this PIN photodiode design, it is important to make the p-layer as shallow as possible [2][3]. In order to achieve a shallow junction, the optimum conditions of ion implantation, such as the thickness of the SiO_2 oxide barrier, the tilting angle of the wafer with respect to the incident ion beam, and the annealing conditions, have been determined by using the results of

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simulation. In this work, we used the device simulation tool, ATHENA, from the SILVACO Company. This tool provides general capabilities for numerical, physically-based, two-dimensional simulation of semiconductor processing.

Information for wafer characteristics is shown in Table 1. Moreover, the doping concentration and thickness for PIN photodiode processing is shown in Table 2. A n-type silicon wafer with <100> orientation has been chosen as the base material of the PIN photodiode because the penetration depth of boron in <100> is shallower than in <111> material [4]. Due to the light weight of B+, the B+ has a long projected range and a lower ionization rate. This leads to an increase in the PN-junction depth. BF2 (49BF+2) ion implantation was employed in this study because the projected range of BF2 was about 25% of boron and BF2 had a higher ionization rate [5]. However, the BF2 implantation induces some undesirable effects, such as damaging and deforming the crystalline lattice which give rise to an amorphous Si layer on the surface of the Si crystal. This may cause recombination of carriers and eventually adversely affect the diode's performance, such as increasing of the leakage current and decreasing photosensitivity. This amorphous Si layer can be recrystallized and cured by a subsequent annealing process. Process parameters for ion implantation, obtained by simulation, are given in Table 3. Moreover, the detail structures and dimensions of the PIN photodiode are described in Table 4. Results of the depletion region, junction capacitance, dark current, and the wavelength of the PIN photodiode with p+ guard rings and n+ guard rings are shown in Fig. 2, 3, 4, and 5, respectively. Because p+ guard rings have the same potential as the p-layer of photosensor, it has the advantage of reduction of dark current. The n+ guard rings are superior to the p+ guard rings from the viewpoint of wavelength.

Table 1. Wafer characteristics

Size & Type	Dia : 5", n-type
Orientation	<100>
Thickness & Resistivity	380um, 5kΩ-cm

Table 2. Doping concentration and thickness for PIN photodiode processing

	N+	Intrinsic	P+(active)
Doping concentration	2×E15	6.16×E11	1×E15
Thickness	1.5um	5000 Å~1.5um	5000 Å

Table 3. Fabrication parameters for ion implantation

Parameters	Value
Ion beam type & Energy	BF2, 40keV
Thickness of oxide barrier layer	200_
Tilting angle	7
Annealing condition	750_900_ , 30min

Table 4. Sensor structure and dimensions for designed PIN photodiodes

Type	Indirect Method
Sensor division	2-D area sensor
Pixel size	48um×48um
AR Coating	Si_3N_4
Guard ring	P+ triple layers

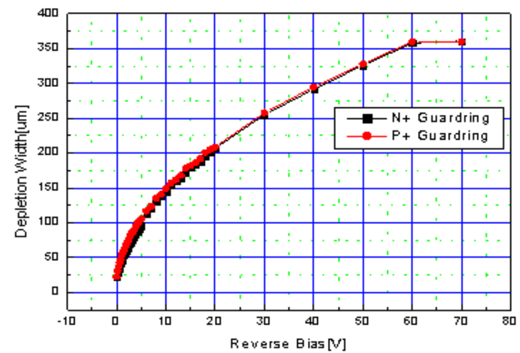


Fig. 2. Depletion width versus reverse bias voltage at indirect sensor.

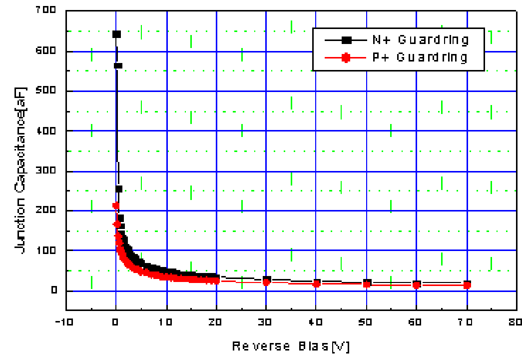


Fig. 3. Junction capacitance versus reverse bias voltage at indirect sensor.

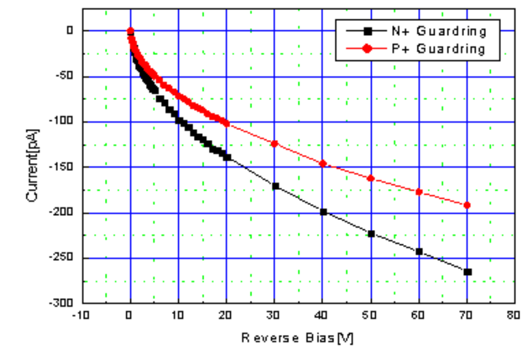


Fig. 4. Cathode current versus reverse bias voltage at indirect sensor.

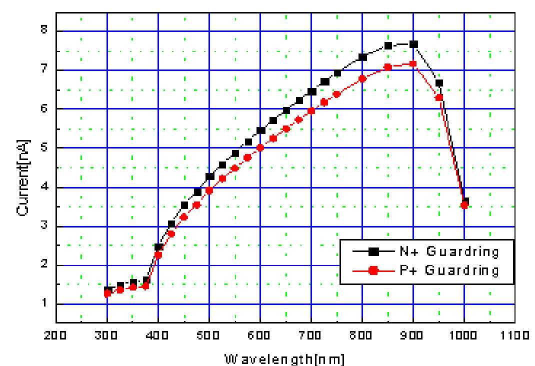


Fig. 5. Anode current versus wavelength at indirect sensor.

C. Design of the Scintillator

A scintillator needs suitable thickness to absorb fully incident radiation. Therefore, we presupposed, before

building the scintillator, the maximum thickness of the scintillator for incident radiation energy using MCNP simulation code. The incident radiation spectrum is shown in Fig. 6. On the assumption that this X-ray was incident on the CsI(Tl) scintillator, having a 48㎛×48㎛ pixel structure, energy deposition is acquired as shown in Fig. 7. In this Fig., the saturation thickness of the scintillator is about 300㎛. The maximum absorption energy is about 6.5MeV at this time.

Scintillator materials such as CsI(Tl) are coated directly on the 2-D array sensor with the above thickness by using physical vapor deposition (PVD) or E-beam Evaporation (EBE) processing.

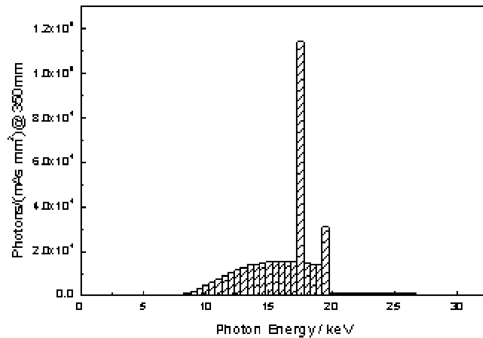


Fig. 6. X-ray spectrum generated by simulation of SRS-78 code for 28 kVp of mammography condition.

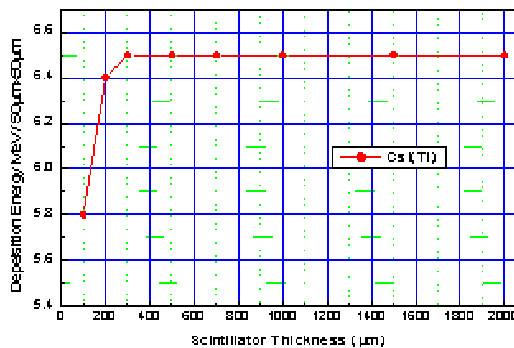


Fig. 7. Deposition energy for CsI(Tl) scintillator at mammography condition.

III. Experimental Results

A. Design of the Readout IC

A 2D array integrated readout circuit and a charge sensitive preamplifier (CSA) have been developed to bump bond to a X-ray detector module that uses 2D array of PIN photodiodes. The CSA has been designed with a traditional scheme as shown in Fig. 8. It consists of a low noise integrator and low impedance output buffer. Both preamplifier and output buffer are based on a single ended folded cascade structure. This solution offers better performances in terms of stability and gain compared with that of a standard cascade [6][7].

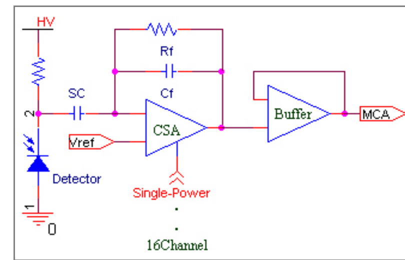


Fig. 8. Schematic diagram of core amplifier

The main performance measurements of the CSA are the following. The input equivalent noise charge is 300 e^- rms at a peaking time of 200ns. The highest gain is 10mV/fC. The peaking time is adjustable between 50ns and 300us by external passive components. The noise simulation yields ENC values of 50e^- and 250e^- for thermal and 1/f noise, respectively. This design has been fabricated in standard 0.35㎛ CMOS technology. The circuit occupies an area of 4×4mm^2 and dissipates 2mW per channel from a 3.3V single power supply.

Some performance characteristics for the 16 channel IC are summarized in Table 5.

Table 5. Some performance characteristics for CSA.

Amplifier Simulation Result Fab - MPW(Hynix 0.35um 2P 4M)			
Gain	10mV/fC	Noise	455uVrms
Output Swing	2.8V	GBW	200MHz
Input Range	10MIP	Peaking Time	200ns
Output Range	1V	Ch - Ch gain variation	~ 2% s.d.
Linearity	0.3% to 50fC Qin	Power Consumption	2mW per channel

We have tested the peak output voltage of the CSA, with leakage current of the radiation detector due to manufacturing uncertainty. It has been verified using four sets of parameters(typical and three corners) from the Hynix 0.35㎛ 2P 4M process. In Fig. 9 the output voltage of the CSA versus four sets of manufacturing parameters from the process is reported. Operating temperature from 0 to 100 with an input charge of 50fC has been applied. Channel to channel variations have been observed. The maximum non-linearity seen in Fig. 9 is less than 0.3% over the entire input charge range at 3us peaking time.

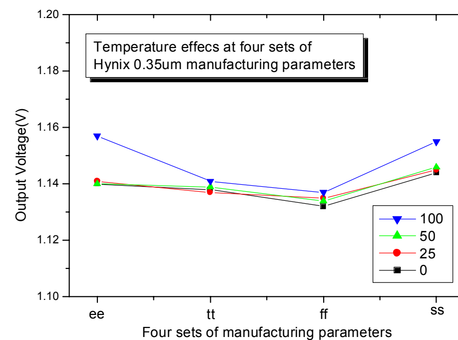


Fig. 9. Temperature effects at four sets of manufacturing parameters

B. Bump Bonding to a PIN Photodiode-Readout IC

A 2D array radiation sensor has been developed using bump bonding between a PIN photodiode and readout electronics. Solder bumps are small spheres of solder (solder balls) that are bonded to contact areas or pads of semiconductor devices and that are subsequently used for face-down bonding. The length of the electrical connections between the chip and the substrate can be minimized by (a) placing solder bumps on the die, (b) flipping the die over, (c) aligning the solder bumps with the contact pads on the substrate, and (d) re-flowing the solder balls in a furnace to establish the bonding between the die and the substrate, as shown in Fig. 10.

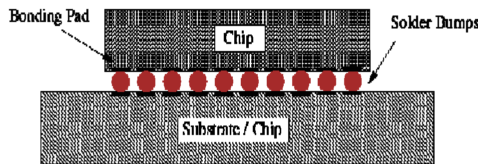


Fig. 10. The flip-chip method of interconnection where solder bumps are used to interconnect a chip to a substrate or sometimes to another chip.

C. System Measurement

We fabricated the PIN silicon photodiode on an n-type silicon substrate with high resistivity of 5,000 - 10,000 Ωcm, intrinsic, and a total layer thickness of 30㎛ and 250㎛, respectively. To assess the performance of the photodiode, the leakage current was measured. Mainly the dark current and its variation were measured by using a probe station and semiconductor parameter analyzer-HP4145A. At zero bias where the system is operated, the leakage currents were nearly identical for all photodiodes, but there was an increase with reverse bias as shown in fig. 11. Fig. 12 shows the fabricated PIN silicon photodiode, CSA -ASIC chip. Fig. 12(c) shows the output voltage pulse recorded on a digital oscilloscope, for a charge injection with PIN photodiode for the X-ray step pulse having tube voltage 100kVp, tube current 20mA, and X-ray pulse time 8.3ms.

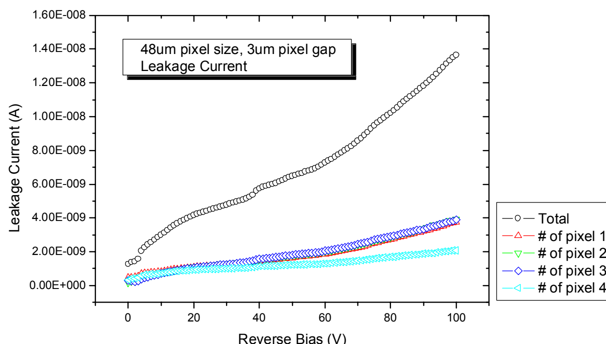
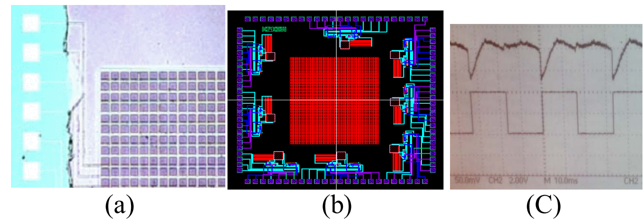


Fig. 11 Leakage current of the 2D PIN photodiode with 3㎛ pixel gap.



(a) (b) (C)

Fig. 12 (a) Fabricated the 2D array PIN photodiode, (b)2D readout CSA chip and (c) Output voltage of readout CSA bumped to PIN photodiode for X-ray step pulse.

IV. Conclusion

In this study, we suggested a new structure for a 2D array PIN photodiode with bump bonding to readout electronics to increase this system's SNR and fill factor. We described a method to design a sensor using this system.

Commercially available combinations of a scintillator and sensor such as a CMOS, CCD, do not have a good fill factor and do not have high SNR due to using a general PN diode and front side illumination. Therefore, we expect that the large depletion width of the PIN photodiode, bump bonded to readout electronics, is one solution for a low energy detector that has good resolution and high SNR.

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