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FPGA-based Sleep Apnea Screening Device for Home Monitoring

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Abstract — **We present the hardware design of an FPGA-based portable device for home screening of sleep apnea syndromes. The device is simple to use, inexpensive, and uses only three signals, namely the nasal air flow and the thorax and abdomen effort signals. The device hardware stores data of overnight sleep on a Secure Digital card. At the clinic, the sleep specialist reads in the stored data and uses an algorithm for the detection and classification of sleep apnea. The device is fairly low-cost and may help spread the ability to diagnose more cases of sleep apnea. Most sleep apnea cases currently go un-diagnosed because of cost and practicality limitations of overnight polysomnography at sleep labs.**

Keywords— **Sleep apnea, screening system, portable devices, home monitoring, FPGA, SD Card.**

I. Introduction

Sleep apnea (SA) is a disorder, in which a person stops breathing during the night, perhaps hundreds of times, usually for periods of 10 seconds or longer and sometimes for as long as a minute [1]. It was shown in [2] that the prevalence of undiagnosed SA is high among the population and is associated with hyper-somnolence.

Overnight polysomnography (PSG) permits an accurate diagnosis of SA [3]. However, it is expensive, inconvenient, time-consuming, and labor intensive. We have previously reported a system suitable for detection and classification of SA using only three breathing signals: nasal airflow, thorax movement, and abdomen movement [6]. We have also presented a comparative study between Alice®4 Sleep Diagnostic System (Respironics, Inc., Pittsburgh, PA, USA) and our fuzzy logic based system for automatic detection and classification. The proposed system was shown to outperform Alice®4 [7]. The encouraging results of the system and the potential low cost of its implementation lead to a complementary approach for designing a screening device for at-home screening.

In this paper, we will describe a design for a screening device to be used at home. The main objective is to determine whether the suspected patient should go through a full PSG evaluation. It will also determine which type of SA he or she is suspected for. In the proposed usage model, the sleep physician trains the patient on how to use the device and connect the sensors. The patient installs the device to record the sleep information at home. The device stores data of nasal airflow, thorax, and abdomen movement on a SecureDigital (SD) memory card. The patient then returns to the physician and the SD card is read via a USB reader. The developed algorithm [6,7] is used to automatically classify the whole sleep period.

The designed hardware is FPGA-based and battery-powered. It features a small size, simple operation and SD card as a storage medium. The proposed screening device is described in section II. Discussion is presented in section III. Conclusions and directions for future research are placed under section IV.

II. Screening Device Description

Figure 1 shows a detailed block diagram of the developed system. It illustrates the use of the FPGA in addition to the interfaces to the outside world. The device is battery-powered, which reflects on the choice of analog and digital components as will be shown shortly. The controls and description of each block is discussed in the following subsections.

A. Sensors

Recording of respiratory airflow is performed using a thermistor sensor. This sensor is based on measuring relative temperature during expiration and inspiration and on the heat content of the air (temperature and volume) passing over the sensor [8]. We have chosen a Sleepmate® sensor - item#1450 (Sleepmate, Inc., USA), which has an output range of +/- 100 μVolts.

The respiratory efforts (thorax and abdomen movements) are measured using piezo-electric sensors, which have the ability to produce small voltages when stress is applied. On each breath, the sensors are stressed by the expansion of the thorax or abdomen. We have chosen two Sleepmate® sensors - item#1301, which have an output range of 1 to 3 mV.

B. Analog Processing

The voltage produced from the sensors is amplified and conditioned to produce clean, reliable respiratory signals. For this purpose 3 instrumentation amplifiers (INAMP) were used, followed by band-pass filters (1 set for each respiratory signal). To meet our specifications, we have chosen the Texas Instruments (TI) INA326 as a high-performance, single-supply, precision INAMPs with rail-to-

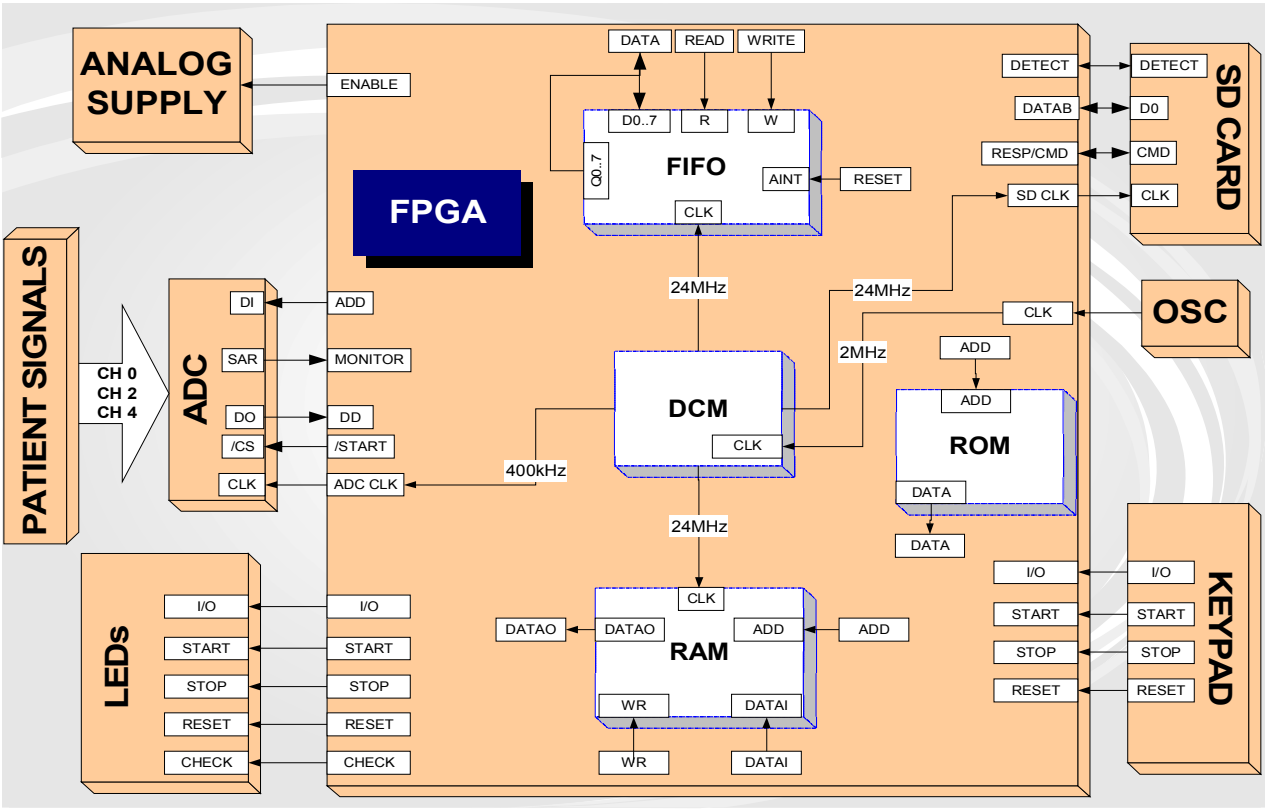

Fig. 1. System Block Diagram

-rail input and output and very low DC errors [9]. The general specifications for this part are:

- Low Input offset Voltage: typical ±20µV.
- Input range: -0.02 to 3.4V.
- Input Impedance: 10^{10} ohm.
- Common Mode Rejection Ratio (CMRR): 114dB.
- Bias Current I_b: ±0.2nA.
- Quiescent Current I_Q = 2.4 mA.

External resistors set a gain of 13000V/V and 1000 V/V for nasal airflow and respiratory efforts, respectively. The voltage range for the nasal airflow signal is from 0.35 to 2.95 volts, and for respiratory efforts is from 1 to 3 volts.

All signals are filtered to achieve the required frequency range from 0.1 to 15 Hz. For this purpose, we have chosen the TI TLV2764 single supply operational amplifiers [10]. The required bandwidth is achieved using a high-pass filter followed by a low-pass filter.

C. A/D Conversion

The 3 signals are sampled at 10 Hz. To achieve the proper digitization, while at the same time saving cost, space and power, the TI TLV0838 3-volt 8-bit ADC with serial control was chosen [11]. This device is an 8-bit successive approximation ADC with an input-configurable 8-channel multiplexer and serial input/output. In our design, the 8-channel multiplexer is software-configurable for single-ended input assignment. The 3 analog signals are connected to channels 0, 2 and 4. The clock frequency to the ADC is 400 kHz and it takes 14 clock cycles for 1 sample conversion. Thus, the 3 signals take 105 µs conversion time and should be repeated every 100 ms to achieve the 10 Hz sampling frequency. Channel selection, input configuration and conversion process are performed under software control using a serial data link from the FPGA chip.

D. CPU

As shown in fig.1, the main core of the digital subsystem is Xilinx Spartan-3 XC3S200-4TQ144C FPGA [12]. The FPGA chip requires 3 supply voltages, namely V_{cco}, V_{ccint} and V_{ccaux} of values 3.3V, 1.2V and 2.5V, respectively. Therefore, the most critical task, from the board design viewpoint, was the power distribution system (PDS) design. A solution made by TI was used in the design to supply the digital ICs and provide the 3 voltages needed by Spartan-3 chip.

One point in favor of Spartan-3 chip used in this design, is that it satisfies the requirements for ROM and RAM, through the provision of efficient SelectRAM™ memory blocks. In this design a ROM was needed to store the commands required for SD card. A RAM is needed also to store and retrieve system data such as number of interrupts during sleep period, relative card address for SD card

operation and number of written data blocks. In addition, storage of at least 512 bytes should be accomplished to be able to write on the SD card, which accepts data blocks of no less than multiples of 512-byte blocks. Therefore a FIFO is needed to accept data from ADC, and when 512 conversions is stored into the FIFO, it raises a flag to start the writing operation of SD card and so on. We have also used the embedded digital clock multipliers (DCM) inside the chip to yield the clocks of all embedded elements (RAM, and FIFO) in addition to the clock of SD card. The input clock to the chip is 2 MHz and the output clock is 24 MHz.

TABLE I
LED INDICATION

LED	ON Condition
I/O LED	the device is on and ready for operation
START LED	Start acquisition and normal operation
STOP LED	STOP key is pressed and operation is interrupted
RESET LED	resetting process
CONFIGURATION LED	configuration of FPGA using the PROM is complete
SYSTEM CHECK LED	Error in the system program. This is implemented using a small testing function in the program configuring the FPGA

TABLE II
KEY FUNCTIONS

KEY	ON Condition
I/O Key	On/Off operation of the device. When operation is off, the analog operation will be out of operation.
START Key	starts the acquisition of the device and storage of data into the SD Card
STOP Key	interrupts or pauses the operation of the device and is used by the patient when he or she wakes up in the middle of sleep time for any purpose and pressed again for resuming the operation.
RESET Key	reset the device operation, reconfiguring the FPGA and initialization of storage medium. It is used whenever unexpected error occurs to the device.

TABLE III
MAIN COMPONENTS

Qty	Code	Description
3	INA326	Instrumentation Amplifier
2	TLV2764	Operational Amplifier
1	TLV0838I	Analog to digital converter
1	TPS79533	Low-dropout regulator
1	XC3S200	Field programmable gate array
1	XCF02S	Configuration PROM
1	TPS75003	Triple-supply power management supply

Fig. 1 illustrates the use of Spartan-3 in addition to it interfaces to other circuit components. It shows also the built-in structure of ROM, RAM and FIFO inside the chip.

Two finite state machines (FSM) were used concurrently to perform the required processing operations.

The first FSM is responsible for data acquisition from the ADC. It controls and monitors the conversion process, select the channel to be converted, determines the sampling period and store the data into the FIFO. The second FSM is responsible for initializing, erasing and writing to the SD card. It is responsible also for sending data from FIFO to SD card. It is worth mentioning that although both machines execute concurrently, they depend on each other to some extent. This is due to some similar monitored parameters between both machines. One example of the similarity is the full or empty states of FIFO. Another example is that if the SD Card is not ready for storage or not detected, the analog regulator and ADC acquisition are disabled. Thus to reduce the superfluous power consumption in addition to avoiding erroneous states, the two state machines were linked together to shutdown superfluous functions.

Since the FPGA chip is SRAM-based, it is configured through a XCF02S platform configuration PROM. The design entry process and synthesis was performed using ISE® 5.2i from Xilinx. The design was simulated using ModelSim® SE plus, Modeltech/Mentor Graphics, USA.

E. Storage

The Secure Digital card is a flash-based memory card designed to operate in a low voltage range and communicate via nine-pin interface [13]. The SD card features 4-bits or 1-bit data bus. In this design, we use only 1-bit data line. Data transfer operations are protected by the cyclic redundancy check (CRC) codes; therefore, any bit changes induced by the card insertion or removal can be detected by the SD bus master. The ROM built into the FPGA stores the SD commands with 7-bits CRC. For data blocks, 16-bits CRC is generated by the finite state machine for data line D0 per transfer block. The SD card product manual in [13], in addition to the master thesis in [14], show the designed state machine required for SD card communication.

F. Display and Keypad

To save power requirements, we have used 6 5mm discrete low current, 2mA light emitting diodes (LED) for display purpose. 4 LEDs show user operations, while 2 LEDs are used for system check as shown in table I.

Surface mount momentary push button switches we used in the design to perform the following functions:
I/O Key, START Key, STOP Key, and RESET Key. Table II shows the function of each key.

G. *Power Supply*

In this design, we have separated analog and digital power supplies and grounds to achieve better performance in PCB design as will be shown shortly. Both analog and

digital regulators are powered by three AAA 1.5 volts batteries.

For analog components, we have used the TI TPS79533 low-dropout (LDO) low-power liner voltage regulator [15]. The regulator achieves continuous output current of 0 to 500 mA, which is very sufficient for analog circuitry consumption. In addition, it was chosen to get maximum accuracy of the 3.3 output voltage because the dropout voltage is 105 – 160 mV.

For powering digital components, including FPGA, we have used TI TPS75003 triple-supply power management IC as the most compact developed solution for powering Xilinx Spartan-3 FPGA [16]. This IC has two integrated buck controllers that allow supplies up to 3A for both CORE and I/O rails of FPGA and other digital ICs. A 300 mA LDO is integrated to provide and auxiliary rail used in our design to supply 2.5 volts to V_{ccaux} of Spartan-3.

H. Physical Features

The dimensions of the device are 20 x 70 x 100 mm and its weight is expected to be no more than 200 g according to the components utilized.

III. Discussion

We have taken a lot of precautions and recommendations that have great influence in the design process. This influence ranged from the most general points such as enclosure type and indicator colors and intensity up to the critical details such as via number and locations, spaces between traces and factors affecting electromagnetic compatibility EMC and electromagnetic interference EMI in PCB design. These factors were considered from the early stage of prototype definition in order to minimize the costs of EMC measures. In this section we will state some but not all of these precautions and recommendations.

The IEC601-1 standard was taken into consideration in this design; and accordingly, the device is class III (Internally powered equipment), type BF.

As a prototype, the PCB was designed as 6 layers. Two of them are used to connect pin headers to FPGA pins in order to connect them with logic analyzer for testing procedure. The other four layers are used as power plane, ground plane, and signal routing (2 layers).

Functional and timing simulation were conducted using ModelSim®, however, in-circuit validation and verification is still required in addition to field testing and clinical evaluation.

Table III shows the main component list used in this design. Further information about this design is shown in [14]

IV. Conclusion

We have presented the details of the hardware design of a device for home screening of sleep apnea syndrome. The device is battery operated, light weight, and easy to use by the average patient with minimal training. Date of overnight sleep from only three sensors is stored on a Secure Digital card and later processed by the sleep specialist. The ability to use this device at home and its cost make it suitable for mass use in screening and diagnosing sleep apnea syndromes.

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